CoolMOS™
AN-CoolMOS-07
CoolMOS - Frequently Asked Questions
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This application note answers frequently asked questions about technology and performance of CoolMOS™ power transistors.

1 Frequently Asked Questions

Q: What is CoolMOS?
A: CoolMOS is a new revolutionary technology for high voltage power MOSFETs. It implements a compensation structure in the vertical drift region of a MOSFET in order to improve the on state resistance.

![Diagram of CoolMOS™ power transistor in conducting and blocking states]

**Figure 1**

Higher doped columns act like a „short“ across the drift region

With applied $V_{DS}$, the space charge region extends across the entire epi-layer
- no free carrier
- high breakdown voltage

[Diagram of conducting and blocking states with labels and symbols]
Q: What is the main advantage of CoolMOS?
A: CoolMOS makes it possible to reduce the on-state resistance $R_{DS(on)}$ of a 600 V transistor by factor of 5 for the same chip area. It literally “breaks” the rules for the $R_{DS(on)}$ limitations of standard MOSFET technologies.

**Figure 2**

Q: Does CoolMOS have lower on-state resistance for the same package compared to other MOSFETs?
A: Yes, CoolMOS has a much lower on-state resistance in the same package.

**Figure 3**
Q: What advantage does CoolMOS low on-state resistance bring to the designer?
A: The conduction based power losses can be reduced dramatically, and therefore the heat generation. The efficiency of the power system increases. CoolMOS is capable to handle two to three times more output power depending on a converter type as a standard MOSFET in the same package.
On the other hand smaller packages can be used for the same output power of a converter.

Figure 4

- More Power in Same Package
- Less Package for Same Power
Q: What is the lowest on-state resistance in standard packages?
A: Best of class 600 V CoolMOS parts have
600 mΩ in D-Pak,
190 mΩ in TO-220,
70 mΩ in TO-247;

Figure 5
800 V CoolMOS transistors have 900 mΩ in D-Pak, 290 mΩ in TO-220 and in TO-247.

**Figure 6**

Q: Is the chip area of CoolMOS for the same on-state resistance $R_{\text{DS(on)}}$ smaller than in case of standard high-voltage MOSFET technology?
A: Yes, due to its main advantage the active chip area of CoolMOS is approximately 5 times smaller than that of standard MOSFET.

Q: Does CoolMOS have the smaller packages for the same on-state resistance as standard MOSFET?
A: Yes, for the same on-state resistance CoolMOS allows a smaller package. As an example, 600 V CoolMOS offers 600 mΩ in D-Pak, but the standard MOSFET technology has 750 mΩ in TO-220.

Q: How can designer use this advantage of CoolMOS smaller packages?
A: The volume of an SMPS or lamp ballast can be reduced, as well as the clearance between the MOSFET package and the case of SMPS or lamp ballast. It helps to improve the isolation strength and to save costs, e.g. less glue compound is needed to secure the components within the device's case. A full SMT design is possible now in many cases where in past expensive mixed mounting (SMT and trough-hole) was necessary.
Q: Does CoolMOS have also 5 times higher thermal resistance due to smaller chip size as the standard MOSFET for the same $R_{DS(on)}$?

A: No, due to a thinner chip and the heat-spreading effect of the internal leadframe the thermal resistance of CoolMOS is only slightly higher than in case of standard MOSFET for a similar current rating. For the same $R_{DS(on)}$, thermal impedance chip to case may be 2X (datasheet’s values), but this will often be only a small part (less than 10%) of the total thermal impedance $R_{th(J-A)}$ (junction to ambient), not having a significant affect in major applications.

![Figure 7 Total Thermal Resistance in SMPS](image)

**Table:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CoolMOS*</th>
<th>Standard MOSFET*</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thJC}$, [K/W]</td>
<td>1</td>
<td>0.45</td>
</tr>
<tr>
<td>iso-pad, [K/W]</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>heat sink, [K/W]</td>
<td>7.5</td>
<td>7.5</td>
</tr>
<tr>
<td>$R_{thJA}$, [K/W]</td>
<td>9.5</td>
<td>8.95</td>
</tr>
</tbody>
</table>

Only 6% higher total thermal resistance junction to ambient!

* same $R_{DS(on)}$.

Q: Does CoolMOS have a lower DC current rating compared to standard MOSFET for the same $R_{DS(on)}$?

A: Yes, due to higher thermal resistance of CoolMOS the maximum DC current rating for 25°C is lower according to the formal definition in the datasheet (see the table below). Device selection should be made based on actual overall power dissipation (which may be lower due to improved switching losses) and system thermal requirements.
Table 1: CoolMOS and Competitors Overview

<table>
<thead>
<tr>
<th>Datasheet values</th>
<th>$V_{DS}$</th>
<th>$R_{DSS}$</th>
<th>$I_{D}$ $T_{C} = 25^\circ C$</th>
<th>$I_{D}$ $T_{C} = 100^\circ C$</th>
<th>$I_{Dpuls}$</th>
<th>$R_{in}je$ K/W</th>
<th>$R_{G}$ rated</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPP03N60S5/C3</td>
<td>600</td>
<td>1.4 Ω</td>
<td>3.2 (25°C)</td>
<td>2 (100°C)</td>
<td>5.7 (25°C)</td>
<td>3.3</td>
<td>20 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRF820</td>
<td>500</td>
<td>3.0 Ω</td>
<td>2.5 (25°C)</td>
<td>1.6 (100°C)</td>
<td>8 (25°C)</td>
<td>2.5</td>
<td>18 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>SPP04N60S5/C2/C3</td>
<td>600</td>
<td>0.95 Ω</td>
<td>4.5 (25°C)</td>
<td>2.8 (100°C)</td>
<td>7.7 (25°C)</td>
<td>2.5</td>
<td>18 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRF830</td>
<td>500</td>
<td>1.5 Ω</td>
<td>4.5 (25°C)</td>
<td>2.9 (100°C)</td>
<td>18 (25°C)</td>
<td>1.7</td>
<td>12 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRFBC30</td>
<td>600</td>
<td>2.2 Ω</td>
<td>3.6 (25°C)</td>
<td>2.3 (100°C)</td>
<td>14 (25°C)</td>
<td>1.7</td>
<td>12 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>SPP07N60S5/C2/C3</td>
<td>600</td>
<td>0.6 Ω</td>
<td>7.3 (25°C)</td>
<td>4.6 (100°C)</td>
<td>14.6 (25°C)</td>
<td>1.5</td>
<td>12 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRFBC40</td>
<td>600</td>
<td>1.2 Ω</td>
<td>6.2 (25°C)</td>
<td>3.9 (100°C)</td>
<td>25 (25°C)</td>
<td>1</td>
<td>9.1 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRFBC40LC</td>
<td>600</td>
<td>1.2 Ω</td>
<td>6.2 (25°C)</td>
<td>3.9 (100°C)</td>
<td>25 (25°C)</td>
<td>1</td>
<td>9.1 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRF840</td>
<td>500</td>
<td>0.85 Ω</td>
<td>8.0 (25°C)</td>
<td>5.1 (100°C)</td>
<td>32 (25°C)</td>
<td>1</td>
<td>9.1 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>SPP11N60S5/C2/C3</td>
<td>600</td>
<td>0.38 Ω</td>
<td>11 (25°C)</td>
<td>7 (100°C)</td>
<td>22 (25°C)</td>
<td>1</td>
<td>6.8 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRFP450</td>
<td>500</td>
<td>0.40 Ω</td>
<td>14 (25°C)</td>
<td>8.7 (100°C)</td>
<td>56 (25°C)</td>
<td>0.65</td>
<td>6.2 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>IRFPC60</td>
<td>600</td>
<td>0.40 Ω</td>
<td>16 (25°C)</td>
<td>10 (100°C)</td>
<td>64 (25°C)</td>
<td>0.45</td>
<td>4.5 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>2SK2889</td>
<td>600</td>
<td>0.75 Ω</td>
<td>10 (25°C)</td>
<td>40 (25°C)</td>
<td>1.25</td>
<td>k.A.</td>
<td>(TO220)</td>
<td></td>
</tr>
<tr>
<td>SGP06N60 IGBT</td>
<td>600</td>
<td>2 V @ 6 A</td>
<td>14 (25°C)</td>
<td>6 (100°C)</td>
<td>28 (25°C)</td>
<td>50</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>SPP20N60S5/C2/C3</td>
<td>600</td>
<td>0.19 Ω</td>
<td>20 (25°C)</td>
<td>13 (100°C)</td>
<td>40 (25°C)</td>
<td>0.6</td>
<td>3.6 Ω</td>
<td>TO220</td>
</tr>
<tr>
<td>IRFP460</td>
<td>500</td>
<td>0.27 Ω</td>
<td>20 (25°C)</td>
<td>13 (100°C)</td>
<td>80 (25°C)</td>
<td>0.45</td>
<td>4.3 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>STW20NB50</td>
<td>500</td>
<td>0.27 Ω</td>
<td>20 (25°C)</td>
<td>12.7 (100°C)</td>
<td>80 (25°C)</td>
<td>0.5</td>
<td>4.7 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>IXFH20N60</td>
<td>600</td>
<td>0.35 Ω</td>
<td>20 (25°C)</td>
<td>12.5 (100°C)</td>
<td>80 (25°C)</td>
<td>0.42</td>
<td>2 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>MTW20N50E</td>
<td>500</td>
<td>0.24 Ω</td>
<td>20 (25°C)</td>
<td>14.1 (100°C)</td>
<td>60 (25°C)</td>
<td>0.5</td>
<td>9.1 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>SPW47N60S5/C2/C3</td>
<td>600</td>
<td>0.07 Ω</td>
<td>47 (25°C)</td>
<td>30 (100°C)</td>
<td>94 (25°C)</td>
<td>0.3</td>
<td></td>
<td>TO247</td>
</tr>
<tr>
<td>IXFX44N60</td>
<td>600</td>
<td>0.13 Ω</td>
<td>44 (25°C)</td>
<td>27.5 (100°C)</td>
<td>176 (25°C)</td>
<td>0.22</td>
<td>1 Ω</td>
<td>TO247</td>
</tr>
<tr>
<td>STY34NB50</td>
<td>500</td>
<td>0.13 Ω</td>
<td>34 (25°C)</td>
<td>21.4 (100°C)</td>
<td>136 (25°C)</td>
<td>0.277</td>
<td>4.7 Ω</td>
<td>TO247</td>
</tr>
</tbody>
</table>

Q: Does CoolMOS have a lower pulse current rating compared to standard MOSFET for the same $R_{DSS}$?

A: Yes, due to higher gate-source threshold voltage and very high current density in the compensation structure of CoolMOS the pulse current rating is lower. The new CoolMOS C3 offers a lower gate source threshold voltage resulting in higher pulse current rating compared to the former families S5 and C2. This new family is comparable in these parameters with a standard MOSFET.
Q: Does the lower pulse current rating of CoolMOS affect the power handling capability in the focus applications?

A: No, in the majority of focus applications (SMPS, lamp ballast) it does not affect the power handling capability because the transistors operating conditions are characterized by external cooling and currents are far below the MOSFET’s rated currents. Tables below demonstrate the peak and r.m.s. currents in frequently used topologies.

Table 2  Flyback Converter (discontinuous current mode)

<table>
<thead>
<tr>
<th>$P_{\text{out}}$ [W]</th>
<th>19</th>
<th>30</th>
<th>50</th>
<th>75</th>
<th>100</th>
<th>150</th>
<th>200</th>
<th>250</th>
<th>300</th>
<th>400</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{p_{\text{max}}}$ [A]</td>
<td>0.6</td>
<td>1.0</td>
<td>1.6</td>
<td>2.4</td>
<td>3.2</td>
<td>4.7</td>
<td>6.3</td>
<td>7.9</td>
<td>9.4</td>
<td>12.6</td>
</tr>
<tr>
<td>$I_{p_{\text{rms}}}$ [A]</td>
<td>0.16</td>
<td>0.25</td>
<td>0.42</td>
<td>0.62</td>
<td>0.83</td>
<td>1.25</td>
<td>1.66</td>
<td>2.08</td>
<td>2.50</td>
<td>3.32</td>
</tr>
</tbody>
</table>

Table 3  Forward Converter (continuous current mode)

<table>
<thead>
<tr>
<th>$P_{\text{out}}$ [W]</th>
<th>50</th>
<th>75</th>
<th>100</th>
<th>150</th>
<th>200</th>
<th>300</th>
<th>400</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{p_{\text{max}}}$ [A]</td>
<td>0.3</td>
<td>0.5</td>
<td>0.7</td>
<td>1.0</td>
<td>1.3</td>
<td>2.0</td>
<td>2.6</td>
<td>3.2</td>
</tr>
<tr>
<td>$I_{p_{\text{rms}}}$ [A]</td>
<td>0.31</td>
<td>0.46</td>
<td>0.62</td>
<td>0.93</td>
<td>1.23</td>
<td>1.9</td>
<td>2.5</td>
<td>3.08</td>
</tr>
</tbody>
</table>

On the contrary, due to the very low total power losses, CoolMOS yields a superior system efficiency and allows to increase output power in most focus applications (see the chart below).

Flyback converter
$T_J=110^\circ\text{C}, T_A=60^\circ\text{C}, R_{\text{th, junction}}=10\text{K/W}, V_{\text{BUS}}=380\text{V}, D=17\%$

Figure 8  CoolMOS™ C3: Superior Power Handling Capability

Due to its superior switching characteristic third generation of CoolMOS can handle up to 30% more output power of a converter as the standard MOSFET with same $R_{\text{DS(on)}}$. 
Just compare the 0.4 Ω / 600 V standard MOSFET curve with 0.38 Ω / 600 V CoolMOS C3 curve in the chart. In the same package (e.g. TO-220) CoolMOS C3 makes it possible to triple the output power of a converter compared to conventional MOSFET under the same operating conditions.

Q: Does CoolMOS have a lower gate charge compared to standard MOSFET for the same $R_{DS(on)}$?

A: Yes, the CoolMOS has almost 2 times lower gate charge as the standard MOSFET for the same $R_{DS(on)}$.

![Figure 9 CoolMOS™ low Gate Charge Technology is a Benchmark](image)

Q: How can designer use this advantage of CoolMOS lower gate charge?

A: The gate drive power rating as well as the switching power losses can be significantly reduced.

Q: Does CoolMOS have lower capacitance’s than a standard MOSFET of the same $R_{DS(on)}$?

A: Yes, the input and reverse capacitance’s of CoolMOS transistors are considerably lower. Chart on the right demonstrates the capacitance’s vs. drain-source voltage curves. The output capacitance of CoolMOS has a very interesting behavior. It has a higher value at low drain-source voltage up to 50 V and a very low value at higher voltages. The effective value of output capacitance of CoolMOS is lower then in case of standard MOSFET. That leads to lower switching losses.
Q: What is the reason for the highly non-linear output capacitance of CoolMOS?
A: The usual voltage dependent capacitance characteristic of power MOSFETs is determined by the expansion of the space charge layer (depletion region) between the p-wells and n-drift region. This behavior can be visualized like a plate capacitance, for which the distance between the two plates increases as a function of voltage. CoolMOS is additionally characterized by a 3D-folded surface of the p-column and their adjacent n-regions, which is depleted at a voltage around 50 V. In other words - and to stay within the picture of the plate capacitance - the distance of the plates increases as well as the surface of the plates decreases as a function of voltage. Therefore a double nonlinear behavior is observed.

Q: How can designer benefit from output capacitance behavior of CoolMOS?
A: The lower effective value of output capacitance of CoolMOS means that there is less energy stored in the output capacitance. This leads to reduction of switching losses stemming from charging and discharging the output capacitance.
Q: Do the CoolMOS devices have avalanche ruggedness?
A: Yes, CoolMOS transistors have single pulse and repetitive avalanche ratings. The area specific amount of avalanche energy is a benchmark value. Due to smaller chip area for the same on-state resistance the absolute value of avalanche energy is lower then in case of standard MOSFET of the same $R_{DS(on)}$.

CoolMOS introduces a new specification for repetitive avalanche, where the greatest application need arises. Please refer to Application Note 1 for more information.

Q: How can designer benefit from the new avalanche specification of CoolMOS?
A: Many of the focus applications have a triangle waveform for the drain current, e.g. the Flyback converter. This current waveform leads to very high crest factor, i.e. the peak to r.m.s. ratio of drain current, and potentially high peak avalanche current. For these applications it is advantageous to have a specification that describes the avalanche current waveforms. The new avalanche specification for CoolMOS was developed to meet these requirements. Diagram on the right shows the new avalanche Safe Operating Area. The color lines correspond to the drain current during the avalanche in Flyback designs from 50 to 250 W. They are well inside the Safe Operating Area. Please refer to Application Note 1 for more information.
Figure 12   CoolMOS can handle repetitive avalanche in all Flyback designs!

Q: Does CoolMOS have an internal anti-parallel diode like a standard MOSFET?
A: Yes, CoolMOS transistors have an internal anti-parallel diode (body diode). The performance of this diode is similar to that of standard MOSFETs. We do not recommend using CoolMOS in topologies that have freewheeling load current conducted in the body diode, and which switch the opposite transistor in the bridge leg on the conducting body diode. The recovered charge and overall characteristics of the body diode are comparable or superior to many standard MOSFETs, but current commutation is very “snappy”, resulting in high di/dt at the completion of commutation, and the likelihood of severe over-voltage transients due to the resulting high dv/dt.

Q: Does CoolMOS have a different gate-source threshold voltage and transconductance than a standard MOSFET?
A: The first two generations offer a higher threshold voltage compared to a standard MOSFET. The transconductance is lower and comparable to other compensation devices available on the market. The CoolMOS C3 offers the same threshold voltage as well as the transconductance than a standard MOSFET with an outstanding peak current capability.
Q: What is the production yield for CoolMOS?
A: Despite the fact that CoolMOS has advanced vertical structure, the production yield is high. It corresponds to our high manufacturing standards and experience in VLSI design and manufacturing.

Q: Does CoolMOS have high quality and reliability standards?
A: The CoolMOS transistors have the same high quality and reliability standards as our automotive devices. Please refer to www.infineon.com for more information regarding quality and reliability. Qualification packages are also available there.

Q: What is the difference between the S5 and C2/C3 types of CoolMOS regarding switching speed?
A: The S5 types are the first generation of CoolMOS. These devices have relatively high internal gate resistance and moderate switching speed. The C2 and C3 types form the second generation of CoolMOS utilize an ultra-fast switching technology due to different gate structure. This technology makes it possible to realize very low internal gate resistance and very fast switching transitions.
Q: How can the designer benefit from the ultra-fast switching technology of CoolMOS C2 and C3?

A: Due to very fast switching transitions (turn on and turn off) the switching losses can be dramatically reduced. In combination with low gate charge and lower effective output capacitance, it makes CoolMOS C2 and C3 the fastest high voltage power MOSFETs available on the market. The superior switching performance of CoolMOS C2 and C3 makes it possible to increase the operating frequency in order to reduce the volume and weight of passive components such as transformers, inductors, and capacitors.

<table>
<thead>
<tr>
<th>Type</th>
<th>$R_{gate\text{ (internal), typical}}$ [Ω]</th>
<th>Type</th>
<th>$R_{gate\text{ (internal), typical}}$ [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPD01N60S5</td>
<td>19.01</td>
<td>SPD01N60S5</td>
<td>19.01</td>
</tr>
<tr>
<td>SPP02N60S5</td>
<td>7.7</td>
<td>SPP02N60S5</td>
<td>7.7</td>
</tr>
<tr>
<td>SPP03N60S5</td>
<td>9.8</td>
<td>SPP03N60S5</td>
<td>9.8</td>
</tr>
<tr>
<td>SPP04N60S5</td>
<td>19.74</td>
<td>SPP04N60C2</td>
<td>0.95</td>
</tr>
<tr>
<td>SPP07N60S5</td>
<td>19.09</td>
<td>SPP07N60C2</td>
<td>0.8</td>
</tr>
<tr>
<td>SPP11N60S5</td>
<td>28.52</td>
<td>SPP11N60C2</td>
<td>0.86</td>
</tr>
<tr>
<td>SPP20N60S5</td>
<td>12.14</td>
<td>SPP20N60C2</td>
<td>0.54</td>
</tr>
<tr>
<td>SPW47N60S5</td>
<td>8.7</td>
<td>SPW47N60C2</td>
<td>0.62</td>
</tr>
</tbody>
</table>

Figure 14  50% Ratio in Switching Losses Compared to Standard MOSFET
Q: Can the designer adjust the switching speed of CoolMOS C2 and C3 by an external gate resistor?
A: Yes, simply changing the value of external gate resistor designer can control both the voltage and current slope during turn on and turn off transients in a very wide range.

Figure 15  Current and VoltageSlopes can be controlled over an extreme wide range

Q: Does fast switching cause additional EMI noise?
A: The theory says in general - faster switching causes more noise. The EMI noise can be influenced by many issues, including the switching speed of transistors, PCB layout, geometrical positioning of components, case construction, materials for thermal insulators, use of shield insulators, etc. The designer has a lot of possibilities for optimizing the EMI behavior. If the layout is well done the switching speed of transistor can be increased. Another possibility can be to slow down the switching speed of transistor, what can be easily done by adjusting the external gate resistor. Please refer to Application Note 2 for more information.
Q: Can designer use CoolMOS in their simulation tools?
A: Yes, the simulation models for CoolMOS can be downloaded at www.infineon.com

Q: Where can I get more information about CoolMOS?
A: Please refer to our Web site - www.infineon.com/CoolMOS


2 List of Related Application Notes

Application Note 1: Introduction to Avalanche Considerations for S5 and C2 CoolMOS, SMPS Applications (AN-CoolMOS-04)

Application Note 2: How to Control the C2 CoolMOS and its EMI behavior (AN-CoolMOS-01)
Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results. Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher