

2.1-Channel Digital Audio Amplifier with Headphone Driver

Features

- I 16/18/20/24-bit input with I²S, Left-alignment and Right-alignment data format
- I PSNR & DR(A-weighting)
Loudspeaker: 98dB (PSNR), 99dB (DR)
Headphone: 85dB (PSNR), 95dB (DR)
- I Multiple sampling frequencies (Fs)
32KHz / 44.1KHz / 48KHz and
64KHz / 88.2KHz /96KHz
- I System clock = 64x, 128x, 192x, 256x, 384x,
512x, 576x, 768x, 1024x Fs
- I Supply voltage
3.0~12V for loudspeaker driver
3.0~3.3V for others
- I 2.5~5.5V tolerant input interface
- I Loudspeaker output power
2x10W(Full,8Ω)+20W(Full, 4Ω) for 2.1-channel
2x5W(Half,4Ω)+20W(Full, 4Ω) for 2.1-channel
2x10W(Full,8Ω) for stereo
2x5W(Half,4Ω) for stereo
2x20W(Full, 4Ω) for stereo
- I Headphone power
34mW into 32Ω@1KHz and 1% THD+N
65mW into 16Ω@1KHz and 1% THD+N
110mW into 8Ω@1KHz and 1% THD+N
200mW into 4Ω@1KHz and 1% THD+N
- I Sound processing including :
Bass (+18dB~-12dB, 3dB frequency is 250Hz),
Treble (+18dB~-12dB, 3dB frequency is 7kHz),
5 bands parametric EQ,
Volume control (+24dB~-103dB, 1dB/step) and
Dynamic range control

- I Anti-pop design
- I Over-temperature protection
- I Under-voltage shutdown
- I Short-circuit protection
- I I²C control interface

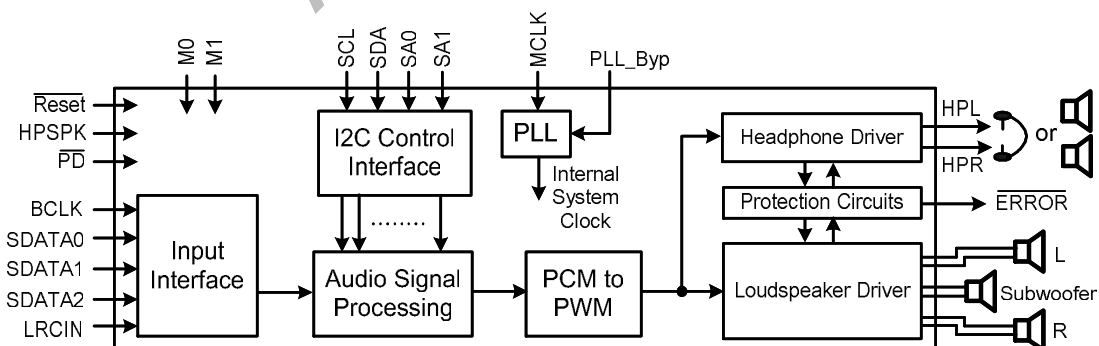
Applications

- I CD and DVD
- I TV audio
- I Car audio
- I Boom-box
- I MP3 docking systems
- I Portable / Handheld
- I PDA
- I Wireless audio
- I USB speaker

Description

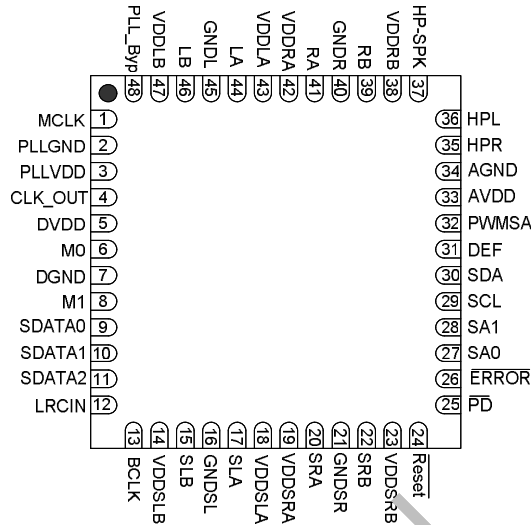
This is a 2.1-channel fully digital audio amplifier with output power which can deliver up to 2x10W to 8Ω load for L,R channel and 20W to 4Ω load for sub-woofer channel simultaneously with 12V supply voltage. AD8356 provides I²C-compatible software control mode. Sound processing includes Bass, Treble, EQ and Dynamic range control which are all available in software control mode. Users can use one AD8356 for stereo or 2.1-channel, two for 5.1-channel and three for 7.1-channel, respectively.

Functional Block Diagram



* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

Pin Assignment



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	MCLK	I	Master clock input	5V tolerant Schmitt trigger TTL input buffer
2	PLLGND	P	Ground for PLL	
3	PLLVDD	P	Supply for PLL	(Note1)
4	CLK_OUT	O	PLL output	5V tolerant TTL output buffer
5	DVDD	P	Digital Power	(Note1)
6	M0	I	Mode selection 0	5V tolerant Schmitt trigger TTL input buffer
7	DGND	P	Digital Ground	
8	M1	I	Mode selection 1	5V tolerant Schmitt trigger TTL input buffer
9	SDATA0	I	Serial audio data input 0	5V tolerant Schmitt trigger TTL input buffer
10	SDATA1	I	Serial audio data input 1	5V tolerant Schmitt trigger TTL input buffer
11	SDATA2	I	Serial audio data input 2	5V tolerant Schmitt trigger TTL input buffer
12	LRCIN	I	Left/Right clock input (Fs)	5V tolerant Schmitt trigger TTL input buffer
13	BCLK	I	Bit clock input (64Fs)	5V tolerant Schmitt trigger TTL input buffer
14	VDDSLB	P	Supply for subwoofer-left channel B	(Note2)
15	SLB	O	Subwoofer-left channel output (-)	
16	GNDSL	P	Ground for subwoofer-left channel	
17	SLA	O	Subwoofer-left channel output (+)	
18	VDDSLA	P	Supply for subwoofer-left channel A	(Note2)
19	VDDSRB	P	Supply for subwoofer-right channel B	(Note2)
20	SRA	O	Subwoofer-right channel output (+)	
21	GNDSR	P	Ground for subwoofer-right channel	
22	SRB	O	Subwoofer-right channel output (-)	
23	VDDSRB	P	Supply for subwoofer-right channel B	(Note2)

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

24	$\overline{\text{Reset}}$	I	Reset, low active	5V tolerant Schmitt trigger TTL input buffer
25	$\overline{\text{PD}}$	I	Power down, low active	5V tolerant Schmitt trigger TTL input buffer
26	$\overline{\text{ERROR}}$	O	ERROR output	Open-drain output
27	SA0	I	I ² C select address 0	5V tolerant Schmitt trigger TTL input buffer
28	SA1	I	I ² C select address 1	5V tolerant Schmitt trigger TTL input buffer
29	SCL	I	I ² C serial clock input	5V tolerant Schmitt trigger TTL input buffer
30	SDA	I	I ² C serial data input	5V tolerant Schmitt trigger TTL input buffer with open-drain output
31	DEF	I	Default volume, 0=Mute, 1=Un-Mute	5V tolerant Schmitt trigger TTL input buffer
32	PWMSA	O	Half-bridge, sub-woofer channel output	5V tolerant TTL output buffer
33	AVDD	P	Analog supply	(Note1)
34	AGND	P	Analog ground	
35	HPR	O	Headphone right channel output	
36	HPL	O	Headphone left channel output	
37	HP-SPK	I	Headphone detection	
38	VDDR _B	P	Supply for right channel B	(Note2)
39	RB	O	Right channel output (-)	
40	GND _R	P	Ground for Right channel	
41	RA	O	Right channel output (+)	
42	VDD _R A	P	Supply for right channel A	(Note2)
43	VDD _L A	P	Supply for left channel A	(Note2)
44	LA	O	Left channel output (+)	
45	GND _L	P	Ground for left channel	
46	LB	O	Left channel output (-)	
47	VDD _L B	P	Supply for left channel B	(Note2)
48	PLL_Byp	I	PLL Bypass	5V tolerant Schmitt trigger TTL input buffer

Note1 : These pins provide the supply for digital PWM controller, headphone drivers, built-in PLL and protection circuits except for loudspeaker short-circuit protection circuits.

Note2 : These pins provide the supply for loudspeaker driver stages.

Available Package

Package Type	Device No.	Thermal resistance
7x7 48L QFN	AD8356NC	(Typical) $\theta_{ja}=24.5^{\circ}\text{C}/\text{W}$ (Condition : 4-Layer PCB)
7x7 48L LQFP	AD8356LC	(Typical) $\theta_{ja}=55.5^{\circ}\text{C}/\text{W}$ (Condition : 4-Layer PCB)

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	0	3.6	V
AVDD	Supply for Analog Circuit	0	3.6	V
PLLVD	Supply for PLL Circuit	0	3.6	V
	Supply for Driver Stage	0	13.5	V
V_i	Input Voltage	-0.3	5.5	V
T_{stg}	Storage Temperature	-45	150	°C
T_a	Ambient Operating Temperature	-40	85	°C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.0~3.3	V
AVDD	Supply for Analog Circuit	3.0~3.3	V
PLLVD	Supply for PLL Circuit	3.0~3.3	V
	Supply for Driver Stage	5.0~12.0	V
T_a	Ambient Operating Temperature	-10~70	°C

Digital Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{OH}	High-Level Output Voltage	2.4			V
V_{OL}	Low-Level Output Voltage			0.4	V
C_i	Input Capacitance		6.4		pF

General Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}	Supply Current during Power Down			23		μA
	Junction Temperature for Driver Shutdown			150		°C
	Temperature Hysteresis for Recovery from Shutdown			30		°C
UV_H	Under Voltage Disabled (For PLLVD)			2.8		V
UV_L	Under Voltage Enabled (For PLLVD)			2.7		V
R_{SC}	Loudspeaker Short-Circuit Detection (Note3)	Normal channel			6.8	Ω
	Loudspeaker Short-Circuit Detection (Note3)	Subwoofer channel			3.4	Ω
R_{SCH}	Headphone Output Short-Circuit Detection				3.4	Ω

Note3: Loudspeaker short-circuit protection is effective when loudspeaker drivers are properly connected with external LC filters. Please also refer to Note5.

Electrical Characteristics and Specifications for 8W Loudspeaker (Note5)

Condition: DVDD=AVDD=3.3V, VDDL=VDDR=12V, F_S=48kHz, Load=8Ω with passive LC lowpass filter (L=10 μH with R_{DC}=0.12Ω, C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P _{OMAX}	Maximum Output Power (Normal Ch.)	+24dB volume	0dB		13.5		W
P _{OMAX(Sub)}	Maximum Output Power (Subwoofer)	+24dB volume	0dB		26		W
P _O	RMS Output Power (THD=10%)	+8dB volume	-6.2dB		9		W
	RMS Output Power (THD=1%)	+8dB volume	-8dB		7		W
THD+N	Total Harmonic Distortion+Noise(Note4)	P _o =5.6W	-1dB		0.5		%
SNR	Signal to Noise Ratio(Note4)	P _o =5.6W	-1dB		96		dB
DR	Dynamic Range(Note4)		-60dB		98		dB
PSRR	Power Supply Rejection Ratio		-60dB		60		dB
	Channel Separation		-1dB		82		dB
<i>h</i>	Efficiency	2x13.5W+26W	0dB		88		%

Note4: Measured with A-weighting filter

Note5: The characteristics, such as: P_{OMAX}, P_{OMAX(Sub)} and efficiency, shown in above table are measured with "2.1-channel" configuration (Please refer to application circuit example section), where "2" stands for two normal L and R channels with two 8Ω loads and ".1" for one subwoofer channel with 4Ω load. The characteristic in this table are only for L and R channels of 2.1-channel configuration. The subwoofer channel characteristics is in the next table for the stereo configuration.

Electrical Characteristics and Specifications for 4W Loudspeaker (Note6)

Condition: DVDD=AVDD=3.3V, VDDL=VDDR=12V, F_S=48kHz, Load=4Ω with passive LC lowpass filter (L=10 μH with R_{DC}=0.06Ω, C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P _{OMAX}	Maximum RMS Output Power	+24dB volume	0dB		26		W
P _O	RMS Output Power (THD=10%)	+8dB volume	-6.2dB		18		W
	RMS Output Power (THD=1%)	+8dB volume	-8dB		14		W
THD+N	Total Harmonic Distortion+Noise(Note4)	P _o =11.2W	-1dB		1		%
SNR	Signal to Noise Ratio(Note4)	P _o =11.2W	-1dB		96		dB
DR	Dynamic Range(Note4)		-60dB		98		dB
PSRR	Power Supply Rejection Ratio		-60dB		60		dB
	Channel Separation		-1dB		82		dB
<i>h</i>	Efficiency	P _O =2x26W	0dB		88		%

Note6: The characteristics, such as: P_{OMAX}, P_{OMAX(Sub)} and efficiency, shown in above table are measured with stereo configuration (For stereo configuration, please refer to application circuit example section).

Electrical Characteristics and Specifications for Headphone

Condition: DVDD=AVDD=3.3V, $F_s=48\text{kHz}$, Load= 32Ω with DC decoupling capacitor ($C_{DC}=100\mu\text{F}$) and passive LC lowpass filter ($L=220\mu\text{H}$, $C=0.068\mu\text{F}$); Input is 1kHz sinewave. MCLK duty cycle is $50\pm 1\%$.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_o	RMS Output Power for Each Channel		0dB		34		mW
I_{cc}	Required Supply Current	2 channel	-9dB		12		mA
THD+N	Total Harmonic Distortion+Noise(Note4)	$P_o=0.4\text{mW}$			0.048		%
SNR	Signal to Noise Ratio(Note4)	$P_o=26\text{mW}$	-1.3dB		86		dB
DR	Dynamic Range(Note4)		-60dB		96		dB
	Channel Separation		-1.3dB		60		dB
h	Efficiency	$P_o=34\text{mW}$	0dB		72		%

Condition: DVDD=AVDD=3.3V, $F_s=48\text{kHz}$, Load= 16Ω with DC decoupling capacitor ($C_{DC}=220\mu\text{F}$) and passive LC lowpass filter ($L=100\mu\text{H}$, $C=0.15\mu\text{F}$); Input is 1kHz sinewave. MCLK duty cycle is $50\pm 1\%$.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_o	RMS Output Power for Each Channel		0dB		65		mW
I_{cc}	Required Supply Current	2 channel	-9dB		15		mA
THD+N	Total Harmonic Distortion+Noise(Note4)	$P_o=3\text{mW}$			0.09		%
SNR	Signal to Noise Ratio(Note4)	$P_o=49\text{mW}$	-1.3dB		82		dB
DR	Dynamic Range(Note4)		-60dB		96		dB
	Channel Separation		-1.3dB		55		dB
h	Efficiency	$P_o=65.3\text{mW}$	0dB		75		%

Condition: DVDD=AVDD=3.3V, $F_s=48\text{kHz}$, Load= 8Ω with DC decoupling capacitor ($C_{DC}=470\mu\text{F}$) and passive LC lowpass filter ($L=47\mu\text{H}$, $C=0.33\mu\text{F}$); Input is 1kHz sinewave. MCLK duty cycle is $50\pm 1\%$.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_o	RMS Output Power for Each Channel		0dB		110		mW
I_{cc}	Peak Supply Current	2 channel	-9dB		20		mA
THD+N	Total Harmonic Distortion+Noise(Note4)	$P_o=4\text{mW}$			0.1		%
SNR	Signal to Noise Ratio(Note4)	$P_o=82\text{mW}$	-1.3dB		80		dB
DR	Dynamic Range(Note4)		-60dB		96		dB
	Channel Separation		-1.3dB		54		dB
h	Efficiency	$P_o=110\text{mW}$	0dB		76		%

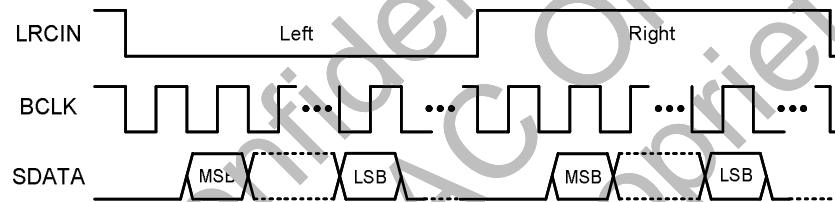
* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

Condition: DVDD=AVDD=3.3V, $F_S=48\text{kHz}$, Load= 4Ω with DC decoupling capacitor ($C_{DC}=470\mu\text{F}$) and passive LC lowpass filter ($L=22\mu\text{H}$, $C=0.68\mu\text{F}$); Input is 1kHz sinewave. MCLK duty cycle is $50\pm 1\%$.

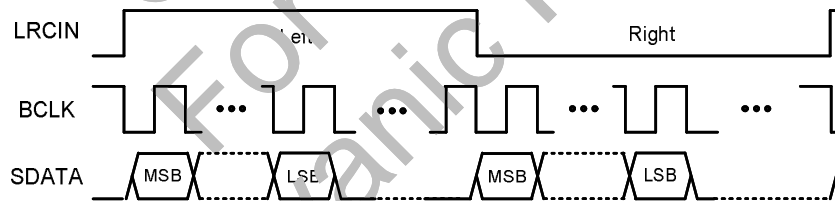
Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_o	RMS Output Power for Each Channel		0dB		200		mW
I_{cc}	Peak Supply Current	2 channel	-9dB		30		mA
THD+N	Total Harmonic Distortion+Noise(Note4)	$P_o=6\text{mW}$			0.2		%
SNR	Signal to Noise Ratio(Note4)	$P_o=150\text{mW}$	-1.3dB		78		dB
DR	Dynamic Range(Note4)		-60dB		95		dB
	Channel Separation		-1.3dB		52		dB
h	Efficiency	$P_o=200\text{mW}$	0dB		78		%

Interface Configuration

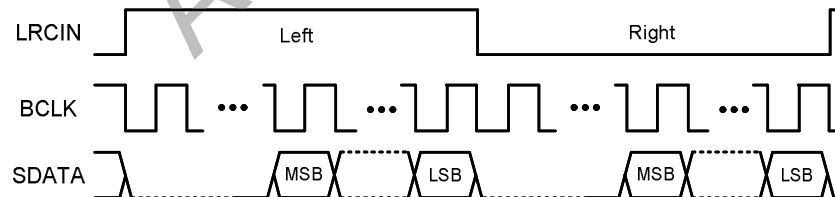
I²S



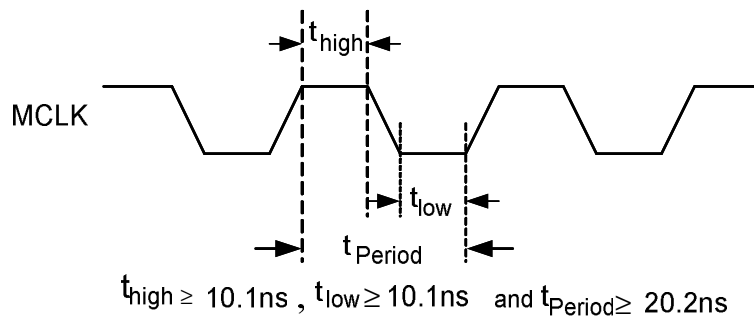
I Left-Alignment



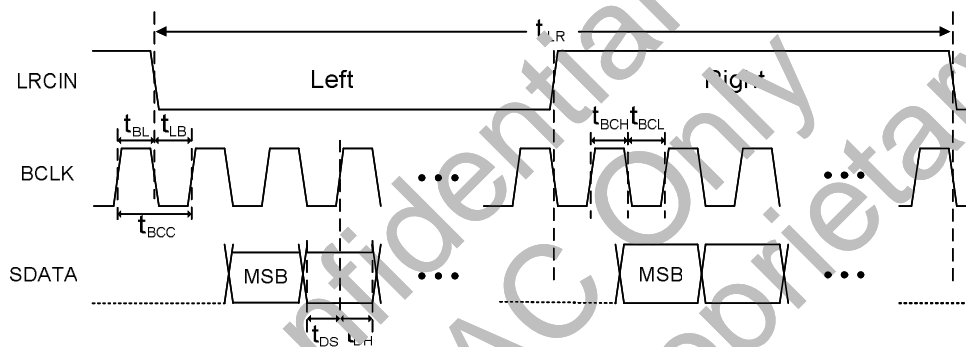
I Right-Alignment



I System Clock Timing

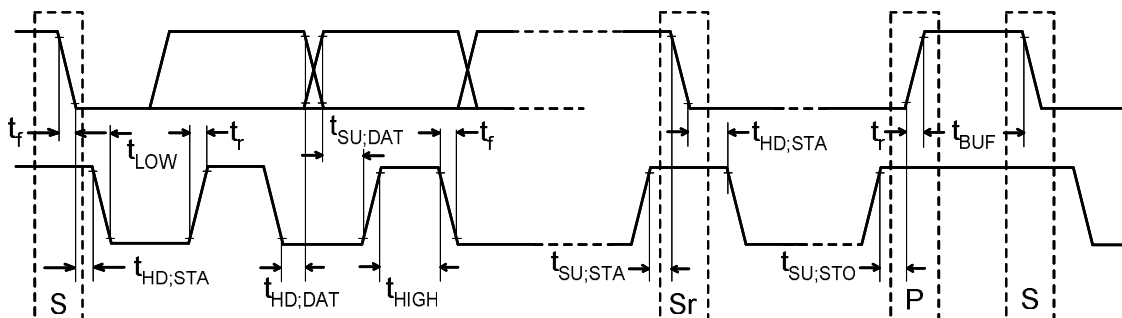


I Timing Relationship (Using I²S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	81.38		244	ns
t_{BCL}	BCLK Pulse Width Low	81.38		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

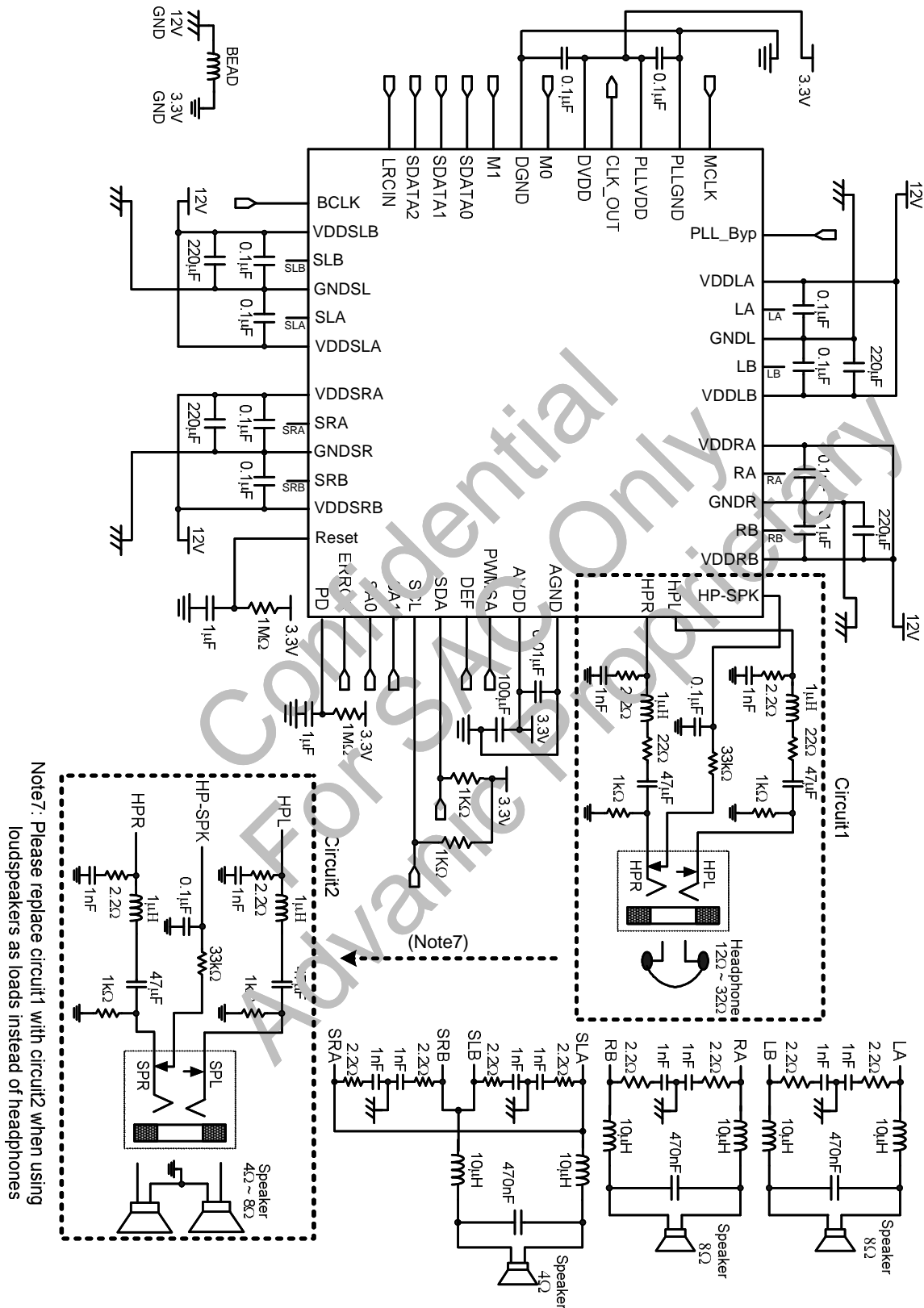
I I²C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for a repeated START condition	$t_{SU,STA}$	4.7	---	0.6	---	μs
Data hold time for I ² C bus devices	$t_{HD,DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU,DAT}$	250	---	100	---	ns
Rise time of both SDA and SDL signals	t_r	---	1000	$20+0.1C_b$	300	ns
Fall time of both SDA and SDL signals	t_f	---	300	$20+0.1C_b$	300	ns
Setup time for STOP condition	$t_{SU,STO}$	4.0	---	0.6	---	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

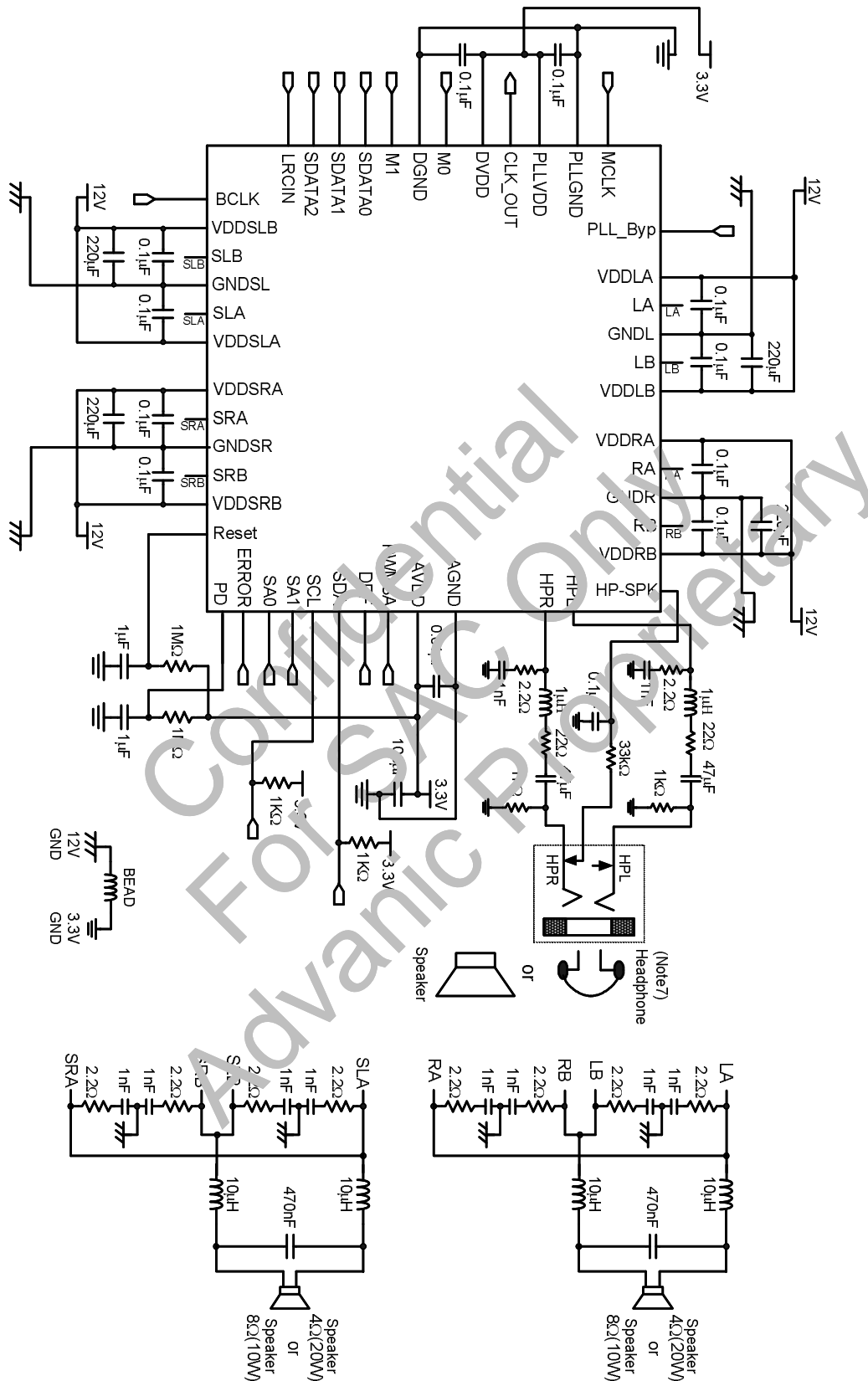
* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

Application Circuit Example (2.1-channel)



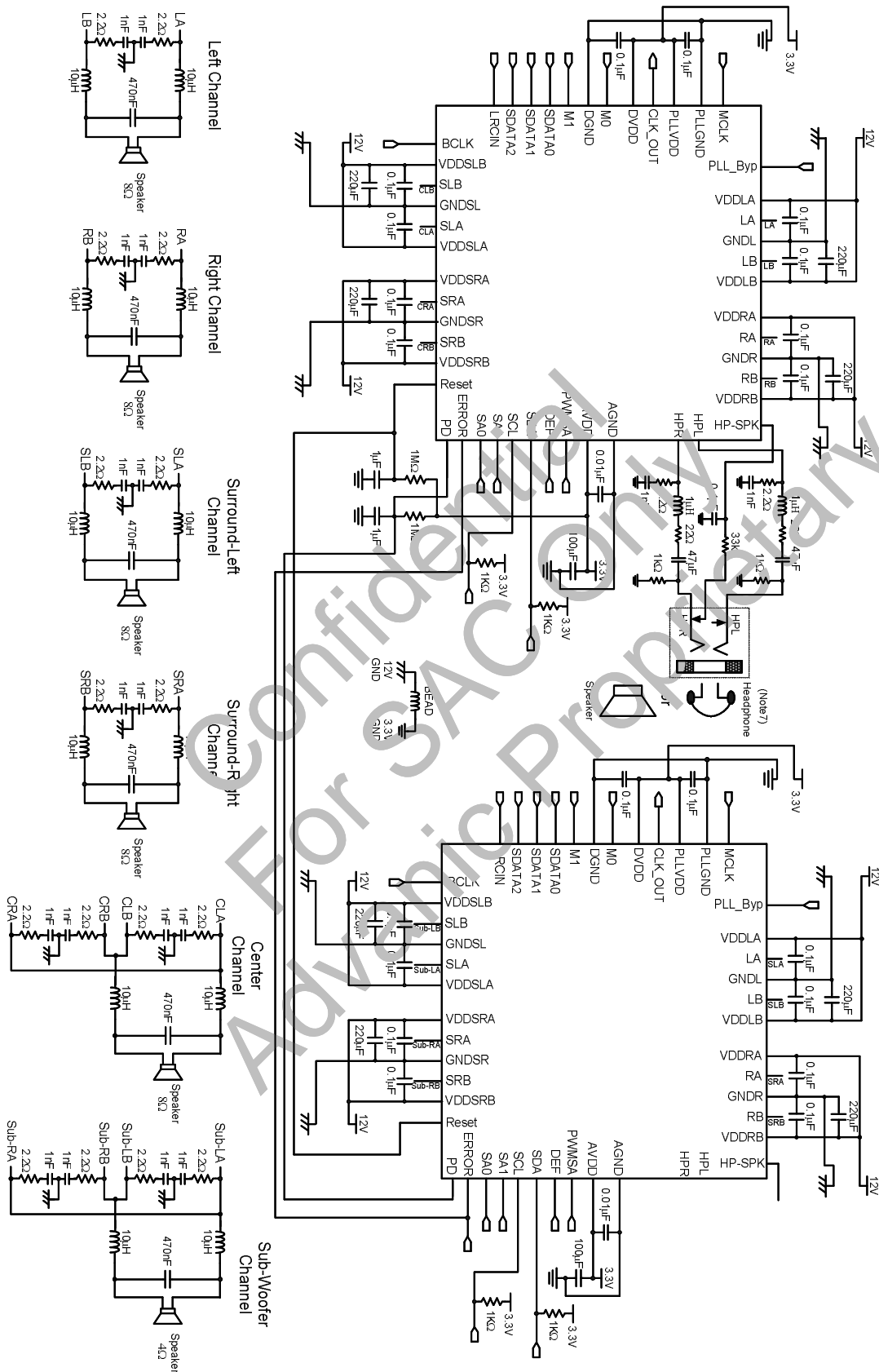
* This document contains information on a new product under development by Advanic. Advanic reserves the right to change or discontinue this product without notice.

Application Circuit Example (Stereo)



* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

Application Circuit Example (5.1-channel)



* This document contains information on a new product under development by Advanic. Advanic reserves the right to change or discontinue this product without notice.

Operation Description

I Operation modes

(i) Without I²C control

Default settings, such as: Bass, Treble, EQ, Volume, DRC, PLL, Subwoofer Bandwidth, ..., and Subwoofer Gain, are applied to register table content when using AD8356 without I²C control. For more information about default settings, please refer to the highlighted column of register table section.

(ii) With I²C control

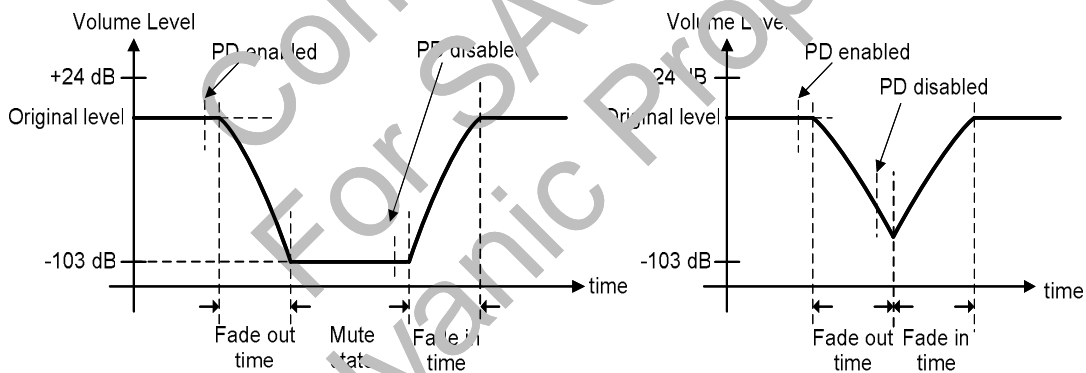
When using I²C control, default settings mentioned above will still be applied to the register table. Users can program more suitable parameters and specifications to AD8356 for their specific applications. Please refer to the I²C control in the next few pages.

I Reset

When the level of Reset pin is low, AD8356 will clear the data of internal storage elements and set the register table content to its default. AD8356 will exit reset state at the 256th MCLK cycles after $\overline{\text{Reset}}$ pin becomes high.

I Power down control

AD8356 has built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



AD8356 will detect PD pin once an LRCIN cycle. When AD8356 detects 9 consecutive zeros, it will execute a fade-out procedure. The volume level will be decreased to $-\infty$ dB in several LRCIN cycles. Once the fade-out procedure is finished, AD8356 will turn off the power stages, stop clock signals (MCLK, BCLK, LRCIN) from feeding into digital circuit and turn off the current of the internal analog circuits. After $\overline{\text{PD}}$ pin is pulled low, AD8356 needs up to 535 LRCIN clocks to finish the above works before entering power down state. Users can't program AD8356 during power down state, but all the settings of register table will still be kept except that DVDD is removed.

When AD8356 detect 9 consecutive ones from $\overline{\text{PD}}$ pin, the PD function will be disabled and a fade-in procedure is then executed. If the PD function is disabled in the midway of the fade-out procedure, AD8356 will also execute the fade-in procedure. AD8356 will return to the settings that before PD function

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

is enabled. In addition, AD8356 will establish the analog circuits' bias current and feed the clock signals (MCLK, BCLK, LRCIN) into digital circuits. Then, AD8356 will return to its normal operation without power down.

I Mode selection (M0, M1)

AD8356 supports stereo, 2.1 and 5.1-channel applications. For stereo, please set (M0,M1)=(0,0).

For 2.1-channel, please set (M0,M1)=(0,1). For 5.1-channel application, please use 2 pcs of AD8356, one with (M0,M1)=(1,0) and the other with (M0,M1)=(1,1).

I PLL bypass (PLL_Byp)

AD8356 has built-in PLL which can be bypassed by pulling PLL_Byp pin high. Except that external MCLK clock owns low enough jitter and duty cycle close to 50%, the use of the internal PLL is suggested.

I Default volume (DEF)

The default volume of AD8356 can be muted by selecting DEF pin low, while high for default volume setting. i.e., +8dB. When using AD8356 without I²C control interface, users should pull this pin high.

I Self-protection circuits

AD8356 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

- (i) If the internal junction temperature is higher than 150°C (over-temperature condition), loudspeaker and headphone power stages will be turned off and the temperature hysteresis for AD8356 to return to normal operation is about 30°C. The temperature value can have around 10% variation.
- (ii) To protect loudspeaker and headphone power stages when the lines connected to loudspeakers (or the lines connected to headphones) are shorted each other or to GND (short-circuit condition), circuits for the detection of output loading are built in AD8356. For normal operation, loudspeaker resistance larger than 6.8Ω for normal channels (3.4Ω for subwoofer channel) are required. Otherwise, the short-circuit detectors may pull the ERROR pin to DGND. When over-temperature or short-circuit condition occurs, the open-drain ERROR pin will be pulled low and the loudspeaker and headphone drivers will be turned-off and latched at ERROR state. Besides removing over-temperature or short-circuit condition, AD8356 won't leave ERROR state until one of the following conditions : (1) Reset pin is pulled low, (2) PD pin is pulled low, (3) Programming master mute via I²C interface. It is recommended that connecting ERROR pin to PD or Reset pin with external RC circuit of which time constant is larger than 1sec.
- (iii) Once the PLLVDD voltage is lower than 2.7V, AD8356 will turn off its loudspeaker and headphone power stages and cease the operation of digital processing circuits. When PLLVDD becomes larger than 2.8V, AD8356 will return to normal operation.

I Anti-pop design

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

AD8356 is with anti-pop design. Annoying pop sounds are suppressed during initial power on, power down/up, mute, power-off and volume level change. When one of the operations mentioned above is applied, AD8356 will internally generate appropriate control signals to suppress pop sounds.

I Loudspeakers and headphone switching

AD8356 can switch between headphone and loudspeaker modes automatically with the application circuits shown in the application circuit section. When HP-SPK pin is pulled high, AD8356 will enter headphone mode and loudspeaker output will be muted. HP-SPK pin is connected to DVDD via a 380k Ω (typical value) resistor in the chip.

I²C-Bus Transfer Protocol

I Introduction

AD8356 employs I²C-bus transfer protocol. Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock (SCL) on the bus. AD8356 is always a slave device in all of its communications.

I Protocol

n START and STOP Condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must be preceding any command for data transfer. A low to high transition on the SDA line while SCL is high defines a STOP condition. A STOP condition terminates communication between AD8356 and the master device on the bus.

n Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. AD8356 samples the SDA signal at rising edge of the clock signal SCL.

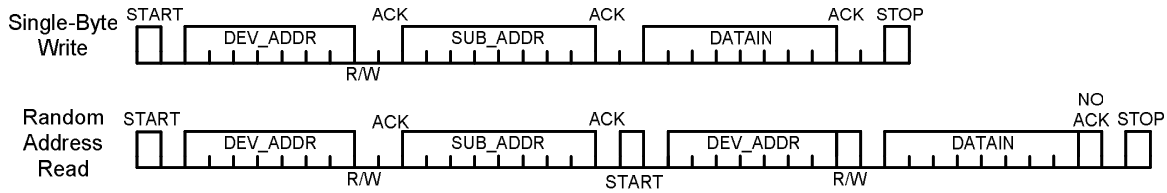
n Device Addressing

The master generates 7-bit address to recognize slave device. When AD8356 receives 7-bit address matched with 0110x0y (where x and y can be selected by external SA0 and SA1 pins, respectively), AD8356 will acknowledge at 9th bit time (8th bit time is for R/W bit). The bytes following the device identification address is for internal sub-address.

n Data Transferring

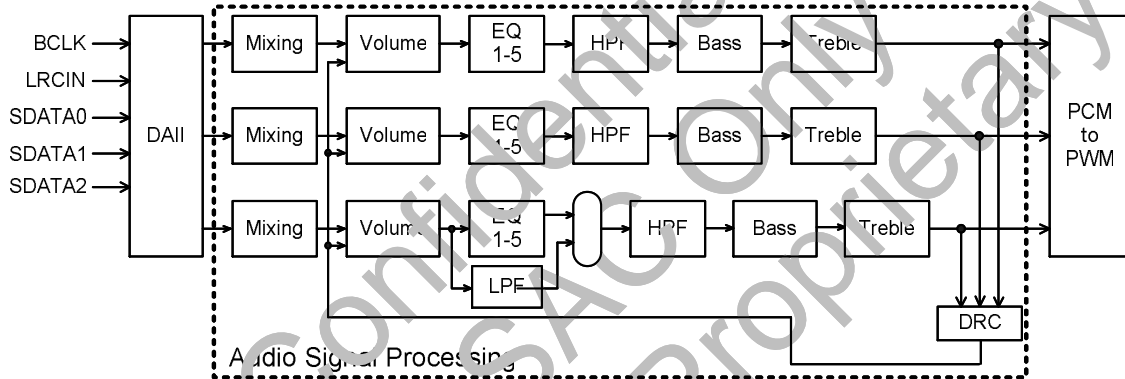
Every byte put on SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with MSB first. As the figure shown below, in both write and read operation, AD8356 supports single-byte. Please refer to the figure shown below for detail data-transferring protocol.

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.



Register Table

The audio signal processing data flow is shown as the following figure. Users can control these function by programming appropriate setting to register table. In this section, the total register table is shown. More detail information will be described in next section. Please note that we reserved the address 69,70 and 71. Never access or change the contents of these 3 addresses.



Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0	State Control 1	IF[2]	IF[1]	IF[0]	HFL	HFR	HFSW	CS	UVSEL
1	State Control 2	MF[1]	MF[0]	ADT	FS	PMF[3]	PMF[2]	PMF[1]	PMF[0]
2	State Control 3	EN_CLKO	HF	LF[1]	LF[0]	MUTE	CM1	CM2	CM3
3	Master Volume	X	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
4	Channel1 Volume	X	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
5	Channel2 Volume	X	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
6	Channel3 Volume	X	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
7	Bass and Treble Gain	TG[3]	TG[2]	TG[1]	TG[0]	BG[3]	BG[2]	BG[1]	BG[0]
8	CH1,CH2 Mixing to CH1	C1MX1[3]	C1MX1[2]	C1MX1[1]	C1MX1[0]	C1MX2[3]	C1MX2[2]	C1MX2[1]	C1MX2[0]
9	CH3,CH4 Mixing to CH1	C1MX3[3]	C1MX3[2]	C1MX3[1]	C1MX3[0]	C1MX4[3]	C1MX4[2]	C1MX4[1]	C1MX4[0]
10	CH5,CH6 Mixing to CH1	C1MX5[3]	C1MX5[2]	C1MX5[1]	C1MX5[0]	C1MX6[3]	C1MX6[2]	C1MX6[1]	C1MX6[0]
11	CH1,CH2 Mixing to CH2	C2MX1[3]	C2MX1[2]	C2MX1[1]	C2MX1[0]	C2MX2[3]	C2MX2[2]	C2MX2[1]	C2MX2[0]
12	CH3,CH4 Mixing to CH2	C2MX3[3]	C2MX3[2]	C2MX3[1]	C2MX3[0]	C2MX4[3]	C2MX4[2]	C2MX4[1]	C2MX4[0]

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

13	CH5,CH6 Mixing to CH2	C2MX5[3]	C2MX5[2]	C2MX5[1]	C2MX5[0]	C2MX6[3]	C2MX6[2]	C2MX6[1]	C2MX6[0]
14	CH1,CH2 Mixing to CH3	C3MX1[3]	C3MX1[2]	C3MX1[1]	C3MX1[0]	C3MX2[3]	C3MX2[2]	C3MX2[1]	C3MX2[0]
15	CH3,CH4 Mixing to CH3	C3MX3[3]	C3MX3[2]	C3MX3[1]	C3MX3[0]	C3MX4[3]	C3MX4[2]	C3MX4[1]	C3MX4[0]
16	CH5,CH6 Mixing to CH3	C3MX5[3]	C3MX5[2]	C3MX5[1]	C3MX5[0]	C3MX6[3]	C3MX6[2]	C3MX6[1]	C3MX6[0]
17	DRC parameter1	X	X	X	LMTEN	ATI[1]	ATI[0]	RTI[1]	RTI[0]
18	DRC parameter2	ATH12[1]	ATH12[0]	RTH12[1]	RTH12[0]	ATH3[1]	ATH3[0]	RTH3[1]	RTH3[0]
19	EQ1 A0 MSB	X	EQ1A0[14]	EQ1A0[13]	EQ1A0[12]	EQ1A0[11]	EQ1A0[10]	EQ1A0[9]	EQ1A0[8]
20	EQ1 A0 LSB	EQ1A0[7]	EQ1A0[6]	EQ1A0[5]	EQ1A0[4]	EQ1A0[3]	EQ1A0[2]	EQ1A0[1]	EQ1A0[0]
21	EQ1 A1 MSB	X	EQ1A1[14]	EQ1A1[13]	EQ1A1[12]	EQ1A1[11]	EQ1A1[10]	EQ1A1[9]	EQ1A1[8]
22	EQ1 A1 LSB	EQ1A1[7]	EQ1A1[6]	EQ1A1[5]	EQ1A1[4]	EQ1A1[3]	EQ1A1[2]	EQ1A1[1]	EQ1A1[0]
23	EQ1 A2 MSB	X	EQ1A2[14]	EQ1A2[13]	EQ1A2[12]	EQ1A2[11]	EQ1A2[10]	EQ1A2[9]	EQ1A2[8]
24	EQ1 A2 LSB	EQ1A2[7]	EQ1A2[6]	EQ1A2[5]	EQ1A2[4]	EQ1A2[3]	EQ1A2[2]	EQ1A2[1]	EQ1A2[0]
25	EQ1 B1 MSB	X	EQ1B1[14]	EQ1B1[13]	EQ1B1[12]	EQ1B1[11]	EQ1B1[10]	EQ1B1[9]	EQ1B1[8]
26	EQ1 B1 LSB	EQ1B1[7]	EQ1B1[6]	EQ1B1[5]	EQ1B1[4]	EQ1B1[3]	EQ1B1[2]	EQ1B1[1]	EQ1B1[0]
27	EQ1 B2 MSB	X	EQ1B2[14]	EQ1B2[13]	EQ1B2[12]	EQ1B2[11]	EQ1B2[10]	EQ1B2[9]	EQ1B2[8]
28	EQ1 B2 LSB	EQ1B2[7]	EQ1B2[6]	EQ1B2[5]	EQ1B2[4]	EQ1B2[3]	EQ1B2[2]	EQ1B2[1]	EQ1B2[0]
29	EQ2 A0 MSB	X	EQ2A0[14]	EQ2A0[13]	EQ2A0[12]	EQ2A0[11]	EQ2A0[10]	EQ2A0[9]	EQ2A0[8]
30	EQ2 A0 LSB	EQ2A0[7]	EQ2A0[6]	EQ2A0[5]	EQ2A0[4]	EQ2A0[3]	EQ2A0[2]	EQ2A0[1]	EQ2A0[0]
31	EQ2 A1 MSB	X	EQ2A1[14]	EQ2A1[13]	EQ2A1[12]	EQ2A1[11]	EQ2A1[10]	EQ2A1[9]	EQ2A1[8]
32	EQ2 A1 LSB	EQ2A1[7]	EQ2A1[6]	EQ2A1[5]	EQ2A1[4]	EQ2A1[3]	EQ2A1[2]	EQ2A1[1]	EQ2A1[0]
33	EQ2 A2 MSB	X	EQ2A2[14]	EQ2A2[13]	EQ2A2[12]	EQ2A2[11]	EQ2A2[10]	EQ2A2[9]	EQ2A2[8]
34	EQ2 A2 LSB	EQ2A2[7]	EQ2A2[6]	EQ2A2[5]	EQ2A2[4]	EQ2A2[3]	EQ2A2[2]	EQ2A2[1]	EQ2A2[0]
35	EQ2 B1 MSB	X	EQ2B1[14]	EQ2B1[13]	EQ2B1[12]	EQ2B1[11]	EQ2B1[10]	EQ2B1[9]	EQ2B1[8]
36	EQ2 B1 LSB	EQ2B1[7]	EQ2B1[6]	EQ2B1[5]	EQ2B1[4]	EQ2B1[3]	EQ2B1[2]	EQ2B1[1]	EQ2B1[0]
37	EQ2 B2 MSB	X	EQ2B2[14]	EQ2B2[13]	EQ2B2[12]	EQ2B2[11]	EQ2B2[10]	EQ2B2[9]	EQ2B2[8]
38	EQ2 B2 LSB	EQ2B2[7]	EQ2B2[6]	EQ2B2[5]	EQ2B2[4]	EQ2B2[3]	EQ2B2[2]	EQ2B2[1]	EQ2B2[0]
39	EQ3 A0 MSB	X	EQ3A0[14]	EQ3A0[13]	EQ3A0[12]	EQ3A0[11]	EQ3A0[10]	EQ3A0[9]	EQ3A0[8]
40	EQ3 A0 LSB	EQ3A0[7]	EQ3A0[6]	EQ3A0[5]	EQ3A0[4]	EQ3A0[3]	EQ3A0[2]	EQ3A0[1]	EQ3A0[0]
41	EQ3 A1 MSB	X	EQ3A1[14]	EQ3A1[13]	EQ3A1[12]	EQ3A1[11]	EQ3A1[10]	EQ3A1[9]	EQ3A1[8]
42	EQ3 A1 LSB	EQ3A1[7]	EQ3A1[6]	EQ3A1[5]	EQ3A1[4]	EQ3A1[3]	EQ3A1[2]	EQ3A1[1]	EQ3A1[0]
43	EQ3 A2 MSB	X	EQ3A2[14]	EQ3A2[13]	EQ3A2[12]	EQ3A2[11]	EQ3A2[10]	EQ3A2[9]	EQ3A2[8]
44	EQ3 A2 LSB	EQ3A2[7]	EQ3A2[6]	EQ3A2[5]	EQ3A2[4]	EQ3A2[3]	EQ3A2[2]	EQ3A2[1]	EQ3A2[0]
45	EQ3 B1 MSB	X	EQ3B1[14]	EQ3B1[13]	EQ3B1[12]	EQ3B1[11]	EQ3B1[10]	EQ3B1[9]	EQ3B1[8]
46	EQ3 B1 LSB	EQ3B1[7]	EQ3B1[6]	EQ3B1[5]	EQ3B1[4]	EQ3B1[3]	EQ3B1[2]	EQ3B1[1]	EQ3B1[0]
47	EQ3 B2 MSB	X	EQ3B2[14]	EQ3B2[13]	EQ3B2[12]	EQ3B2[11]	EQ3B2[10]	EQ3B2[9]	EQ3B2[8]
48	EQ3 B2 LSB	EQ3B2[7]	EQ3B2[6]	EQ3B2[5]	EQ3B2[4]	EQ3B2[3]	EQ3B2[2]	EQ3B2[1]	EQ3B2[0]

* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

49	EQ4 A0 MSB	X	EQ4A0[14]	EQ4A0[13]	EQ4A0[12]	EQ4A0[11]	EQ4A0[10]	EQ4A0[9]	EQ4A0[8]	
50	EQ4 A0 LSB		EQ4A0[7]	EQ4A0[6]	EQ4A0[5]	EQ4A0[4]	EQ4A0[3]	EQ4A0[2]	EQ4A0[1]	EQ4A0[0]
51	EQ4 A1 MSB	X	EQ4A1[14]	EQ4A1[13]	EQ4A1[12]	EQ4A1[11]	EQ4A1[10]	EQ4A1[9]	EQ4A1[8]	
52	EQ4 A1 LSB		EQ4A1[7]	EQ4A1[6]	EQ4A1[5]	EQ4A1[4]	EQ4A1[3]	EQ4A1[2]	EQ4A1[1]	EQ4A1[0]
53	EQ4 A2 MSB	X	EQ4A2[14]	EQ4A2[13]	EQ4A2[12]	EQ4A2[11]	EQ4A2[10]	EQ4A2[9]	EQ4A2[8]	
54	EQ4 A2 LSB		EQ4A2[7]	EQ4A2[6]	EQ4A2[5]	EQ4A2[4]	EQ4A2[3]	EQ4A2[2]	EQ4A2[1]	EQ4A2[0]
55	EQ4 B1 MSB	X	EQ4B1[14]	EQ4B1[13]	EQ4B1[12]	EQ4B1[11]	EQ4B1[10]	EQ4B1[9]	EQ4B1[8]	
56	EQ4 B1 LSB		EQ4B1[7]	EQ4B1[6]	EQ4B1[5]	EQ4B1[4]	EQ4B1[3]	EQ4B1[2]	EQ4B1[1]	EQ4B1[0]
57	EQ4 B2 MSB	X	EQ4B2[14]	EQ4B2[13]	EQ4B2[12]	EQ4B2[11]	EQ4B2[10]	EQ4B2[9]	EQ4B2[8]	
58	EQ4 B2 LSB		EQ4B2[7]	EQ4B2[6]	EQ4B2[5]	EQ4B2[4]	EQ4B2[3]	EQ4B2[2]	EQ4B2[1]	EQ4B2[0]
59	EQ5 A0 MSB	X	EQ5A0[14]	EQ5A0[13]	EQ5A0[12]	EQ5A0[11]	EQ5A0[10]	EQ5A0[9]	EQ5A0[8]	
60	EQ5 A0 LSB		EQ5A0[7]	EQ5A0[6]	EQ5A0[5]	EQ5A0[4]	EQ5A0[3]	EQ5A0[2]	EQ5A0[1]	EQ5A0[0]
61	EQ5 A1 MSB	X	EQ5A1[14]	EQ5A1[13]	EQ5A1[12]	EQ5A1[11]	EQ5A1[10]	EQ5A1[9]	EQ5A1[8]	
62	EQ5 A1 LSB		EQ5A1[7]	EQ5A1[6]	EQ5A1[5]	EQ5A1[4]	EQ5A1[3]	EQ5A1[2]	EQ5A1[1]	EQ5A1[0]
63	EQ5 A2 MSB	X	EQ5A2[14]	EQ5A2[13]	EQ5A2[12]	EQ5A2[11]	EQ5A2[10]	EQ5A2[9]	EQ5A2[8]	
64	EQ5 A2 LSB		EQ5A2[7]	EQ5A2[6]	EQ5A2[5]	EQ5A2[4]	EQ5A2[3]	EQ5A2[2]	EQ5A2[1]	EQ5A2[0]
65	EQ5 B1 MSB	X	EQ5B1[14]	EQ5B1[13]	EQ5B1[12]	EQ5B1[11]	EQ5B1[10]	EQ5B1[9]	EQ5B1[8]	
66	EQ5 B1 LSB		EQ5B1[7]	EQ5B1[6]	EQ5B1[5]	EQ5B1[4]	EQ5B1[3]	EQ5B1[2]	EQ5B1[1]	EQ5B1[0]
67	EQ5 B2 MSB	X	EQ5B2[14]	EQ5B2[13]	EQ5B2[12]	EQ5B2[11]	EQ5B2[10]	EQ5B2[9]	EQ5B2[8]	
68	EQ5 B2 LSB		EQ5B2[7]	EQ5B2[6]	EQ5B2[5]	EQ5B2[4]	EQ5B2[3]	EQ5B2[2]	EQ5B2[1]	EQ5B2[0]

Detail Description for Register

In this section, please note that the highlighted columns are the default value of these tables.

I Address 0 : State Control 1

AD8356 support multiple serial data input formats including I²S, Left-alignment and Right-alignment.

These formats is chosen by user via bit7~bit5 of address 0. Also, the controller of AD8356 provides both full-bridge and half-bridge PWM signals to power stages, and bit4, 3 and 2 is used respectively for left, right and sub-woofer channel programming these feature. The power stage only supports full-bridge configuration in AD8356. If half-bridge configuration is required, please refer to Advanic's AD8350 product.

Bit1 of this address is center and sub-woofer selection. If we assign 0, the audio signal processing for the 3rd channel will pass low-pass filter for narrow-band sub-woofer application, otherwise the 3rd channel will pass treble filter and EQ1~5, acts as normal channel like left and right channel.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I ² S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits

* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
B[4]	HFL	Left Half/Full Bridge Selection	0	Full
			1	Half
B[3]	HFR	Right Half/Full Bridge Selection	0	Full
			1	Half
B[2]	HFSW	Subwoofer Half/Full Bridge Selection	0	Full
			1	Half
B[1]	CS	Center/SubWoofer Selection	0	Sub-Woofer
			1	Center
B[0]	UVSEL	Under-voltage selection	0	2.7V
			1	2.2V

I Address 1 : State Control 2

AD8356 has built-in PLL which can be bypassed by pull low the PLL_Byr pin. When PLL is bypassed, AD8356 supports auto-detection (bit5 = 1) for 256x, 384x and 576x MCLK/Fs ratio, or you can select these 3 kinds of ratio by bit7 and bit6 (bit5 = 0). When PLL is enabled, multiple MCLK/FS ratios is supported. Detail setting is shown as the above table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MF[1:0]	MCLK/Fs setup when PLL is bypassed	00	256x
			01	256x
			10	384x
			11	576x
B[5]	ADT	Auto-detection when PLL is bypassed	0	Using MF[1:0] settings
			1	auto-detection
B[4]	FS	Sampling Frequency	0	32/44.1/48kHz
			1	64/88.2/96kHz
B[3:0]	PMF[3:0]	MCLK/Fs setup when PLL is not bypassed	0000	Reset Default
			0001	64x
			0010	128x
			0011	192x
			0100	256x
			0101	384x
			0110	512x
			0111	576x
			1000	768x

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

I Address 2 : State Control 3

To prevent DC component from damaging the speaker, high pass filter (3dB frequency = 10Hz) is built in AD8356, which can be enabled or disabled by bit6 of address 2. Sub-woofer channel employs low-pass filter to create narrow-band audio processing channel.

AD8356 has mute function including master mute and channel mute. When master mute is enabled, all 3 processing channels are muted. User can mute these 3 channels individually by channel mute. Surely, for anti-pop consideration, fade-out when mute is enabled and fade-in when mute is disabled is provided.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	EN_CLK_OUT	PLL Clock Output	0	Disabled
			1	Enabled
B[6]	HF	High-Pass Filter	0	5Hz
			1	Disabled
B[5:4]	LF[1:0]	Low-Pass Filter	00	150Hz
			01	200Hz
			10	250Hz
			11	Disable
B[3]	MUTE	Master Mute	0	Un-Mute
			1	Mute
B[2]	CM1	Channel 1 Mute	0	Un-Mute
			1	Mute
B[1]	CM2	Channel 2 Mute	0	Un-Mute
			1	Mute
B[0]	CM3	Channel 3 Mute	0	Un-Mute
			1	Mute

I Address 3 : Master Volume

AD8356 supports both master-volume and channel-volume control for the 2.1 processing channels. Both master volume control (Address 3) and channel volume (Address 4, 5 and 6) settings range from +12dB ~ -103dB. Given master volume level, say, Level A (in dB unit) and channel volume level, say Level B (in dB unit), the total volume equals to Level A plus with Level B and its range is from +24dB ~ -103dB, i.e., $-103\text{dB} \leq \text{Total Volume (Level A + Level B)} \leq +24\text{dB}$.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	MV[6:0]	Master Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0000100	+8dB

			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110011	-103dB
			1110100	$-\infty$ dB
			:	:
			1111111	$-\infty$ dB

I Address 4 : Channel1 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	C1V[6:0]	Channel 1 Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110011	-103dB
			1110100	$-\infty$ dB
			:	:
			1111111	$-\infty$ dB

I Address 5 : Channel2 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	C2V[6:0]	Channel 2 Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110011	-103dB
			1110100	$-\infty$ dB
			:	:
			1111111	$-\infty$ dB

* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

I Address 6 : Channel3 Volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	C3V[6:0]	Channel 3 Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110011	-103dB
			1110100	-∞dB
			:	:
			1111111	-∞dB

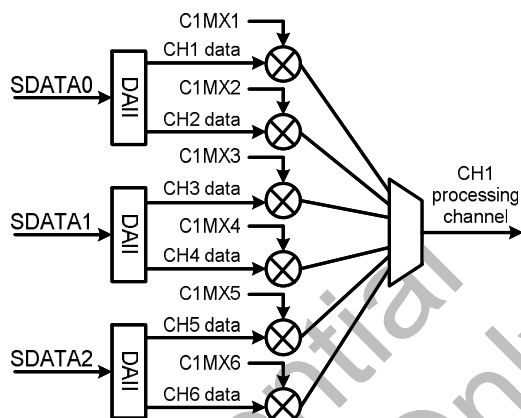
I Address 7 : Bass and Treble Gain Control

Gain control for treble filter (3dB frequency is 7kHz) and bass filter (3dB frequency is 250Hz) is selected by bit7~bit4 and bit3~bit0 of address 7, respectively. Treble filter is used for boost or cut the high-frequency sound effect, while bass filter is for low-frequency sound effect. The following figure shows the frequency response of treble and bass filter ranging from +18dB to -12dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	TG[3:0]	Treble Gain Control	1111	+18dB
			1110	+16dB
			1101	+14dB
			:	:
			0110	0dB
			:	:
			0001	-10dB
			0000	-12dB
B[3:0]	BG[3:0]	Bass Gain Control	1111	+18dB
			1110	+16dB
			1101	+14dB
			:	:
			0110	0dB
			:	:
			0001	-10dB
			0000	-12dB

I Address 8~10, 11~13 and 14~16 : CH1~6 Mixing Scale to CH1,CH2 and CH3

As the following diagram about mixing function of AD8356, there are three serial SDATA input, where SDATA0 can be decoded and we will get CH1,2 audio data. With the same principle, SDATA1 can get CH3,4 and SDATA2 can get CH5,6. Channel 1~6 audio data which we just get from SDATA0, 1 and 2 will be multiplied by a mixing scale C1MX1~C1MX6. After adding these 6 products, we'll get CH1 processing channel. It is similar for CH2 and CH3 processing channels.



Address 8

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	C1MX1[3:0]	Mixing Scale for Channel1 Mixing to Channel1	0000	0/15
			0001	1/15
			:	:
			:	:
			1110	14/15
			1111	15/15
B[3:0]	C1MX2[3:0]	Mixing Scale for Channel2 Mixing to Channel1	0000	0/15
			0001	1/15
			:	:
			:	:
			1110	14/15
			1111	15/15

Address 9

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	C1MX3[3:0]	Mixing Scale for Channel3 Mixing to Channel1	0000	0/15
			0001	1/15
			:	:
			:	:

* This document contains information on a new product under development by Advanic. Advanic reserves the right to change or discontinue this product without notice.

			1110	14/15
			1111	15/15
B[3:0]	C1MX4[3:0]	Mixing Scale for Channel4 Mixing to Channel1	0000	0/15
			0001	1/15
			:	:
			:	:
			1110	14/15
			1111	15/15

Address 10

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	C1MX5[3:0]	Mixing Scale for Channel5 Mixing to Channel1	0000	0/15
			0001	1/15
			:	:
			:	:
			1110	14/15
			1111	15/15
B[3:0]	C1MX6[3:0]	Mixing Scale for Channel6 Mixing to Channel1	0000	0/15
			0001	1/15
			:	:
			:	:
			1110	14/15
			1111	15/15

From the table shown above, addresses 8,9 and 10 represent CH1, CH2, CH3, CH4, CH5 and CH6 mixing scale to CH1, respectively. Addresses 11~13 and 14~16 are the same as address 8~10 except that addresses 11~13 are for CH2 and addresses 14~16 are for CH3.

The default settings of address 8~13 are $F_{0(h)}$, $0_{0(h)}$, $0_{0(h)}$, $0F_{(h)}$, $0_{0(h)}$ and $0_{0(h)}$, respectively. The default setting of address 14~16, i.e., C3MX1~C3MX6, are determined by M0 and M1. Please refer to the table shown below for detail information.

M0	M1	Configuration	C3MX1	C3MX2	C3MX3	C3MX4	C3MX5	C3MX6	Note
0	0	Stereo	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	
0	1	2.1-channel	$7_{(h)}$	$7_{(h)}$	$7_{(h)}$	$7_{(h)}$	$7_{(h)}$	$7_{(h)}$	
1	0	5.1(L)	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$F_{(h)}$	$0_{(h)}$	Subwoofer at L
1	1	5.1(R)	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$0_{(h)}$	$F_{(h)}$	Subwoofer at R

* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

I Address 17 : DRC (Dynamic Range Control) Parameter 1

AD8356 has two dynamic range control functions, RMS limiter and noise gate mute. Channel 1 & 2 use the same RMS limiter setting and channel 3 uses the other. For example, if we set ATH12 = "11", RTH12 = "10". When AD8356 detects signal RMS of channel 1 exceeding preset attack threshold (ATH12[1:0] = "11", the attack threshold equals 0.25), it will decrease the gain of channel 1 with the speed of attack rate until RMS of channel 1 is below 0.25. When AD8356 detects signal RMS of channel 1 is below release threshold (RTH12[1:0] = "10", the release threshold equals 0.125), it will increase the gain of channel 1 with the speed of release rate until RMS of channel 1 reaches release threshold (or DRC feedback gain reaches 0 dB). When RMS limiter is disabled, DRC feedback gain is 0dB. Channel 1, 2, 3 use the same noise gate setting. When AD8356 detects continue 1024 data (after mixing, volume, Bass, Treble, EQ, high pass or low pass) below noise gate threshold, it will mute corresponding channel. Noise gate mute status will be disable only when AD8356 detects 1 sample above noise gate threshold or disable this function.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4]	LMTEN	Attack/Release Limit	0	Disabled
		Enable/Disable	1	Enabled
B[3:2]	ATI[1:0]	Attack Time	00	0.75dB/ms
			01	0.1875dB/ms
			10	0.0469dB/ms
			11	0.0117dB/ms
B[1:0]	RTI[1:0]	Release Time	00	0.0117dB/ms
			01	0.0059dB/ms
			10	0.0029dB/ms
			11	0.0015dB/ms

I Address 18 : DRC (Dynamic Range Control) Parameter 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	ATH12 [1:0]	Attack Threshold for Channel 1, 2	00	1/2 signal power
			01	1/4 signal power
			10	1/8 signal power
			11	1/16 signal power
B[5:4]	RTH12 [1:0]	Release Threshold for Channel 1, 2	00	Attack Threshold
			01	1/2 Attack Threshold
			10	1/4 Attack Threshold
			11	1/8 Attack Threshold

* This document contains information on a new product under development by Advanic.
Advanic reserves the right to change or discontinue this product without notice.

B[3:2]	ATH3[1:0]	Attack Threshold for Channel 3	00	1/2 signal power
			01	1/4 signal power
			10	1/8 signal power
			11	1/16 signal power
B[1:0]	RTH3[1:0]	Release Threshold for Channel 3	00	Attack Threshold
			01	1/2 Attack Threshold
			10	1/4 Attack Threshold
			11	1/8 Attack Threshold

I Address 19~28 : EQ1 coefficient

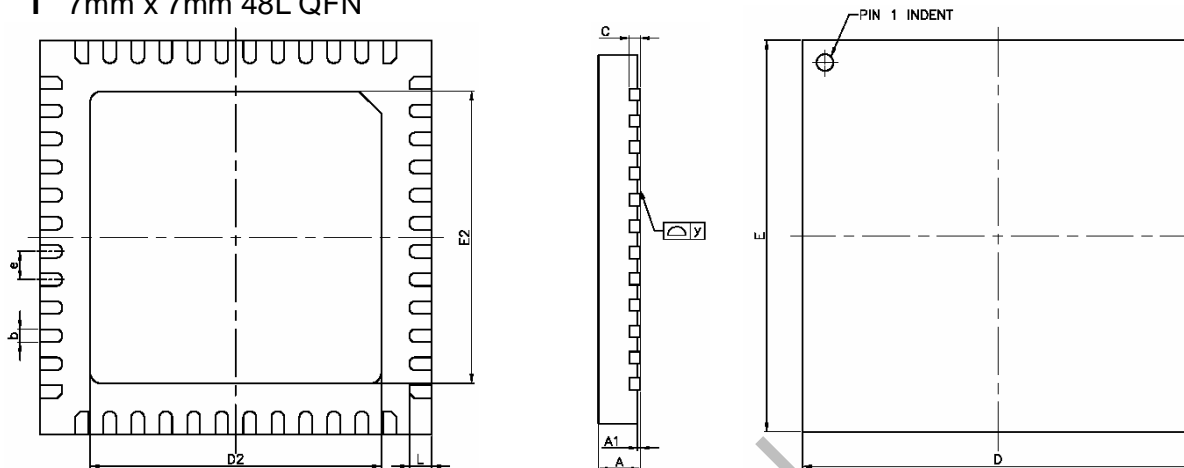
AD8356 has built-in 5-bands parametric EQ. For each EQ, Users can program its coefficient via I²C interface to determine its frequency response. The transfer function of EQ is:

$$H(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2}}{1 - b_1z^{-1} - b_2z^{-2}}$$

The bit6~bit0 of address 19 and bit7~bit0 of address 20 are combined and used to represent the 15 bits coefficient a0 of EQ1. The data format of binary code for EQ coefficient is 4.11. i.e., 4-bits for integer (MSB is sign bit) and 11-bits for mantissa. For example, if coefficient a0 of EQ1 is "2.875" in decimal, it will be represented as "0010_1110000000" in binary. User should program "X0010111" (X stands for don't care) for address 19 and "00000000" for address 20. Address 21、22、23、24、25、26 and 27、28 is for a1, a2, b1 and b2 of EQ1, respectively. The coefficient for both EQ2~5 are following this rule. To avoid unexpected sound, It is strongly recommended that to use multi-write protocol to program a set of EQ's coefficient in the same data transferring.

Package Dimensions

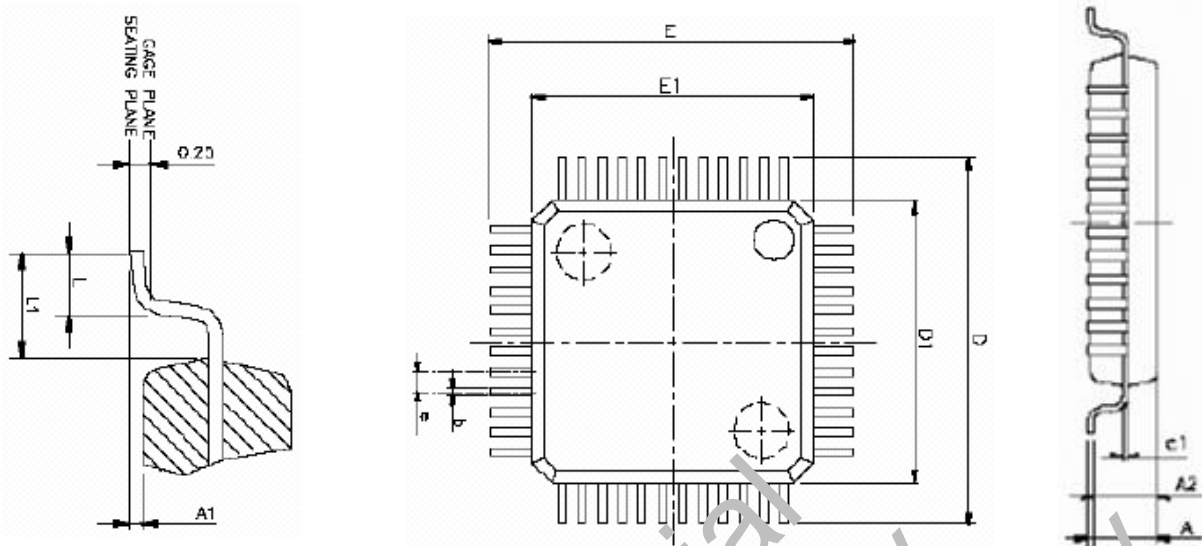
I 7mm x 7mm 48L QFN



Symbols	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
C	---	0.20 REF.	---
D	6.90	7.00	7.10
D2	5.05	5.20	5.35
E	6.90	7.00	7.10
E2	5.05	5.20	5.35
e	---	0.50	---
L	0.30	0.40	0.50
y	0.00	---	0.076

* This document contains information on a new product under development by Avanic.
Avanic reserves the right to change or discontinue this product without notice.

I 7mm x 7mm 48L LQFP



Symbols	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.50 BSC		
c1	0.09		0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.

Revision History

Version	Date	Revision Summary	Remark
0.1	2004/7/29		First Version
0.2	2004/9/4	1. Remove H/W control mode 2. Modification on DRC spec. 3. Mixing, volume, EQ, Bass, Treble, LPF, HPF and state control description are added 4. I ² C multi-byte read NOACK -> ACK 5. Mixing scale 1111 for 0/15 -> 0000 for 0/15 and 1111 for 15/15 6. Auto-HBOFF when no MCLK	
0.3	2005/1/5	Simplified version datasheet for enough application information	
0.4	2005/2/1	Full-version datasheet	

Confidential
For SAC Only
Advanic Proprietary

ADDRESS

Advanic Technologies, Inc.
 4F, No.159, Sec. 2, Minchiuan Rd.,
 Tainan City 700
 Taiwan
 台灣台南市中區民權路二段 159 號 4F

Tel: 886-6-2255786

Fax: 886-6-2276351

<http://advanic.com.tw/>

* This document contains information on a new product under development by Advanic.
 Advanic reserves the right to change or discontinue this product without notice.