



Digital Tuned FM Stereo Radio
LV24000 / LV24001 / LV24002

DATA SHEET

DS2400S02

PRELIMINARY

REVISION HISTORY**V0.0** 17-March-2004

- Initial version

V0.1 25-March-2004

- Modified after reviewing with project group
- Add timing diagrams and counter 2 sequence
- Add VQLP40 packaging dimensions
- Adjust Supply voltage

V0.2 02-May-2004

- TSSOP24 (225 mil) packaging dimension added
- Read diagram added
- Register definitions changed:
 - Register 100h - chip ID definitions changed:
 - 04: LV24002
 - 05: LV24000/LV24001
 - Register 102h - MSR_O bit is moved from bit 7 to bit 4
 - Register 106h - SWP_CNT bit becomes SWP_CNT_L (active low)
 - Register 108h - IRQ_LVL bit is inverted (1: active low - 0: active high)
 - Register 202h - DIR_AFC bit: description changed
 - Register 206h - IF_PM becomes IF_PM_L (active low)
 - Register 207h - AMUTE becomes AMUTE_L (active low)
 - Register 207h - CTRLB becomes TB_ON (Treble/Bass on)
 - Register 208h - FILTSW bit becomes AUTOSSR
 - Register 209h - Tone (bit [7:4]) and volume (bit [3:0]) levels are inverted
 - Register 20Ah - Beep frequencies (bit [7:6]) are reversed
 - Register 20Ah - BASS_L becomes BASS_PP
 - Register 20Bh - Soft audio mute moved from bit [7:5] to bit [4:2]. 8 control levels
 - Register 20Bh - Soft stereo moved from bit [4:2] to bit [7:5]. 8 control levels
- Register 208h - ST_M bit is inverted (1: mono - 0: stereo)Applied DIR_AFC bit level to "Using the digital automatic frequency control"
- Divider factor of counter 2 changed from 16 to 2
- Volume, tone, treble, bass handling added
- Soldering chapter is removed
- Write/Read timing changed

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OVERVIEW

The LV2400x¹ family are single chip tuner IC's targeted for portable applications where space and power consumption are of utmost importance. Due to a unique design no external components are required. When the newly developed VQLP40 package is used the complete FM radio design consumes only 25 mm² in the application. Integration of additional features like a Source Selector with master volume control and audible feedback function (LV24001) and on top of that a Bridge Tight Load Headphone Amplifier with Bass Boost function (LV24002) makes this IC the most compact and versatile tuner IC for portable applications.

Features LV24000

- No external components
- No alignments necessary
- Complete adjustment free stereo decoder - no external crystal required
- Fully integrated MPX VCO circuit
- Fully integrated low IF selectivity and demodulation
- No external FM discriminator needed due to full integration
- Built in adjacent channel interference total reduction (no 114kHz, no 190kHz)
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- RF Automatic Gain Control (AGC) circuit
- Very low power Standby mode. No power switch circuitry required
- MPX output for RDS application
- 3-wire low voltage digital bus to communicate with host
- Digital AFC - Tuner locks to frequency after tuning sequence
- 20 step (-60dB) master volume control
- 8 levels programmable Soft Mute
- 8 levels programmable Soft Stereo
- In combination with the host, fast, low power operation of preset mode, manual search, automatic search with programmable antenna level and automatic preset store are possible
- Low voltage operation. Digital interface runs at min 1.5V
- Automatic standby mode at power on. No initialization required until using radio function
- Covers all Japanese, European and US bands

Additional Features LV24001

- Source selector with stereo line-in for glue less integration into any audio application
- Audible feedback feature for glue less generation of audio sequences to confirm user interaction

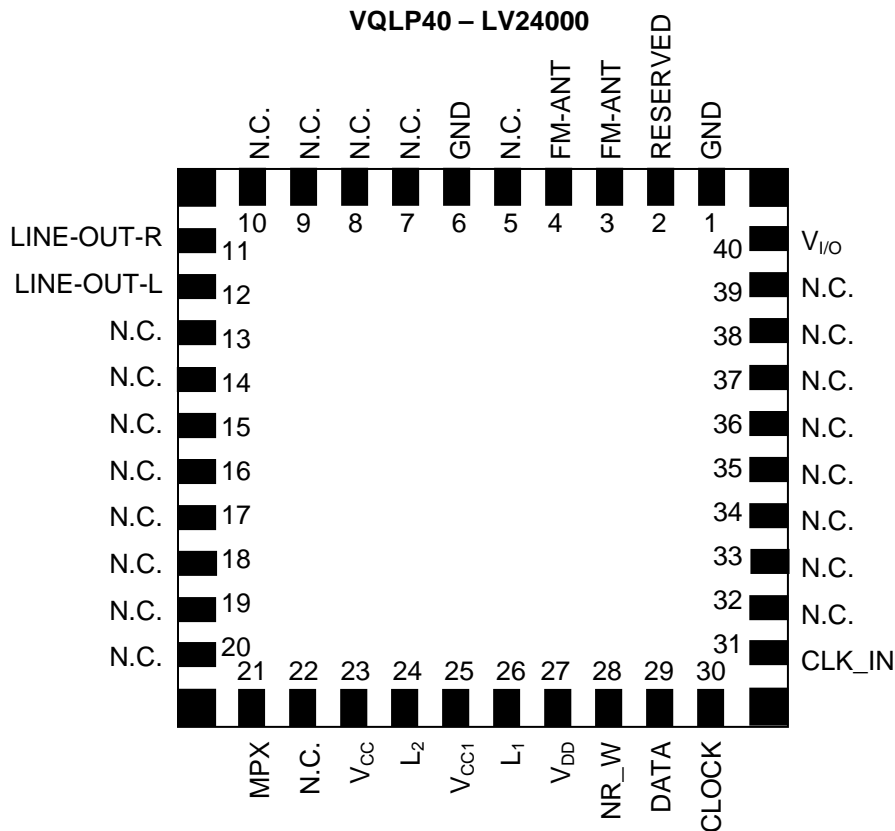
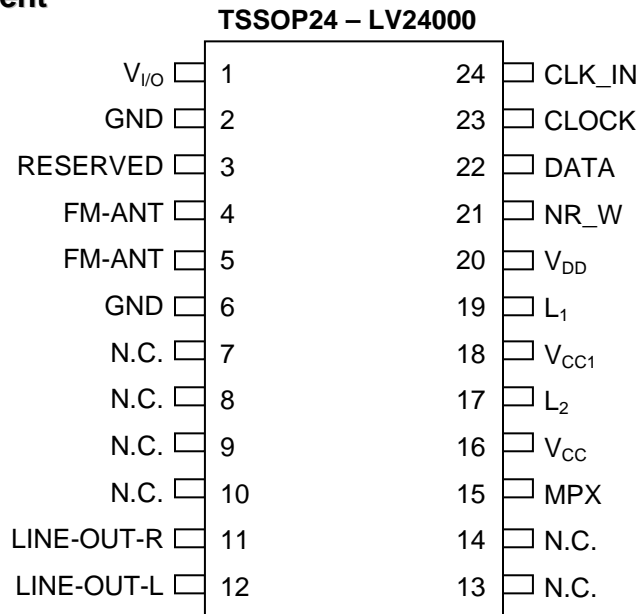
Additional Features LV24002

- Bridge Tight Load Headphone amplifier – highly power efficient, one component FM radio add-on to any application with a micro controller
- Bass enhancement control

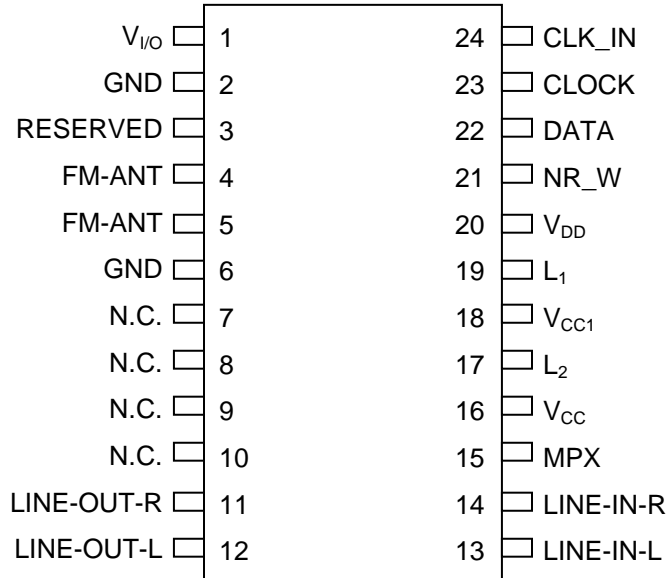
¹ The name "LV2400x" indicates the products LV24000, LV24001 and LV24002.

Chip layout

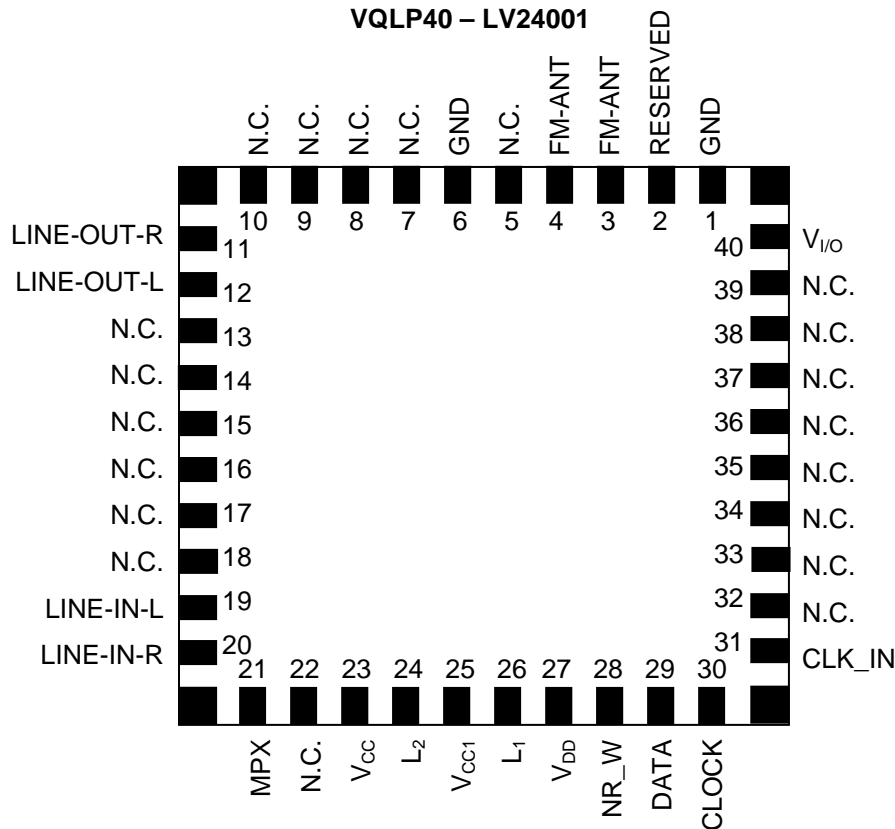
Pin assignment



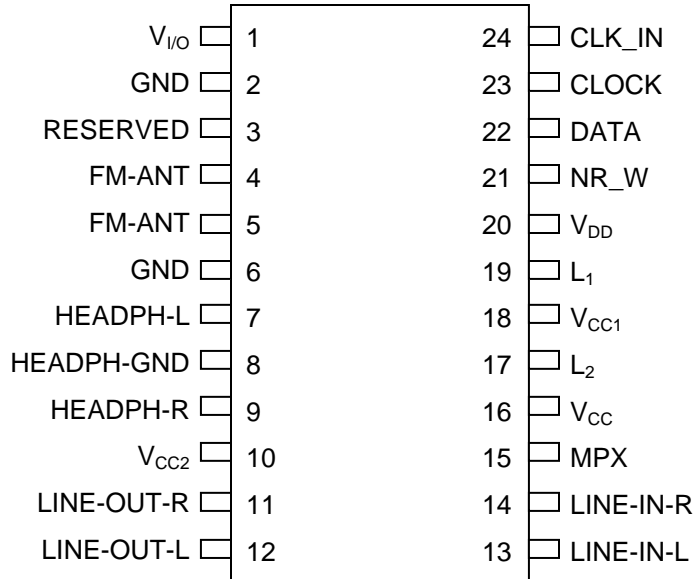
TSSOP24 – LV24001



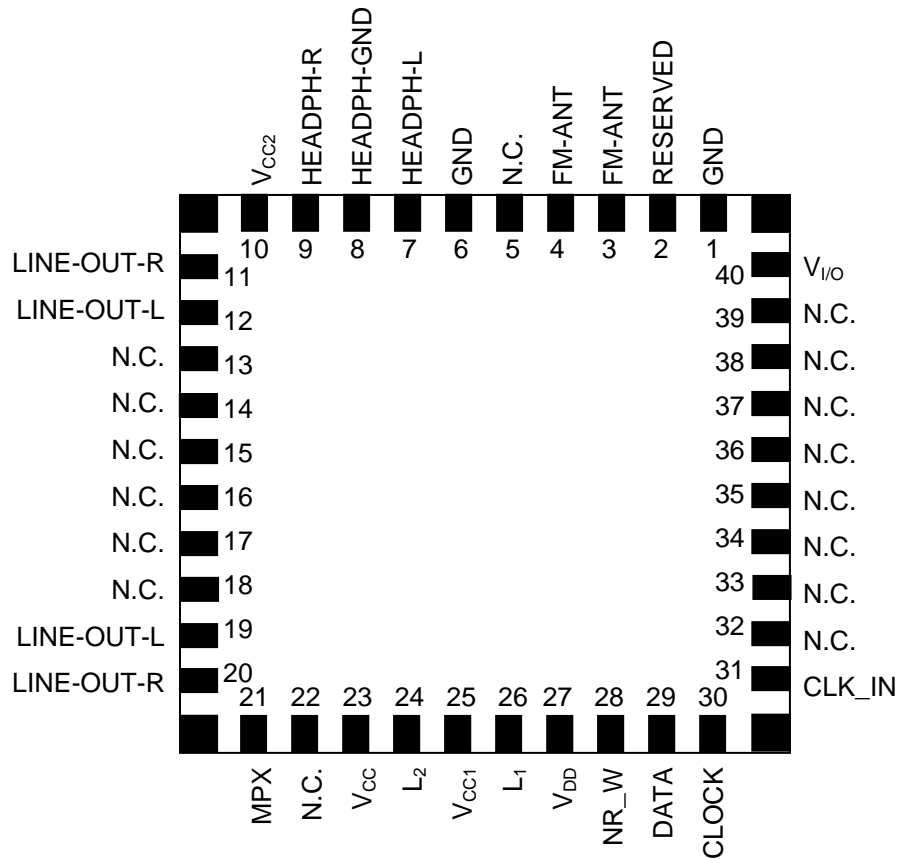
VQLP40 – LV24001



TSSOP24 – LV24002

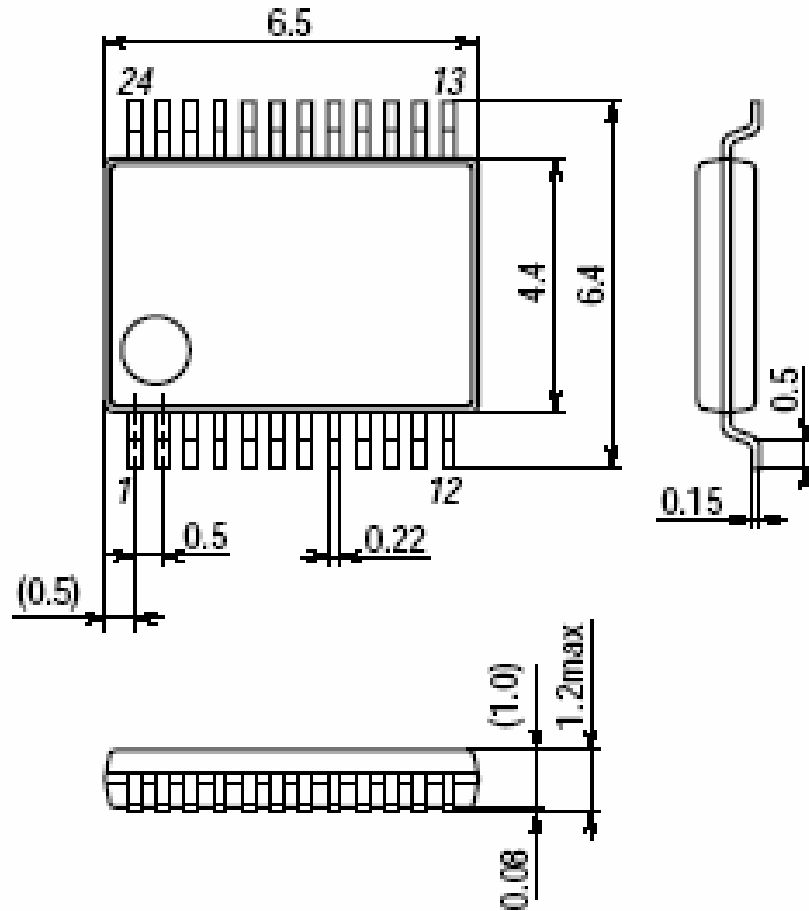


VQLP40 – LV24002

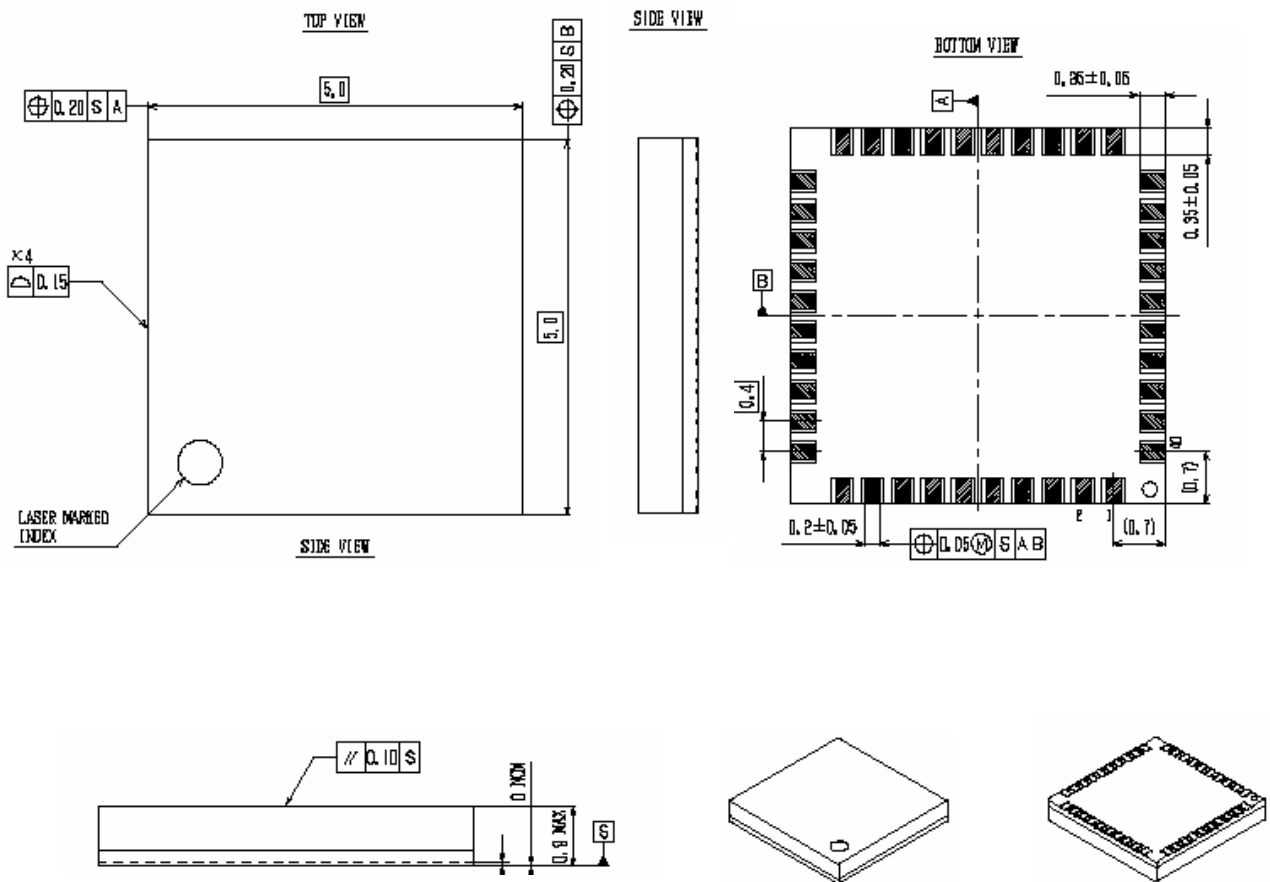


Pin Description

Name	I/O	Function description	Remark
V _{CC}		Analogue circuitry voltage	
V _{CC2}		Headphone amplifier voltage	Only LV24002
V _{DD}		Digital circuitry voltage	
V _{I/O}		Digital interface voltage	
GND		Ground	
FM-ANT	I	FM radio antenna input	
LINE-OUT-L	O	Radio Line-out (Left)	
LINE-OUT-R	O	Radio Line-out (Right)	
LINE-IN-L	I	Line-in (Left)	LV24001 and LV24002
LINE-IN-R	I	Line-in (Right)	LV24001 and LV24002
HEADPH-L	O	Headphone (Left)	Only LV24002
HEADPH-R	O	Headphone (Right)	Only LV24002
HEADPH-GND		Headphone Ground	Only LV24002
MPX	O	MPX-signal	
CLK_IN	I	Reference clock-source input for measurement (will be divided with 16)	Usage is optional. Connect to ground if not used.
V _{CC1} , L1, L2		PCB-coils	Only TSSOP24
RESERVED	-	Reserved (do not connect)	
CLOCK	I	Digital-interface Clock	
DATA	I/O	Digital-interface Data	
NR_W	I	Digital-interface Read/Write	

Packaging dimensions**TSSOP24 (225 mil)**

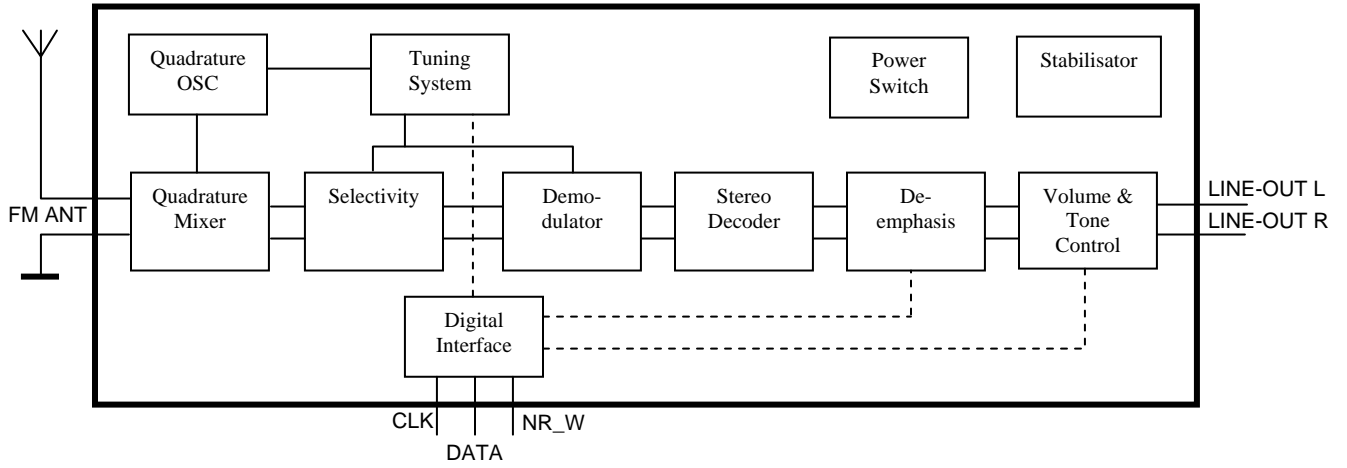
VQLP40



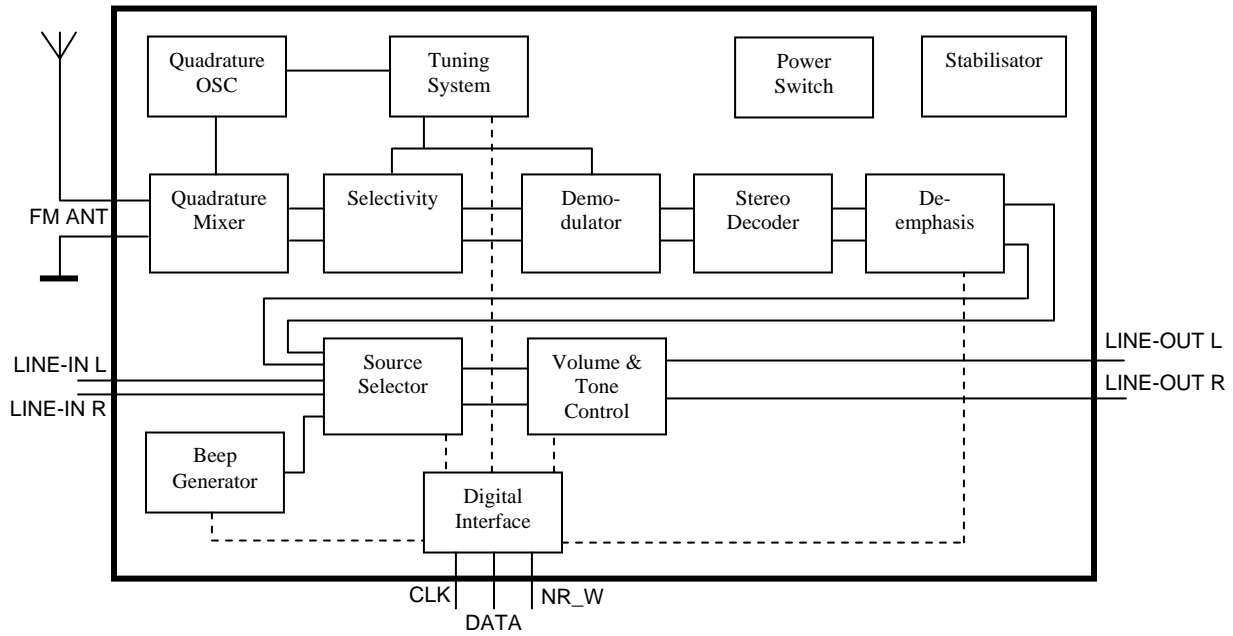
VQLP40 (5, 035, 0) X01

Block Diagram

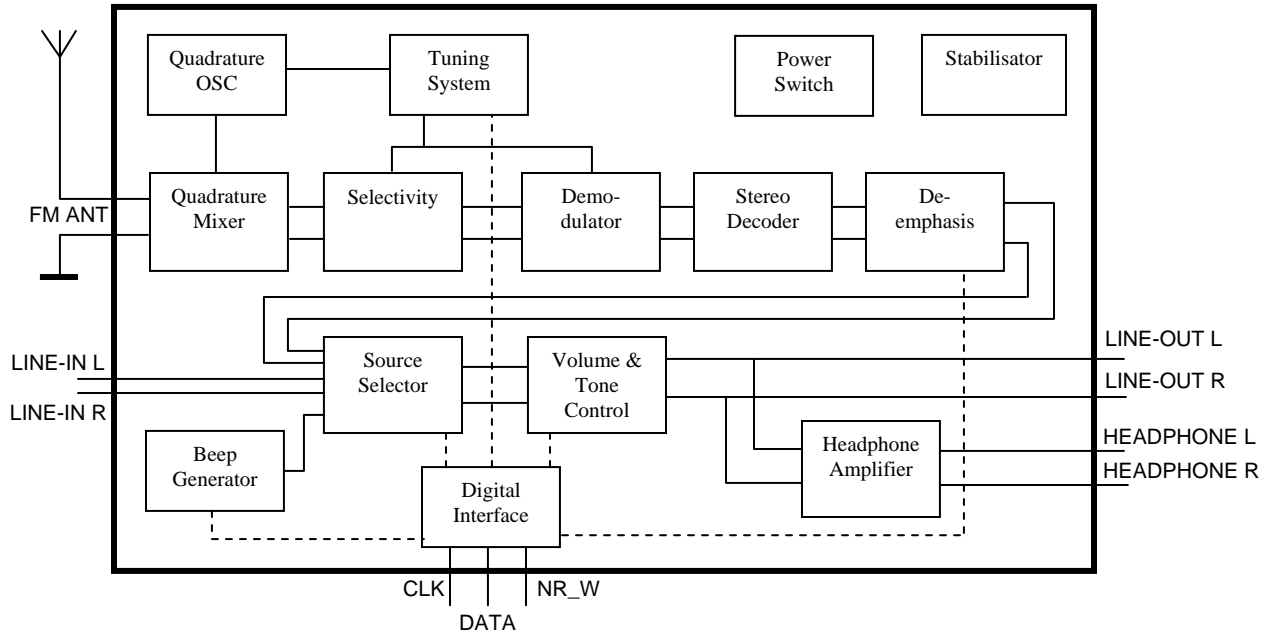
LV24000



LV24001



LV24002



AC/DC parameters

Absolute maximum ratings / Ta=25°C, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
V _{DD}	Digital interface voltage		-0.3	-	5	V
V _{CC} , V _{CC2}	Analogue voltage		-0.3	-	8	V
T _{stg}	storage temperature		-55	-	150	C
T _{amb}	ambient temperature	V _{CCA} =V _{CC(VCO)} =V _{CCD} =3V	-20	-	75	C
V _{es}	electrostatic handling for all pins	Machine model (R=10Ω, C=200pF, 75μH)	-200	-	200	V
		Human body model (R=1.5kΩ, C=100pF)	-2000	-	2000	V

Digital Input AC Values

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
Digital inputs						
V _{IH}	HIGH level input voltage		1.4	-	-	V
V _{IL}	LOW level input voltage		-	-	0.6	V
Digital outputs						
I _{OL}	LOW level output current		-	-	2	mA
V _{OL}	LOW level output voltage	I _{OL} = 2 mA	-	-	0.6	V
Timing						
f _{clk}	clock input		-	-	1	MHz
t _{HIGH}	clock HIGH time		495	-	-	ns
t _{LOW}	clock LOW time		495	-	-	ns
f _{FM(ant)}	FM input frequency		76	-	108	MHz
T _{amb}	ambient temperature	V _{CCA} =V _{CC(VCO)} =V _{CCD} =3V	-20	-	75	C
		V _{CCA} =V _{CC(VCO)} =V _{CCD} =5V	-40	-	85	C

Recommended operating range / Ta=-20°C to +70°C, GND = 0V

Symbol	Parameter	Pins	Conditions	Limits			
				Min	typ	max	unit
V _{CC}	Analogue supply voltage	V _{CC}		2.7	3.3	5.0	V
V _{CC2}	Analogue headphone amplifier supply voltage	V _{CC2}		2.7	3.3	5.0	V
V _{DD}	Digital supply voltage	V _{DD}		2.5	3.3	5.0	V
V _{I/O}	Interface voltage	V _{I/O}		1.6	3.0	5.0	V
I _{CC}	Analogue supply current	V _{CC}		-	19	21	mA
			Standby	-	1	-	μA
I _{CC2}	Analogue headphone amplifier current	V _{CC2}		-	4	5	mA
I _{DD}	Digital supply current	V _{DD}		3.0	250	500	μA
			Standby	-	-	1	μA
f _{FM(ant)}	FM input frequency	FM-ANT		76	-	108	MHz
T _{AMB}	Ambient temperature		V _{CC} = V _{DD} = 3V	-10	-	75	°C
			V _{CC} = V _{DD} = 5V	-40	-	85	°C
FM parameters							
V _{RF}	RF sensitivity input voltage		f _{RF} = 76 to 108 MHz df = 22.5kHz f _{mod} = 1kHz (S+N)/N = 26dB de-emphasis = 75us BAF=300 Hz to 15 kHz	-	1	3	UV
	Pilot suppression		d _{f_pilot} = 6.75kHz d _f =68.5kHz		35		dB
IP _{3in}	Inband 3 rd order intercept point at LNA input			-	-	-	dBμV
IP _{3out}	Outband 3 rd order intercept point at LNA input			-	-	-	dBμV
S ₋₃₀₀	LOW side 300 Khz selectivity		dF = -300kHz f _{tuned} = 76 to 108 MHz	32	35	-	dB
S ₊₃₀₀	HIGH side 300 Khz selectivity		dF = +300kHz f _{tuned} = 76 to 108 MHz	42	45	-	dB
S ₋₂₀₀	LOW side 200 Khz selectivity		dF = -200kHz f _{tuned} = 76 to 108 MHz	-	25	-	dB
S ₊₂₀₀	HIGH side 200 Khz selectivity		dF = +200kHz f _{tuned} = 76 to 108 MHz	-	35	-	dB
IR	Image Rejection		f _{tuned} = 76 to 108 MHz	-	26	-	dB
V _{OUTL} V _{OUTR}	L and R audio output voltage		V _{RF} = 1mV; L = R; df = 22.5kHz; f _{mod} =1kHz	-	100	-	mV
(S+N)/N	maximum signal plus noise-to-noise ratio		V _{RF} = 1mV; L = R; df = 22.5kHz; f _{mod} =1kHz de-emphasis = 75us	48	55	-	dB
α _{cs(stereo)}	Stereo channel separation		V _{RF} = 1mV; R = 1 and L = 0 or R = 0 and L = 1; f _{mod} = 1kHz; d _{f_pilot} = 6.75kHz; d _{fL} = 68.5kHz and d _{fR} = 0 or d _{fR} = 68.5kHz and d _{fL} = 0	22	25	-	dB
THD	Total Harmonic Distortion		V _{RF} =1mV; L=R; df=75kHz; f _{mod} =1kHz; BAF=300Hz to 15kHz	-	0.9	2.0	%
			V _{RF} =1mV; L=R; df=22.5kHz; f _{mod} =1kHz; BAF=300Hz to 15kHz	-	0.4	1.0	%
	Integrated De-emphasis			50/75			μs

Digital interface

3-wire bus

Access to the LV2400x is done through the 3-wire bus:

CLOCK	Data strobe, input to the LV2400x
NR_W	Command (Write or read data), input to the LV2400x
DATA	Bi-directional pin: input to the LV2400x when NR_W is high, output from the LV2400x when NR_W is low.

The LV200x can be configured to generate interrupt through the DATA-line. When interrupt mode is selected, care should be taken that the DATA-line connection to the application micro-controller also supports interrupt.

When the required timing window for frequency measurements is not generated by the application micro-controller, an external clock must be connected to CLK_IN pin of the LV2400x

Register map

The LV2400x registers are divided in 2 blocks:

Block 01h	Status and measurement
Block 02h	Control

To access a register in a block, the block must be first selected by writing the block number to the BLK_SEL register. Block selection can be skipped for subsequent accesses to other registers in the same block.

The mapping is as follows:

Block	Address	Register name	Access	Operation
01h	00h	CHIP_ID	R	Chip identification
	01h	BLK_SEL	W	Block Select
	02h	MSRC_SEL	W	Measure source select
	03h	FM_OSC	W	DAC control for FM-RF oscillator
	04h	SD_OSC	W	DAC control for stereo decoder oscillator
	05h	IF_OSC	W	DAC control for IF oscillator
	06h	CNT_CTRL	W	Counter control
	07h	NA	-	
	08h	IRQ_MSK	W	Interrupt mask
	09h	FM_CAP	W	CAP bank control for RF-frequency
	0Ah	CNT_L	R	Counter value low byte
	0Bh	CNT_H	R	Counter value high byte
	0Ch	CTRL_STAT	R	Control status
	0Dh	RADIO_STAT	R	Radio station status
	0Eh	IRQ_ID	R	Interrupt identify
	0Fh	IRQ_OUT	W	Set Interrupt on DATA-line
	02h	01h	BLK_SEL	W
02h		RADIO_CTRL1	W	Radio control 1
03h		IFCEN_OSC	W	IF Center Frequency Oscillator

	04h	NA	-	
	05h	IF_BW	W	IF Bandwidth
	06h	RADIO_CTRL2	W	Radio Control 2
	07h	RADIO_CTRL3	W	Radio control 3
	08h	STEREO_CTRL	W	Stereo Control
	09h	AUDIO_CTRL1	W	Audio Control 1
	0Ah	AUDIO_CTRL2	W	Audio Control 1
	0Bh	PW_SCTRL	W	Power and soft control

Not mentioned registers are not defined and should not be accessed.

Register description

Block x, Register 01h – BLK_SEL – Block Select register (Write Only)

7	6	5	4	3	2	1	0
BN[7:0]							
Bit 7-0: BN[7:0] : 8-bit block number. For LV2400x, the following numbers are valid: 01h. 02h.							
Note: This register can be accessed from any block							

Block 1, Register 00h – CHIP_ID – Chip identify register (Read Only)

7	6	5	4	3	2	1	0
ID[7:0]							
Bit 7-0: ID[7:0] : 8-bit chip ID. The following ID's are defined: 05h for LV24000/LV24001 04h for LV24002							

Block 1, Register 02h – MSRC_SEL – Measurement Source Select Register (Write-only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	MSR_O	Reserved	MSS_SD	MSS_FM	MSS_IF
<p>Bit 7: Reserved: Must be programmed with 0.</p> <p>Bit 6-5: Reserved: Must be programmed with 0.</p> <p>Bit 4: MSR_O: Output measure source to DATA-pin 0 = Measuring source not available at DATA-pin (Normal operation). 1 = Measuring source available at DATA-pin (test-mode). Must be programmed with 0.</p> <p>Bit 3: Reserved: Must be programmed with 0.</p> <p>Bit 2: MSS_SD: Stereo decoder oscillator measurement 0 = Disable stereo decoder oscillator measurement 1 = Enable stereo decoder oscillator measurement</p> <p>Bit 1: MSS_FM: FM RF oscillator measurement 0 = Disable FM RF oscillator measurement 1 = Enable FM RF oscillator measurement</p> <p>Bit 0: MSS_IF: IF oscillator measurement 0 = Disable IF oscillator measurement 1 = Enable IF oscillator measurement</p> <p>Note:</p> <ul style="list-style-type: none"> - Only one of the measurement source MSS_xx bits may be set at a time. - The FM RF frequency is divided with 256 before it goes to the measuring circuitry. 							

Block 1, Register 03h – FM_OSC – FM RF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
FMOSC[7:0]							
<p>Bit 7-0: FMOSC[7:0]: DAC value to control the FM RF oscillator (fine step)</p> <p>Note:</p> <ul style="list-style-type: none"> - Positive DAC control (i.e. the frequency increases with the register's value) - See also FM_CAP register 							

Block 1, Register 04h – SD_OSC – Stereo Decoder Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
SDOSC[7:0]							
Bit 7-0: SDOSC[7:0]: DAC value to control the stereo decoder oscillator							
Note: Positive DAC control (i.e. the frequency increases with the register's value)							

Block 1, Register 05h – IF_OSC – IF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
IFOSC[7:0]							
Bit 7-0: IFOSC[7:0]: DAC value to control the IF oscillator							
Note: Positive DAC control (i.e. the frequency increases with the register's value)							

Block 1, Register 06h – CNT_CTRL – Counters Control Register (Write-only)

7	6	5	4	3	2	1	0																											
CNT1_CLR	CTAB2	CTAB1	CTAB0	SWP_CNT_L	CNT_EN	CNT_SEL	CNT_SET																											
Bit 7: CNT1_CLR: Clear counter 1 bit 0 = Normal mode 1 = Clear and keep counter 1 in reset mode																																		
Bit 6-4: CTAB[2:0]: Tab select for counter 2 measuring interval bits																																		
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Value</th> <th>Dec.</th> <th>Stop value</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0</td> <td>Stop after 2 counts</td> </tr> <tr> <td>001b</td> <td>1</td> <td>Stop after 8 counts</td> </tr> <tr> <td>010b</td> <td>2</td> <td>Stop after 32 counts</td> </tr> <tr> <td>011b</td> <td>3</td> <td>Stop after 128 counts</td> </tr> <tr> <td>100b</td> <td>4</td> <td>Stop after 512 counts</td> </tr> <tr> <td>101b</td> <td>5</td> <td>Stop after 2048 counts</td> </tr> <tr> <td>110b</td> <td>6</td> <td>Stop after 8192 counts</td> </tr> <tr> <td>111b</td> <td>7</td> <td>Stop after 32768 counts</td> </tr> </tbody> </table>								Value	Dec.	Stop value	000b	0	Stop after 2 counts	001b	1	Stop after 8 counts	010b	2	Stop after 32 counts	011b	3	Stop after 128 counts	100b	4	Stop after 512 counts	101b	5	Stop after 2048 counts	110b	6	Stop after 8192 counts	111b	7	Stop after 32768 counts
Value	Dec.	Stop value																																
000b	0	Stop after 2 counts																																
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100b	4	Stop after 512 counts																																
101b	5	Stop after 2048 counts																																
110b	6	Stop after 8192 counts																																
111b	7	Stop after 32768 counts																																
Bit 3: SWP_CNT_L: Swap counter 1 and counter 2 bit (Active low) 0 = Clock source 1 to counter 2, clock source 2 to counter 1 (swapping) 1 = Clock source 1 to counter 1, clock source 2 to counter 2 (no swap)																																		
Bit 2: CNT_EN: Enable the currently selected counter bit 0 = Disable counter (stop counting) 1 = Enable counter (counting mode)																																		
Bit 1: CNT_SEL: counter select bit 0 = Select counter 1 for measurement 1 = Select counter 2 for measurement																																		
Bit 0: CNT_SET: Set counters bit 0 = Normal mode 1 = Set both counter 1 and counter 2 to FFFFh and keep them set																																		

Block 1, Register 08h – IRQ_MSK – Interrupt Mask Register (Write-only)

7	6	5	4	3	2	1	0
Reserved	IM_MS	Reserved	Reserved	IRQ_LVL	IM_AFC	IM_FS	IM_CNT2
<p>Bit 7: Reserved: Must be programmed with 0.</p> <p>Bit 6: IM_MS: Mono/Stereo interrupt mask bit 0 = Disable mono/stereo change interrupt 1 = Enable mono/stereo change interrupt</p> <p>Bit 5: Reserved: Must be programmed with 0.</p> <p>Bit 4: Reserved: Must be programmed with 0.</p> <p>Bit 3: IRQ_LVL: Interrupt level select bit 0 = Drive DATA-line from low to high when interrupt occurs (active high) 1 = Drive DATA-line from high to low when interrupt occurs (active low)</p> <p>Bit 2: IM_AFC: AFC out of range interrupt mask bit 0 = Disable AFC out of range interrupt 1 = Enable AFC out of range interrupt</p> <p>Bit 1: IM_FS: Field strength change interrupt mask bit 0 = Disable field strength change interrupt 1 = Enable field strength change interrupt</p> <p>Bit 0: IM_CNT2: Counter 2 counting done interrupt mask bit 0 = Disable counter 2 counting done interrupt 1 = Enable counter 2 counting done interrupt</p>							

Block 1, Register 09h – FM_CAP – FM RF Capacitor Bank Register (Write-only)

7	6	5	4	3	2	1	0
FMCAP[7:0]							
<p>Bit 7-0: FMCAP[7:0]: CAP bank value to control the FM RF frequency (coarse steps)</p> <p>Note:</p> <ul style="list-style-type: none"> - 7½ bit CAP value (Bit[7:6]: Combination 10b and 01b results in the same CAP-range) - Negative control: de RF frequency decreases when increasing the register's value - See also FM_OSC register 							

Block 1, Register 0Ah – CNT_L – Counter Value Low Register (Read-only)

7	6	5	4	3	2	1	0
CNT_LSB[7:0]							
Bit 7-0: CNT_LSB[7:0] : Lower 8-bit value of the 16 bit counter							

Block 1, Register 0Bh – CNT_H – Counter Value High Register (Read-only)

7	6	5	4	3	2	1	0
CNT_MSB[7:0]							
Bit 7-0: CNT_MSB[7:0] : Upper 8-bit value of the 16 bit counter							

Block 1, Register 0Ch – CTRL_STAT – Control Status Register (Read-only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AFC_FLG
Bit 7-1: Reserved[7:1] : should be read as all 1							
Bit 0: AFC_FLG : AFC out of range bit 0 = AFC is within control range 1 = AFC is out of control range							
Note: Reading this register will clear AFC, count 2 done interrupt.							

Block 1, Register 0Dh – RADIO_STAT – Radio Station Status Register (Read-only)

7	6	5	4	3	2	1	0
RSS_MS	RSS_FS						
Bit 7: RSS_MS : Radio station mono/stereo state bit 0 = Mono 1 = Stereo							
Bit 6-0: RSS_FS[6:0] : Radio station field strength bits 1111111b = Field strength less than 10 dB μ V 1111110b = Field strength between 10 to 20 dB μ V 1111100b = Field strength between 20 to 30 dB μ V 1111000b = Field strength between 30 to 40 dB μ V 1110000b = Field strength between 40 to 50 dB μ V 1100000b = Field strength between 50 to 60 dB μ V 1000000b = Field strength between 60 to 70 dB μ V 0000000b = Field strength above 70 dB μ V							
Note: Reading this register will clear field strength and mono/stereo interrupt.							

Block 1, Register 0Eh – IRQ_ID – Interrupt Identify Register (Read-only)

7	6	5	4	3	2	1	0
Reserved	Reserved	II_CNT2	Reserved	II_AFC	Reserved	II_MS	II_FS
<p>Bit 7: Reserved: should be read as 1</p> <p>Bit 6: Reserved: should be read as 1</p> <p>Bit 5: II_CNT2: Counter 2 counting done flag 0 = No counting 2 counting done interrupt 1 = Measuring with counter 2 is done</p> <p>Bit 4: Reserved: should be read as 1</p> <p>Bit 3: II_AFC: AFC out of range interrupt bit 0 = No AFC interrupt 1 = AFC fails to hold the RF-frequency in range</p> <p>Bit 2: Reserved: should be read as 1</p> <p>Bit 1: II_MS: Mono/stereo interrupt bit 0 = No change in mono/stereo mode 1 = Mono/stereo mode has changed</p> <p>Bit 0: II_FS: Field strength interrupt bit 0 = No change in field strength 1 = Changing in field strength bits detected</p>							

Block 1, Register 0Fh – IRQ_OUT – Set Interrupt Out Register (Write Only)

7	6	5	4	3	2	1	0
IRQO_VAL[7:0]							
<p>Bit 7-0: IRQO_VAL[7:0]: Write any value to this register will select the interrupt as output on the DATA-line of the LV2400x (the DATA-line can then be used as interrupt pin)</p>							

Block 2, Register 02h – RADIO_CTRL1 – Radio Control 1 Register (Write-only)

7	6	5	4	3	2	1	0
EN_MEAS	EN_AFC	Reserved	Reserved	DIR_AFC	RST_AFC	Reserved	Reserved
Bit 7:	EN_MEAS: Enable measurement bit 0 = Normal mode 1 = Measurement mode						
Bit 6:	EN_AFC: Enable AFC bit 0 = Disable AFC 1 = Enable AFC						
Bit 5:	Reserved: should be written with 0						
Bit 4:	Reserved: should be written with 0						
Bit 3:	DIR_AFC: AFC direction bit 0 = AFC normal direction 1 = AFC reverse direction (for test purpose)						
Bit 2:	RST_AFC: Reset AFC bit 0 = Normal operation 1 = Reset AFC to the middle of the control range						
Bit 1:	Reserved: should be written with 0						
Bit 0:	Reserved: should be written with 0						

Block 2, Register 03h – IFCEN_OSC – IF Center Frequency Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
IFCOSC[7:0]							
Bit 7-0:	IFCOSC[7:0]: Tuning value for IF center frequency oscillator						

Block 2, Register 05h – IF_BW – IF Bandwidth Register (Write-only)

7	6	5	4	3	2	1	0
IFBW[7:0]							
Bit 7-0:	IFBW[7:0]: Value for IF bandwidth						

Block 2, Register 06h – RADIO_CTRL2 – Radio Control 2 Register (Write-only)

7	6	5	4	3	2	1	0
VREF2	VREF	AFC_WS	IF_PM_L	Reserved	Reserved	AGCSP	Reserved
Bit 7:	VREF2: V_{REF2} control bit 0 = V_{REF2} is ON 1 = V_{REF2} is OFF						
Bit 6:	VREF: V_{REF} control bit 0 = V_{REF} is ON 1 = V_{REF} is OFF						
Bit 5:	AFC_WS: AFC window shift bit 0 = Disable AFC window shift(normal control range) 1 = Enable AFC window shift (extend control range)						
Bit 4:	IF_PM_L: IF PLL mute bit 0 = IF PLL mute on (presetting IF mode) 1 = IF PLL mute off (normal operation mode)						
Bit 3:	Reserved: should be written with 0						
Bit 2:	Reserved: should be written with 0						
Bit 1:	AGCSP: AGC speed control bit 0 = Normal speed 1 = High speed						
Bit 0:	Reserved: should be written with 0						

Block 2, Register 07h – RADIO_CTRL3 – Radio Control 3 Register (Write-only)

7	6	5	4	3	2	1	0
PWR_LV	VOLSH	TB_ON	AMUTE_L	SE_FM	Reserved	SE_BE	SE_EXT
<p>Bit 7: PWR_LVL: Power level bit 0 = Normal power level 1 = Power level for test</p> <p>Bit 6: VOLSH: Volume level shift bit 0 = Normal volume level 1 = Extra volume of 12 dB</p> <p>Bit 5: TB_ON: Treble/Bass on bit 0 = Turn off treble/Bass control 1 = Turn on treble/Bass control</p> <p> Note: This bit should be written with 1 when one of the TREB_N, TREB_P, BASS_N, BASS_P and BASS_PP bits of AUDIO_CTRL2 register is 1. When none of these bits is set, this bit should be written with 0</p> <p>Bit 4: AMUTE_L: Audio mute bit 0 = Audio muted 1 = Audio not muted</p> <p>Bit 3: SE_FM: FM radio select bit 0 = FM radio is not selected as playing source 1 = FM radio is selected as playing source</p> <p>Bit 2: Reserved: should be written with 0</p> <p>Bit 1: SE_BE: Beep select bit 0 = Beep not selected as playing source 1 = Beep is selected as playing source</p> <p>For LV24000: Bit 0: Reserved: should be written with 0</p> <p>For LV24001 and LV24002: Bit 0: SE_EXT: External source select bit 0 = FM not selected as playing source 1 = FM is selected as playing source</p>							

Block 2, Register 08h – STEREO_CTRL – Stereo Control Register (Write-only)

7	6	5	4	3	2	1	0
FRCST	FMCS[2:0]			AUTOSSR	DISITG	SD_PM	ST_M
Bit 7:	FRCST: Force stereo bit 0 = Normal mode 1 = Force stereo mode for test						
Bit 6-4:	FMCS[2:0]: FM channel separation bits 0...7 = FM channel separation level						
Bit 3:	AUTOSSR: Auto stereo slew rate enable bit 0 = Disable stereo auto slew rate 1 = Enable stereo auto slew rate						
Bit 2:	DISITG: Disable integrator bit 0 = Enable integrator 1 = Disable integrator						
Bit 1:	SD_PM: Stereo decoder PLL mute bit 0 = Stereo decoder PLL not muted (normal operation) 1 = Stereo decoder PLL is muted (presetting mode)						
Bit 0:	ST_M: FM stereo/mono mode bit 0 = Stereo mode 1 = Mono mode						

Block 2, Register 09h – AUDIO_CTRL1 – Audio Control 1 Register (Write-only)

7	6	5	4	3	2	1	0
TONE_LVL				VOL_LVL			
Bit 7-4:	TONE_LVL: Tone level bits 1111b = Minimum tone level. 0000b = Maximum tone level.						
Bit 3-0:	VOL_LVL: volume level bits 1111b = Minimum volume level. 0000b = Maximum volume level. Each level is 3dB volume adjustment.						
<p>Note: The tone level may not be greater than the volume level. This means the value of bit [7:4] must be greater or equal to the value of bit [3:0] (the higher the value, the lower the level)</p>							

Block 2, Register 0Ah – AUDIO_CTRL2 – Audio Control 2 Register (Write-only)

7	6	5	4	3	2	1	0
BPFREQ		DEEMP	TREB_N	TREB_P	BASS_N	BASS_P	BASS_PP
<p>Bit 7-6: BPFREQ: Beep frequency bits 00b = 2 kHz beep tone. 01b = 1 kHz beep tone. 10b = 0.5 kHz beep tone. 11b = beep-output high.</p> <p> Note: Bit [7:6] should be programmed with 11b when beep source is disabled (SE_BE bit of RADIO_CTRL3 register is 0)</p> <p>Bit 5: DEEMP: De-emphasis bit 0 = De-emphasis 50 μs. 1 = De-emphasis 75 μs.</p> <p>Bit 4: TREB_N: Treble negative bit 0 = Normal treble 1 = Negative treble</p> <p>Bit 3: TREB_P: Treble positive bit 0 = Normal treble 1 = Positive treble</p> <p> Note: TREB_N and TREB_P may be not be activated at the same time.</p> <p>Bit 2: BASS_N: Bass negative bit 0 = Normal bass 1 = Negative bass</p> <p>Bit 1: BASS_P: Bass positive bit 0 = Normal bass 1 = Positive bass</p> <p> Note: BASS_N and BASS_P may be not be activated at the same time.</p> <p>Bit 0: BASS_PP: Bass extra positive level bit 0 = Normal bass positive level 1 = Extra bass positive level</p>							

Block 2, Register 0Bh – PW_SCTRL – Power and Soft Control Register (Write-only)

7	6	5	4	3	2	1	0
SS_CTRL			SM_CTRL			PW_HPA	PW_RAD
Bit 7-5:	SS_CTRL: Soft stereo control bits (8 levels) 000b = Minimal soft stereo (off) 111b = Maximal soft stereo level						
Bit 4-2:	SM_CTRL: Soft audio mute bits (8 levels) 000b = Minimal audio mute (off) 111b = Maximal soft audio mute level						
For LV24000 and LV24001:							
Bit 1:	Reserved: should be written with 0						
For LV24002:							
Bit 1:	PW_HPA: Headphone amplifier power bit 0 = Headphone amplifier is switched OFF. 1 = Switch headphone amplifier ON Note: PW_HPA is 0 at power up						
Bit 0:	PW_RAD: Radio circuitry power bit 0 = Radio circuitry is switched OFF. 1 = Switch radio circuitry ON Note: - PW_RAD is 0 at power up - PW_RAD does not switch on the headphone amplifier of the LV24002. The headphone amplifier is controlled by PW_HPA bit.						

Functional descriptions

Initialization the LV2400x

After power-up, the LV2400x needs to be initialized as follow:

1. Default value for register: TBD
2. IF filter setting: TBD
3. IF center filter setting: TBD
4. Calibrate the IF frequency at 110 kHz as follows:
 - Enable measure mode of LV2400X (register RADIO_CTRL1 – EN_MEAS bit)
 - Enable the demodulator PLL mute (register RADIO_CTRL2 – IF_PM_L bit)
 - Enable measuring IF-frequency (register MSRC_SELL – MSS_IF bit)
 - Tuning the IF_OSC register to the specified frequency
 - Restore measurement source select (register MSRC_SEL)
 - Disable the demodulator PLL mute (register RADIO_CTRL2 – IF_PM_L bit)
 - Restore the measure mode of LV2400X (register RADIO_CTRL1 – EN_MEAS bit)
5. Calibrate the stereo decoder clock at 37.5kHz as follows:
 - Enable measure mode of LV2400X (register RADIO_CTRL1 – EN_MEAS bit)
 - Enable the stereo PLL mute (register STEREO_CTRL - SD_PM bit)
 - Enable measuring stereo decoder frequency (register MSRC_SELL – MSS_SD bit)
 - Tuning the SD_OSC register to the specified frequency.
 - Restore measurement source select (register MSRC_SEL)
 - Disable the stereo PLL mute (register STEREO_CTRL - SD_PM bit)
 - Restore the measure mode of LV2400X (register RADIO_CTRL1 – EN_MEAS bit)

Accessing the LV2400x

Access to the LV24000x can be done through the 3-wire bus. At host side, The NR_W and CLOCK are output signals, while the DATA is bi-directional.

When power up, host should initialize the 3-wire bus in host read mode:

1. Set direction of the DATA-line to input-mode.
2. Drive NR_W low
3. Drive CLOCK high

Note : Use following sequence for changing read/write mode:

- A. Change from host read-mode to host write-mode:
 - A.1. Keep the CLOCK signal HIGH.
 - A.2. Set the NR_W signal to HIGH (write mode)
 - A.3. Set the DATA-pin direction to OUTPUT mode.
- B. Change from host write-mode to host read-mode:
 - B.1. Keep the CLOCK signal HIGH.
 - B.2. Set the DATA-pin direction to INPUT mode.
 - B.3. Set NR-W to LOW (read mode).

Writing the LV2400x

Writing the LV2400x is done in two phases (if appropriate). First the correct block address needs to be written to the Block Select register (BLK_SEL). The 16-bits data pattern for the block selection consists of:

- Bit[15:8] = 0x01: the address of BLK_SEL register: block select cycle
- Bit[7:0] = block number: block to be selected

Note that the block select register needs to be written unless the last read of write was already done from/to the same block.

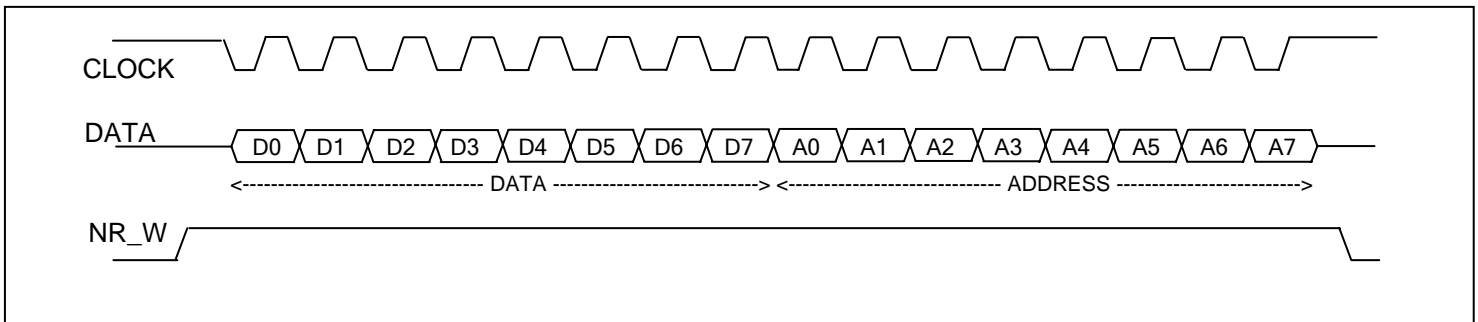
Next the register can be written. The 16 bits data pattern consists of:

- Bit[15:8]: 8 bits register address.
- Bit[7:0]: 8 bits register data.

The 16-bits data pattern (block select and register write) is serially sent to the LV2400X as follows:

- a) Drive NR_W pin high to set the LV2400X in input mode.
- b) Set the direction of DATA-line to output of the host (if required)
- c) Drive the DATA pin to correct level.
- d) Generate positive edge of CLOCK (driving CLOCK from low to high). This signals the LV2400x to latch the data bit.
- e) Delay some time to meet the data hold time requirement of LV2400X.
- f) The clock can be driven low except for the last data bit.
- g) Repeat step (c) to (f) 16 times to shift the 16 bits data pattern into the LV2400X.
- h) Set the direction of DATA-line to input of the host (if required)
- i) Drive NR_W pin to low. This signals the LV2400X to latch the data into correct register.

Note: LSB of the data pattern should be shifted out first.



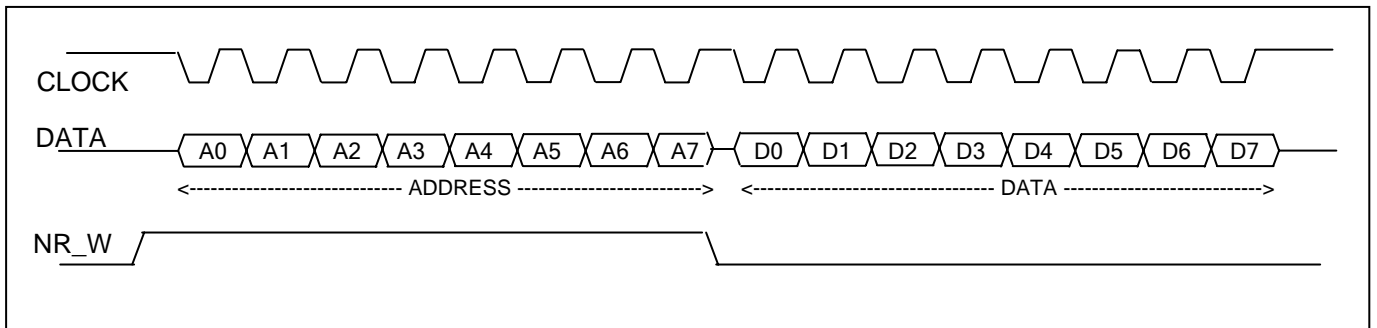
Reading the LV2400X

To read a chip register, the 8 bits register address must be written followed by reading the 8 data bits. Remember that before accessing a register, the correct block must be selected first, unless it already selected (see above).

The register can be serially read as follow:

- a) Optionally select correct block
- b) Drive NR_W line high (write mode)
- c) Set the direction of DATA-line to output of the host (if required)
- d) Drive DATA-line to correct level
- e) Generate positive edge of CLOCK (driving CLOCK from low to high).
- f) Delay some time to meet the data hold time requirement of LV2400X.
- g) The clock can be driven low except for the last address bit.
- h) Repeat step (d) to (j) 8 times to shift the 8 bits register address into the LV2400X (LSB must be shifted out first)
- i) Set the direction of DATA-line to input of the host (if required)
- j) Drive the NR_W line low (read mode).
- k) Drive the CLOCK high to low to generate a negative edge. This signals the LV2400x to put the data bit on the DATA-line.
- l) Delay sometime to meet the data setup time requirement of LV2400x.
- m) Drive CLOCK-line low to high.
- n) Read the data bit at the DATA-line (The data can also be read after step l).
- o) Repeat step (k) to (m) 8 times to read the 8 bits data out of the LV2400x.

Note: The LV2400X will shift the LSB of the data out first.

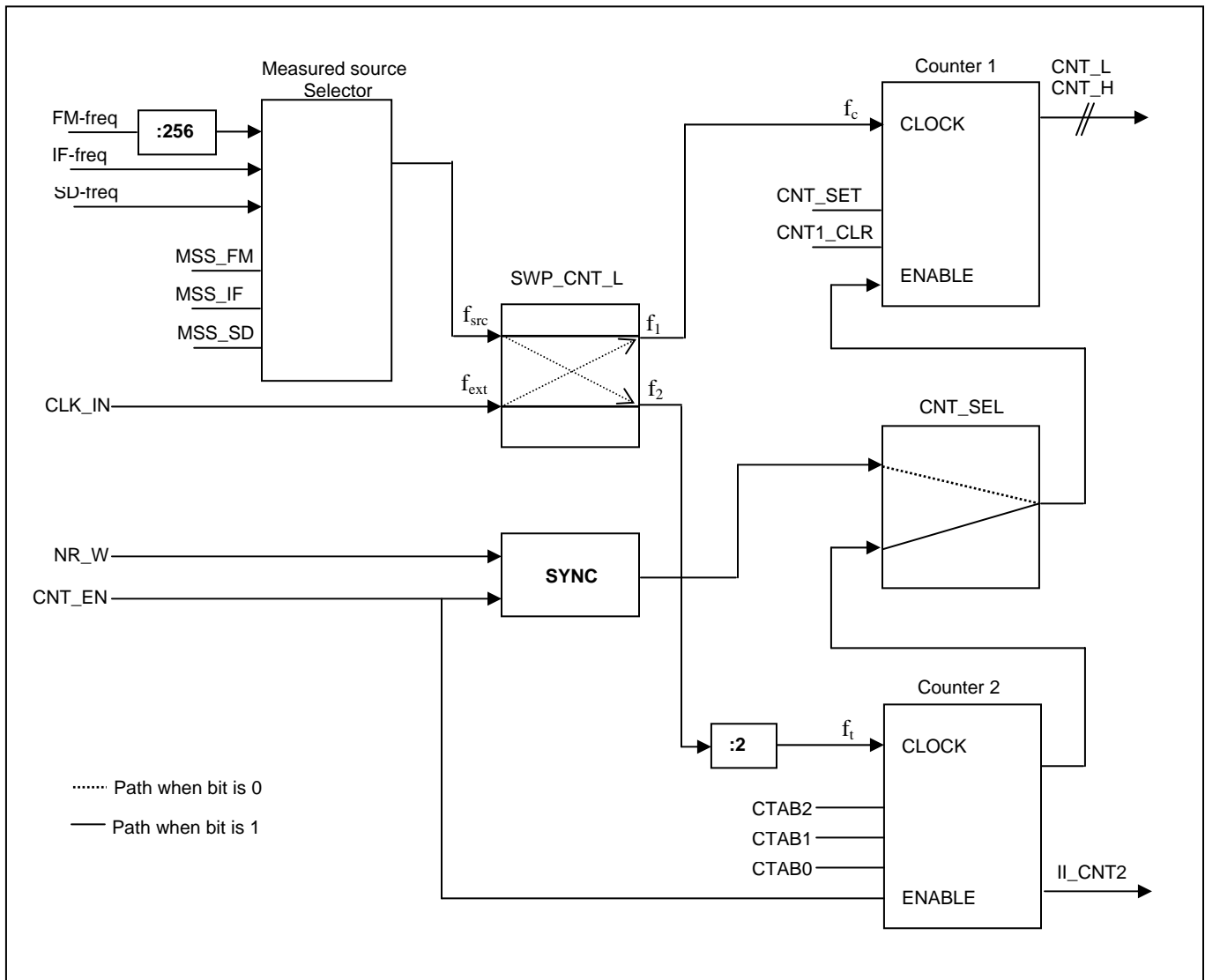


Measuring frequency with the LV2400X

The 3 frequencies IF, stereo decoder clock and FM can be determined by counting the pulses within a timing window. The pulses can be counted with the built-in counter 1. The timing window can be created by host software or by (optionally) using counter 2.

When counter 1 is selected (CNT_SEL bit in CNT_CTRL register is 0), the measurement is controlled by NR_W-line: counter 1 starts counting when it is enabled and the NR_W-line goes low. Counter 1 stops with counting as soon as the NR_W-line goes high. The 16-bit pulse count can be read back at CNT_H/CNT_L register. The active time of NR_W is the measuring period.

When counter 2 is selected, the measurement is controlled by CLK_IN line and the tab select bits CTAB[2:0]. Counter 2 will enable counter 1 when CNT_EN is active, after the number of count which is selected by the host software via CTAB[2:0]-bits, counter 2 stops the measurement and drives II_CNT2 flag active to indicate the measurement is ended. The 16-bit pulse count can be read back at CNT_H/CNT_L register. The input clock of counter 2 and the tab-selection determines the measuring period. When SWP_CNT bit is high, the measuring source will go to counter 2 instead of counter 1. Only set this bit when CLK_IN is greater than 100 kHz.



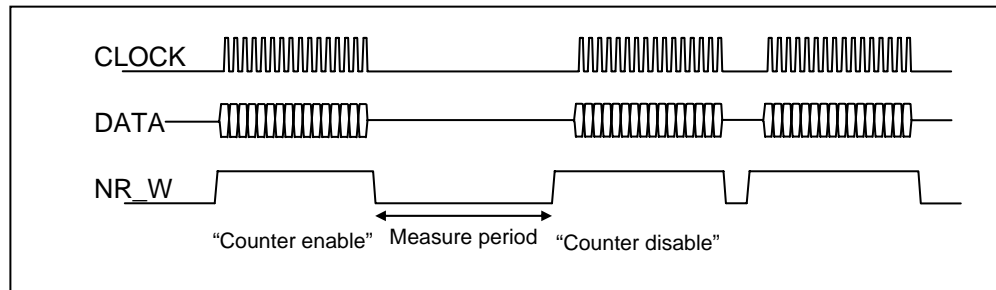
The frequencies of the LV2400x are divided as below table before they go to the measuring circuitry:

Frequency	Divider factor
IF-frequency	1
RF-frequency	256
Stereo decoder clock	1

Measuring with counter 1 (NR_W control)

Perform following steps:

- Enable the frequency source to be measured (register MSRC_SELL – set one of the MSS_xx bits).
- Make sure counter 1 is selected (Register CNT_CTRL – bit CNT_SEL is 0)
- Enable measuring mode (register RADIO_CTRL1 – EN_MEAS bit).
- Reset the counter (register CNT_CTRL – Driving bit CNT1_CLR high then low).
- Start the counter 1 on LV2400x (register CNT_CTRL – set CNT_EN bit). At the moment the NR_W signal gets LOW, the counter starts.
- Wait time t.
- To stop the counter, first set the NR_W signal HIGH, then disable the counter of LV2400x (register CNT_CTRL – clear CNT_EN bit).
- Read the pulse count n from the counter register of LV2400x (register CNT_H/CNT_L).
- Restore the measure mode.
- Restore the measure source select (register MSRC_SEL)



Note:

- The measuring window begins at the moment that the NR_W signal is driving LOW (point e) and ends when the NR_W signal is driving HIGH (point g).
- The precision of the measurement depends on:
 - The duration of t. 1 pulse wrong at t=1ms results in more deviation than at t=32ms
 - The precision of the measuring window: calculate with t=32ms gives other f than with t=32,1ms. Application should take some care to have an accurate measuring window t.

Then the frequency can be calculated with formula:

$$\text{Frequency [Hz]} = \frac{\text{Count value}}{\text{Counting time [s]}} \times \text{Divider factor}$$

The accuracy of this method is shown in below table.

Measure period	Measure deviation		
	IF-frequency	RF-frequency	Stereo-decoder frequency
8 ms	+ 125 Hz	+ 32 kHz	+ 125 Hz
16 ms	+ 62 Hz	+ 16 kHz	+ 62 Hz
32 ms	+ 31 Hz	+ 8 kHz	+ 31 Hz
64 ms	+ 15 Hz	+ 4 kHz	+ 15 Hz
100 ms	+ 10 Hz	+ 2.5 kHz	+ 10 Hz

Measuring with counter 2 (CLK_IN control)

Perform following steps:

- a) Enable the frequency source to be measured (register MSRC_SELL – set one of the MSS_xx bits).
- b) Make sure counter 2 is selected (Register CNT_CTRL – bit CNT_SEL is 1)
- c) Enable measuring mode (register RADIO_CTRL1 – EN_MEAS bit).
- d) Reset the counter (register CNT_CTRL – Driving bit CNT1_CLR high then low).
- e) Program the appropriate tab-select (register CNT_CTRL - CTAB[2:0] bits)
- f) Program the SWP_CNT bit in CNT_CTRL register appropriately
- g) Enable counter 2 interrupt (register IRQ_MSK – IM_CNT2 bit)
- h) Start the counter on LV2400x (register CNT_CTRL – set CNT_EN bit).
- i) Write any data pattern to IRQ_OUT register to let the LV2400x use the DATA-line as interrupt
- j) Host software can poll the DATA-line or wait for interrupt.
- k) When counter 2 interrupt occurs (DATA-line goes active, II_CNT2 flag is set in IRQ_ID register), de measuring is done.
- l) Disable the counter of LV2400x (register CNT_CTRL – clear CNT_EN bit).
- m) Read the pulse count n from the counter register of LV2400x (register CNT_H/CNT_L).
- n) Restore the measure mode.
- o) Restore the measure source select (register MSRC_SEL)
- p) Restore interrupt setting

The frequency can be calculated as follows:

When SWP_CNT_L is 1 (no counters swapping):

$$\text{Frequency [Hz]} = \frac{N * f_{\text{ext}}}{\text{Tab} * 2} \times \text{Divider factor}$$

When SWP_CNT_L is 0 (counters are swapped):

$$\text{Frequency [Hz]} = \frac{f_{\text{ext}} * \text{Tab} * 2}{N} \times \text{Divider factor}$$

N: pulse count (read back from CNT_L/CNT_H)

f_{ext}: Frequency of the external clock on CLK_IN-line

Tab: tab selected by CTAB[2:0] (example: if CTAB[2:0] = 101b, value of tab is 2048)

The deviation 1/N (assume no deviation in f_{ext})

Using the Digital Automatic Frequency Control (AFC) of the LV2400x

AFC is the mechanism that prevents the FM-frequency from drifting (FM-frequency drifting will de-tune the radio reception)

To enable the AFC:

- The AFC_WS bit (RADIO_CTRL2 register) should be high
- Clear the DIR_AFC bit (RADIO_CTRL1 register) for normal operation mode
- Clear the RST_AFC bit ((RADIO_CTRL1 register)
- Set the EN_AFC bit (RADIO_CTRL1 register)

To disable the AFC:

- Don't touch the AFC_WS bit (RADIO_CTRL2 register) and DIR_AFC bit (RADIO_CTRL1 register)
- Set the RST_AFC bit (RADIO_CTRL1 register)
- Clear the EN_AFC bit (RADIO_CTRL1 register)

Because the AFC adjusts the FM-frequency, it is recommended to disable the AFC before setting FM-frequency.

Using interrupt of the LV2400x

Prepare the LV2400x for generating interrupt:

- Clear any pending interrupt (by reading RADIO_STAT and CTRL_STAT register)
- Program the interrupt level (register IRQ_MSK - IRQ_LVL bit)
- Program the IRQ_MSK register to enable the desired interrupt(s)
- Write any data pattern to IRQ_OUT register to let the LV2400x generate interrupt on the DATA-line

Interrupt handler on the host side:

- Read the IRQ_ID register to identify the interrupt(s)
- Serve all enabled interrupts
- Clear the served interrupt(s)
- Write any data pattern to IRQ_OUT register to arm the interrupt again

Overview of LV2400x interrupts

Interrupt	Enable bit (IRQ_MSK)	ID bit (IRQ_ID)	Clear action	Handling
Counter 2 done	IM_CNT2	II_CNT2	Disable counter	Frequency calculation
AFC out of range	IM_AFC	II_AFC	Read CTRL_STAT register	Re-tune the FM-frequency
Mono/Stereo changed	IM_MS	II_MS	Read RADIO_STAT register	Update display
Field strength changed	IM_FS	II_FS	Read RADIO_STAT register	Update display

Using audio control of the LV2400x

Audio volume control

21 volume levels can be realized using AMUTE_L-bit, VOLSH-bit in RADIO_CTRL3-register and the 4 volume level VOL_LVL bits in AUDIO_CTRL1-register as following scheme:

Volume	AMUTE_L	VOLSH	VOL_LVL[3:0]	Remark
0	0	X	X	No sound (audio muted)
1...16	1	0	15...0	Volume without VOLSH-bit
17...20	1	1	3..0	Extra levels with VOLSH-bit

Tone (loudness) control

The 4 tone level bits TONE_LVL (bit [7:4] of the AUDIO_CTRL1-register) can be used for dynamic bass boost feature: Host software can let the tone level follow the volume level until a pre-defined tone level is reached to introduce more or less bass according to the volume level. Program these 4 bits with 1111b to keep the LV2400x at fixed bass level when this feature is not desired (no dynamic bass boost).

Host software should make sure that the tone level may not exceed the volume level (Note that that tone/volume levels are the inverse of the register's value). For example when the dynamic bass boost is preset at 9 (value 15-9=6 must be used as lowest tone value), following scheme should be used:

VOL_LVL (AUDIO_CTRL1[3:0])	TONE_LVL (AUDI_CTRL1[7:4])	Remark
15...6	15...6	Tone bits follow volume bits (Volume level varies from 0...9, so does tone level)
5...0	6	Tone bits stick at 6 for dynamic bass level 9

Treble control

3 treble levels can be realized using TREB_N-bit, TREB_P-bit in AUDIO_CTRL2 -register and TB_ON-bit in RADIO_CTRL3-register as following scheme:

TB_ON	TREB_N	TREB_P	Remark
1	1	0	Treble level 0
0	0	0	Treble level 1 (flat frequency response)
1	0	0	Treble level 1 (do not use)
1	0	1	Treble level 2

Note: Not mentioned combinations are not allowed.

Bass control

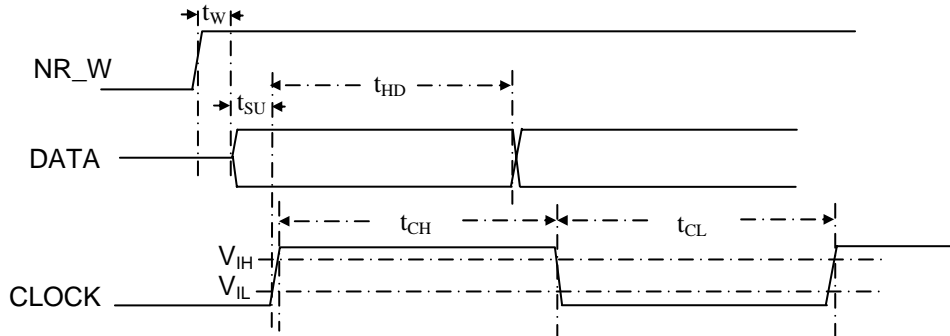
4 bass levels can be realized using BASS_N-bit, BASS_P-bit, BASS_PP-bit in AUDIO_CTRL2 -register and TB_ON-bit in RADIO_CTRL3-register as following scheme:

TB_ON	BASS_N	BASS_P	BASS_PP	
1	1	0	0	Bass level 0
0	0	0	0	Bass level 1 (flat freq. response)
1	0	0	0	Bass level 1 (do not use)
1	0	1	0	Bass level 2
1	0	1	1	Bass level 3

Note: Not mentioned combinations are not allowed.

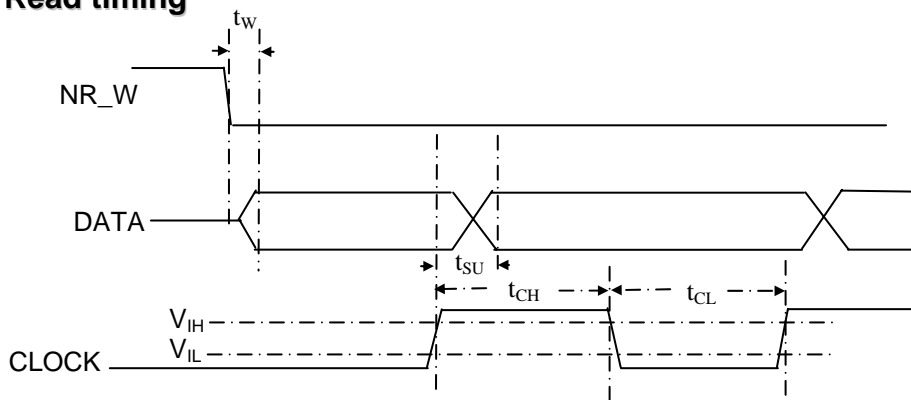
Timing diagrams

Write timing



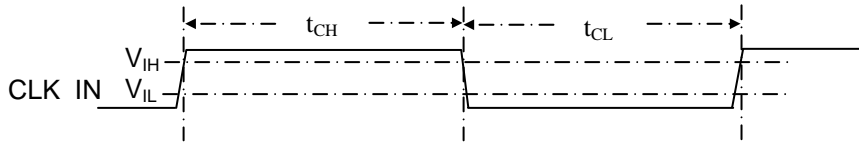
Parm		Ratings			Unit
		Min.	Typ.	Max.	
t_w	Delay from command to data				ns
t_{SU}	Data Setup time				ns
t_{HD}	Data Hold time				ns
t_{CH}	Clock High-level time				ns
t_{CL}	Clock Low-level time				ns

Read timing



Parm		Ratings			Unit
		Min.	Typ.	Max.	
t_w	Delay from command to 1 st data bit				ns
t_{SU}	Data Setup time				ns
t_{CH}	Clock High-level time				ns
t_{CL}	Clock Low-level time				ns

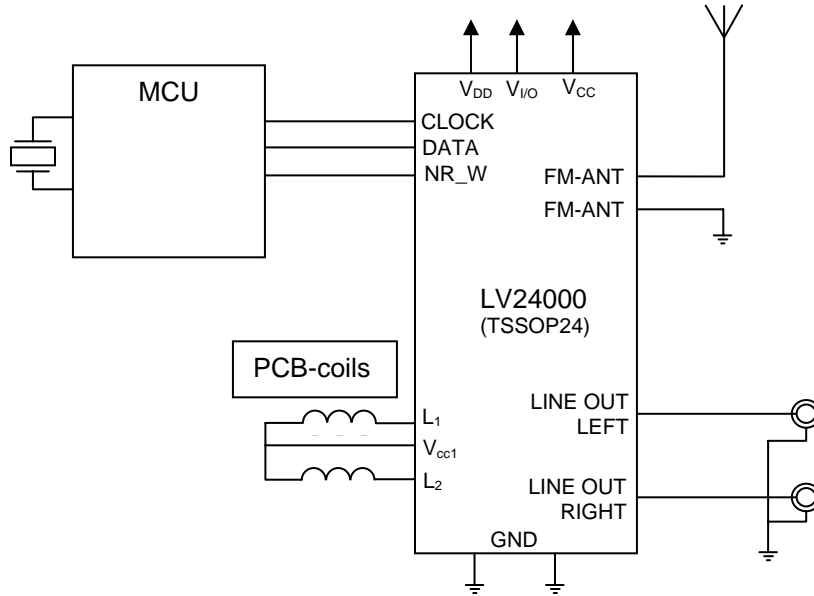
External clock timing



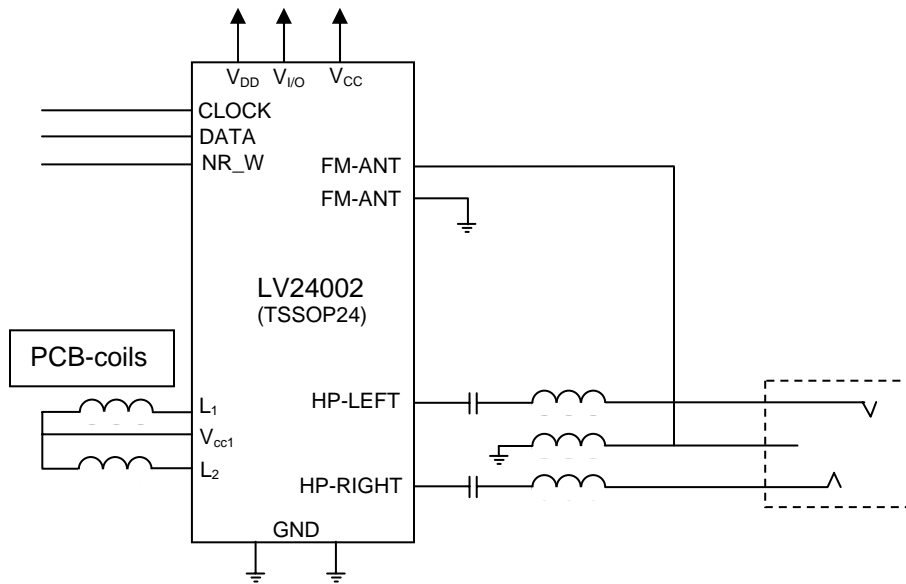
Parm		Ratings			Unit
		Min.	Typ.	Max.	
t_{CH}	Clock High-level time				ns
t_{CL}	Clock Low-level time				ns

Application schematic

LV24000 with line-out/antenna connection.



LV24002 with combined headphone amplifier/antenna circuit.



PCB coil Layout (TSSOP24 only)