



# **VT6206**

## **USB 2.0 Flash Drive Controller**

**Supporting NAND Flash Interface  
USB 2.0 and USB Storage Class 1.0 compliant**

Revision 0.4  
January 19, 2004

**VIA TECHNOLOGIES, INC.**

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## REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	6/13/03	Initial internal release	WL
0.2	7/16/03	Modified product features and functional block diagram Added mechanical specification diagram	EY
0.3	8/26/03	Supported maximum 4 NAND devices, not 8 NAND devices Removed "preliminary" from document revision	EY
0.4	1/19/04	Feature bullet update – Removed ICE support Added LQFP-128 pin diagram and package information	SV

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# VT6206

## USB 2.0 Flash Drive Controller

Supporting NAND Flash interface  
USB 2.0 and USB Storage Class 1.0 compliant

### PRODUCT FEATURES

- **USB Specification 2.0 Compatible**
  - Complies with Universal Serial Bus specification rev 2.0
  - Complies with USB Storage Class specification rev 1.0 (Bulk only protocol)
  - Interface compliant with the UTMI (USB 2.0 Transceiver Macrocell Interface) specification
  - Supports 480Mbit/s high speed and 12Mbit/s full speed
  - Supports endpoints: bi-direction control, bulk read, bulk write, and interrupt
    - 2K-byte buffers for bulk endpoints
    - 64-byte buffers for control endpoint
    - 8-byte buffer for interrupt endpoint
    - Hardware speed negotiation
    - Dedicated bus idle timer
    - Supports firmware upgrade via USB bus
- **Fast 8051 Macrocell 80C32-compatible**
  - Standard 8051 instruction set
  - 60 / 40 / 30 / 10MHz execution speed at 4 cycles per instruction average
  - Supports CPU clock stop
  - Embedded 24KB mask ROM and 256-byte SRAM
  - Additional 256-byte SRAM for general purpose
  - Supports external 64KB ROM/Flash for flexibility
  - Dedicated 2K-byte SRAM for lookup table
- **NAND Flash Interface**
  - Supports 8 / 4-pcs data flash chips
  - Supports 32Mbits - 4Gbits NAND flash disk
  - Supports both 8-bit and 16-bit flash
  - Supports cache read command
  - Hardware ECC generation and verification
  - Firmware ECC error correct capability
  - RBC command conversion for flash disk device
- **Supports External Serial EEPROM Interface for Firmware Parameters**
- **GPIOs for Special Function Use**
  - Dedicated LED indicators
  - Dedicated power control to memory devices

- **Built-in Power-on Reset (POR) and Low-voltage Detector (LVD)**
- **Power**
  - 3.3V power only
  - Built-in 3.3V to 2.5V regulator for core power
- **0.22um Process**
- **Available in 48-pin LQFP Package (7x7x1.4 mm) / 128 LQFP Package (14x14x1.4mm)**

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## OVERVIEW

VIA's VT6206 is a high-performance flash drive controller, which supports USB 2.0 high-speed transmission to NAND type flash memory. The VT6206 integrates USB 2.0 UTMI transceiver to allow for high speed or full speed data transmission (480Mbps or 12Mbps). In addition, it integrates high efficiency card interface hardware engine for data transmission and the RBC command conversion for flash disk devices control.

The VT6206 is a 48-pin LQFP package to make the best cost competitive for high-speed single flash card design. In addition, 128-pin LQFP package with 8 NAND devices for external ROM support is also provided. Therefore, the VT6206 is capable of supporting 8 or 4 NAND flash disks and flash capacity ranges from 32Mbits to 4Gbits, depending on the package being used. With GPIOs and some controllable pins, it provides active LED indication and the power control to memory devices.

For operating systems, the VT6206 flash drive controller is supported by most of the existing operating systems, including Windows XP, Windows 2000, Windows ME, Windows 98, Windows 98SE, Mac OS 9.x, Mac OS X and Linux kernel 2.4.0 and its future versions.

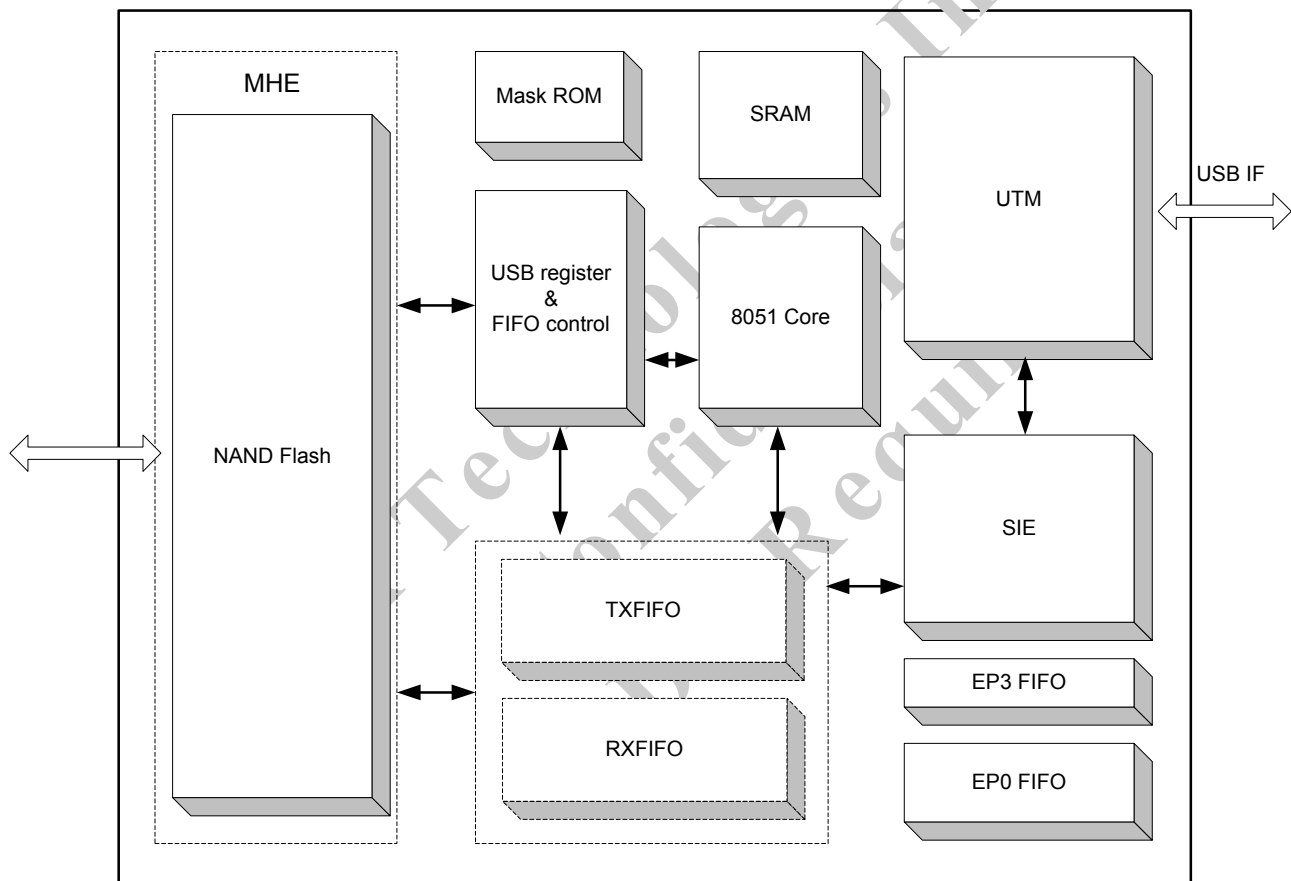


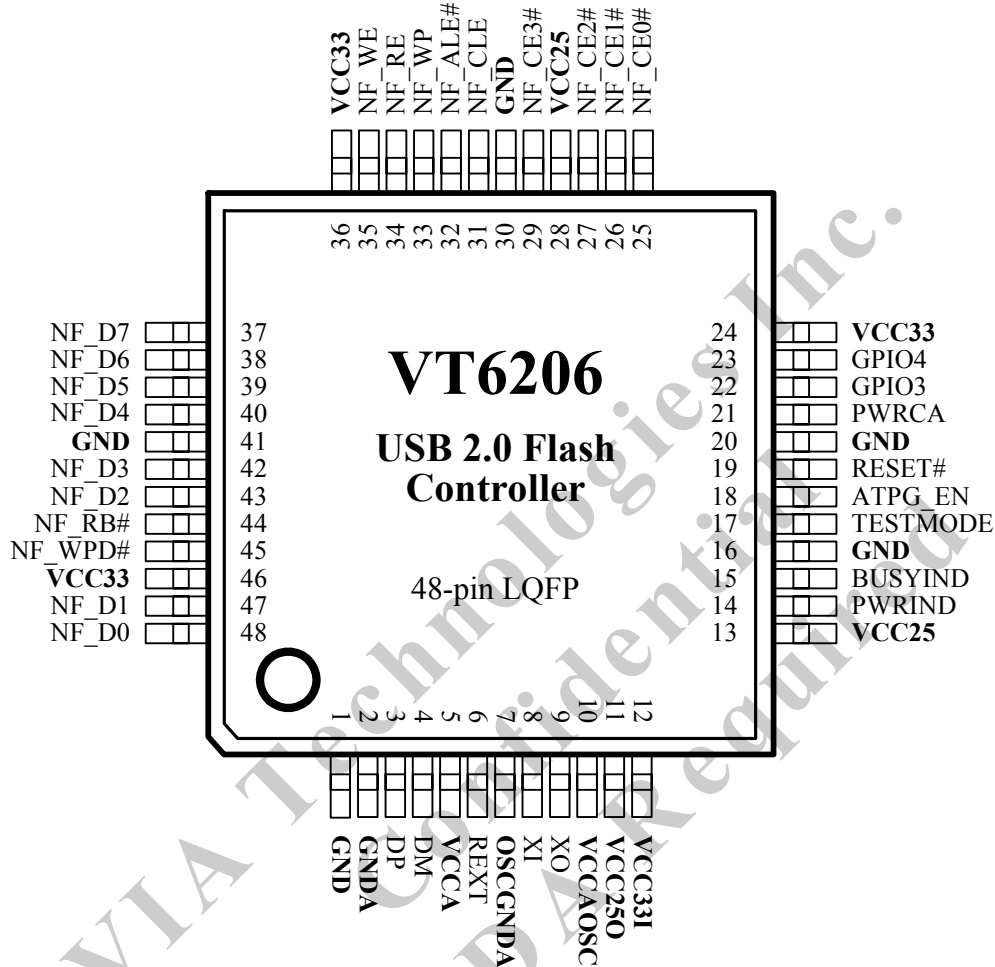
Figure 1. Functional Block Diagram

Notation:

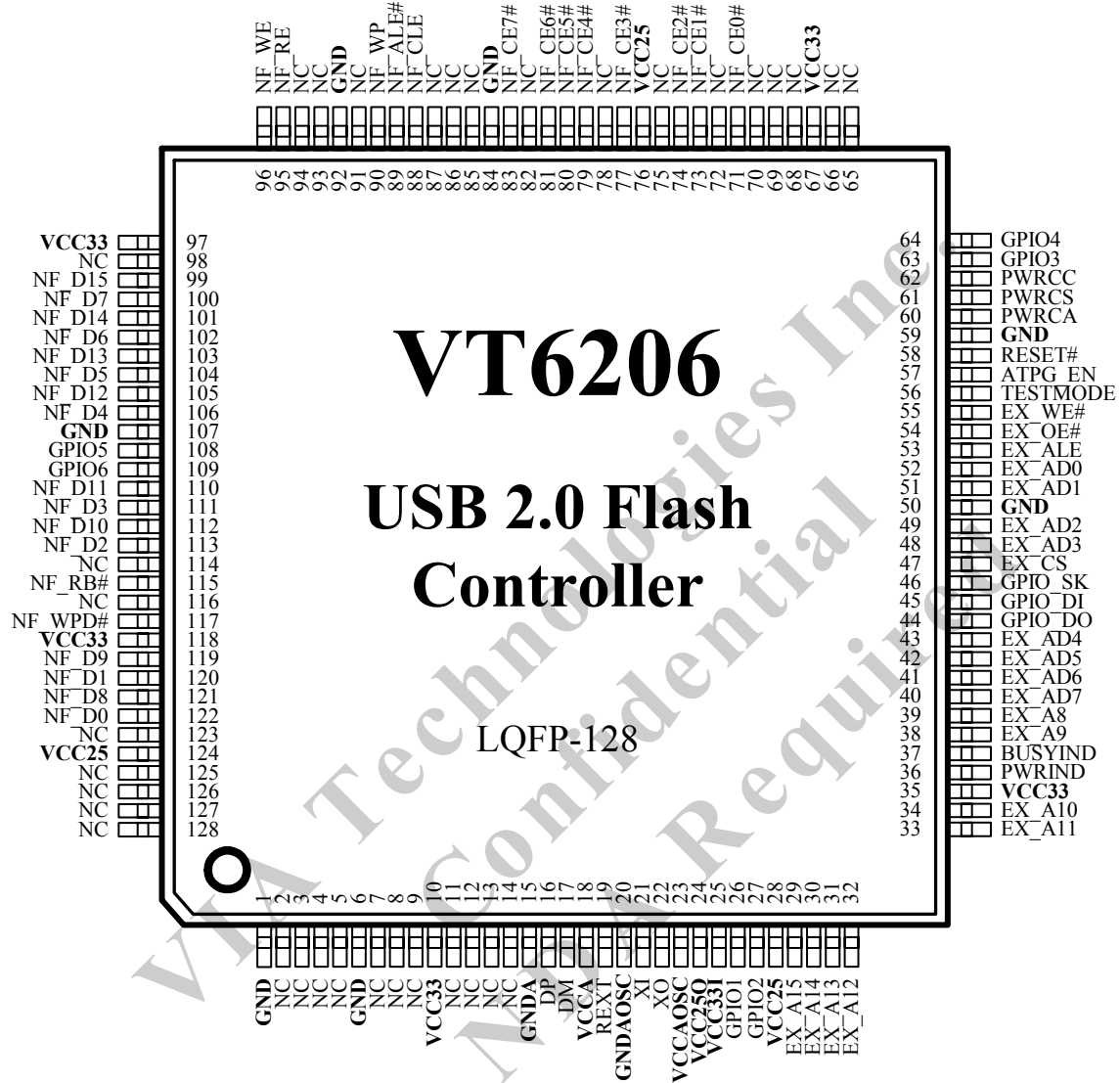
- Abbrev. IF: Interface
- EP: Endpoint
- FIFO: First In / First Out (Buffer)
- EP3 FIFO: It is an 8-byte FIFO for endpoint
- EP0 FIFO: It is used for endpoint0 data transfer.
- MHE: Media Hardware Engine
- SIE: Serial Interface Engine

# PINOUTS

## Pin Diagram



**Figure 2. Pin Diagram for LQFP-48 (Top View)**



**Figure 3. Pin Diagram for LQFP-128 (Top View)**

Pin List
**Table 1. Pin List - 48-pin LQFP (Alphabetical Order)**

Pin Name	Pin#	Type	Pin Name	Pin#	Type
ATPG_EN	18	I	NF_D5	39	B
BUSYIND	15	O	NF_D6	38	B
DM	4	B	NF_D7	37	B
DP	3	B	NF_RB#	44	I
GND	1	P	NF_RE	34	O
GND	16	P	NF_WE	35	O
GND	20	P	NF_WP	33	O
GND	30	P	NF_WPD#	45	I
GND	41	P	PWRCA	21	O
GNDA	2	P	PWRIND	14	O
GNDAOSC	7	P	RESET#	19	I
GPIO3	22	B	REXT	6	I
GPIO4	23	B	TESTMODE	17	I
NF_ALE#	32	O	VCC25	13	P
NF_CE0#	25	O	VCC25	28	P
NF_CE1#	26	O	VCC33	24	P
NF_CE2#	27	O	VCC33	36	P
NF_CE3#	29	O	VCC33	46	P
NF_CLE	31	O	VCC250	11	P
NF_D0	48	B	VCC33I	12	P
NF_D1	47	B	VCCA	5	P
NF_D2	43	B	VCCAOSC	10	P
NF_D3	42	B	XI	8	I
NF_D4	40	B	XO	9	O

## Pin Descriptions

The following table provides a brief description of each signal of VT6206. Pins with dual usage may be listed twice for consistency.

The following abbreviations are used to identify pin types:

B = Bi-directional  
 I = Input  
 O = Output  
 P = Power / Ground  
 PU = Pull-up  
 PD = Pull-down

**Table 2. Pin Descriptions**

NAND Flash Interface					
Signal Name	Pin # (48-pin)	Pin # (128-pin)	Type	Attr	Description
NF_ALE#	32	89	O		<b>Address Latch Enable.</b>
NF_CE[3:0]#	29,27,26,25	77, 74, 73, 71	O		<b>Chip Enable.</b> This is the active low chip enable signal to NF device.
NF_CE[7:4]#		83, 81, 80, 79	O		<b>Chip Enable.</b>
NF_CLE	31	88	O		<b>Command Latch Enable.</b>
NF_D[15:8]		99, 101, 103, 105, 110, 112, 119, 121	B		<b>NF Data 15-8.</b>
NF_D[7:0]	37,38,39,40, 42,43,47,48	100, 102, 104, 106, 111, 113, 120, 122	B		<b>NF Data 7-0.</b> These pins are the bi-directional data signal D7-0 of NF devices.
NF_RB#	44	115	I		<b>Ready/Busy.</b> This pin is connected to the BSY/RDY pin of NF device.
NF_RE	34	95	O		<b>Read Enable.</b>
NF_WE	35	96	O		<b>Write Enable.</b> This pin is an active low write strobe signal for NF device.
NF_WP	33	90	O		<b>Write Protect.</b>
NF_WPD#	45	117	I		<b>Write Protect Detection.</b>

USB Interface					
Signal Name	Pin # (48-pin)	Pin # (128-pin)	Type	Attr	Description
DP	3	16	B		<b>USB Bus Data Plus (USB+).</b> Analog differential data pair for USB 2.0 data transmission.
DM	4	17	B		<b>USB Bus Data Minus (USB-).</b> Analog differential data pair for USB 2.0 data transmission.
REXT	6	19	I		<b>External Resistor.</b>
XI	8	21	I		<b>Crystal Input.</b> May be connected to a 24.000 MHz parallel resonant fundamental mode crystal.
XO	9	22	O		<b>Crystal Output.</b> May be connected to a 24.000 MHz parallel resonant fundamental mode crystal.

External ROM Interface					
Signal Name	Pin # (128-pin)	Type	Attr	Description	
EX_A[15:8]	29-30, 31-34, 38-39	O		<b>Address.</b>	
EX_AD[7:0]	40-43, 48-49, 51-52	B	PD	<b>Address / Data 7-0.</b>	
EX_ALE	53	O		<b>Address Latch Enable.</b>	
EX_OE#	54	O		<b>Output Enable.</b>	
EX_WE#	55	O		<b>Write Enable.</b>	
EX_CS / EE_CS	47	O		<b>Chip Select.</b>	

Serial EEPROM					
Signal Name	Pin # (128-pin)	Type	Attr	Description	
EE_CS / EX_CS	47	O		<b>EEPROM Chip Select.</b> Connect to EECS pin.	
GPIO_DO	44	B/I	PU	<b>EEPROM Data Out.</b> Connect to EEDO pin.	
GPIO_DI	45	B/O	PU	<b>EEPROM Data In.</b> Connect to EEDI pin.	
GPIO_SK	46	B/O	PU	<b>EEPROM Clock.</b> Connect to EESK pin.	

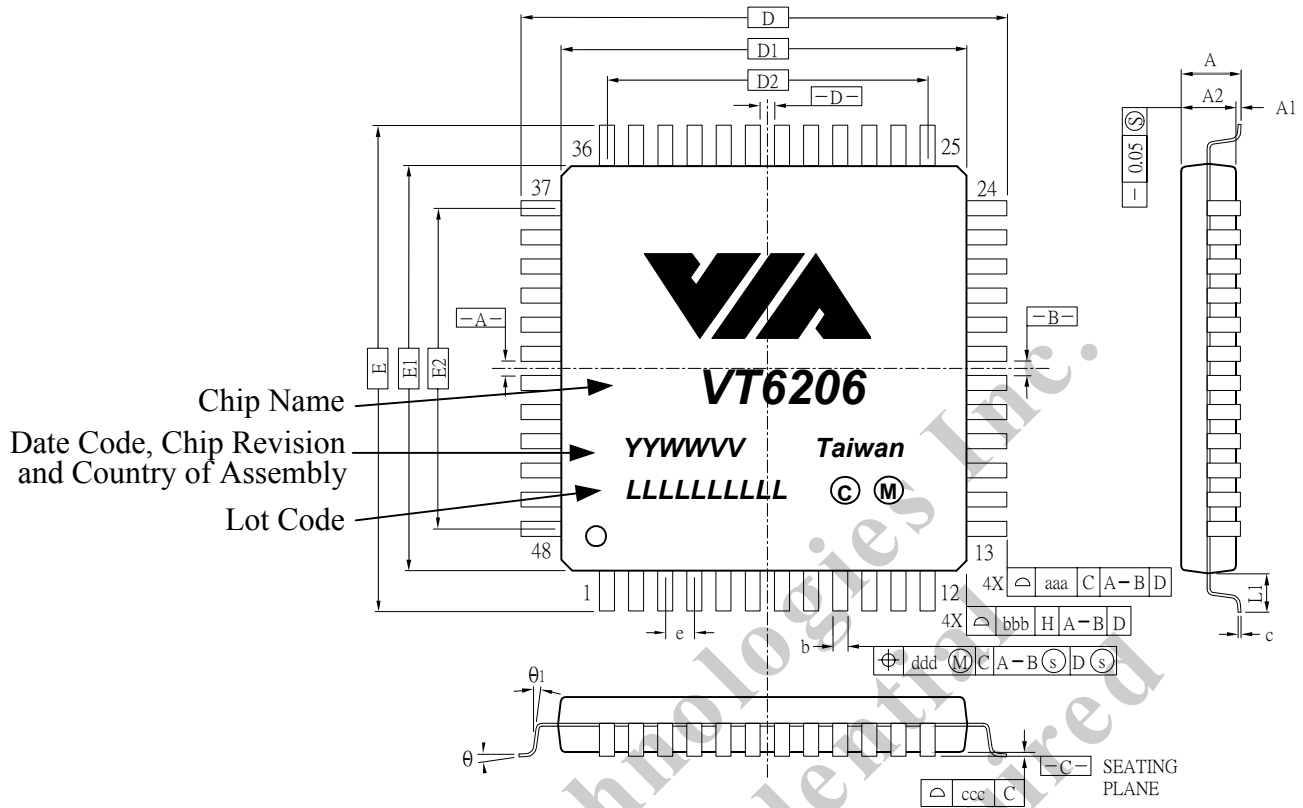
TEST Pins					
Signal Name	Pin # (48-pin)	Pin # (128-pin)	Type	Attr	Description
ATPG_EN	18	57	I	PD	<b>Automatic Test Program Generator Enable.</b> Do not connect for normal operation.
TESTMODE	17	56	I	PD	<b>Test Mode Enable.</b> This pin is used for testing the chip. Do not connect for normal operation.

General Purpose I/O and Miscellaneous					
Signal Name	Pin # (48-pin)	Pin # (128-pin)	Type	Attr	Description
<b>GPIO[6:1]</b>		109, 108, 64, 63, 27, 26	B	PU	<b>General Purpose I/O 6-1.</b>
<b>GPIO[4:3]</b>	23,22		B	PU	<b>General Purpose I/O 4-3.</b> These pins may be used either as input, edge sensitive interrupt input, or output.
<b>PWRC[C:A]</b>		62, 61, 60	O		<b>Power Switch Control C-A.</b>
<b>PWRCA</b>	21		O		<b>Power Switch Control A.</b>
<b>BUSYIND</b>	15	37	O		<b>Busy Indicator.</b>
<b>PWRIND</b>	14	36	O		<b>Power Indicator.</b>
<b>RESET#</b>	19	58	I	PU	<b>External Chip Reset.</b>

No Connect					
Signal Name	Pin # (128-pin)	Type	Attr	Description	
NC	2-5, 7-9, 11-14, 65-66, 68-70, 72, 75, 78, 82, 85-87, 91, 93-94, 98, 114, 116, 123, 125-128	—	—	<b>No Connected.</b>	

General Purpose I/O and Miscellaneous					
Signal Name	Pin # (48-pin)	Pin # (128-pin)	Type	Attr	Description
<b>VCC25</b>	13,28	28, 76, 124	P		<b>Internal Logic Power.</b> 2.5±5%.
<b>VCC33</b>	24,36,46	10, 35, 67, 97, 118	P		<b>Digital I/O Power.</b> 3.3V±100mV.
<b>VCC250</b>	11	24	P		<b>Regulator Power Output:</b> 3.3V.
<b>VCC33I</b>	12	25	P		<b>Regulator Power Input:</b> 2.5V.
<b>VCCA</b>	5	18	P		<b>Analog Power.</b> 3.3V
<b>VCCAOSC</b>	10	23	P		<b>Oscillator Power/Core Power.</b> Connect to quiet 2.5V ±5% power source.
<b>GND</b>	1,16,20,30,41	1, 50, 84, 107, 6, 59, 92	P		<b>Ground.</b>
<b>GND A</b>	2	15	P		<b>Analog Ground.</b>
<b>GND AOSC</b>	7	20	P		<b>Oscillator Analog Ground.</b> Connect to analog ground plane.

## PACKAGE MECHANICAL SPECIFICATIONS



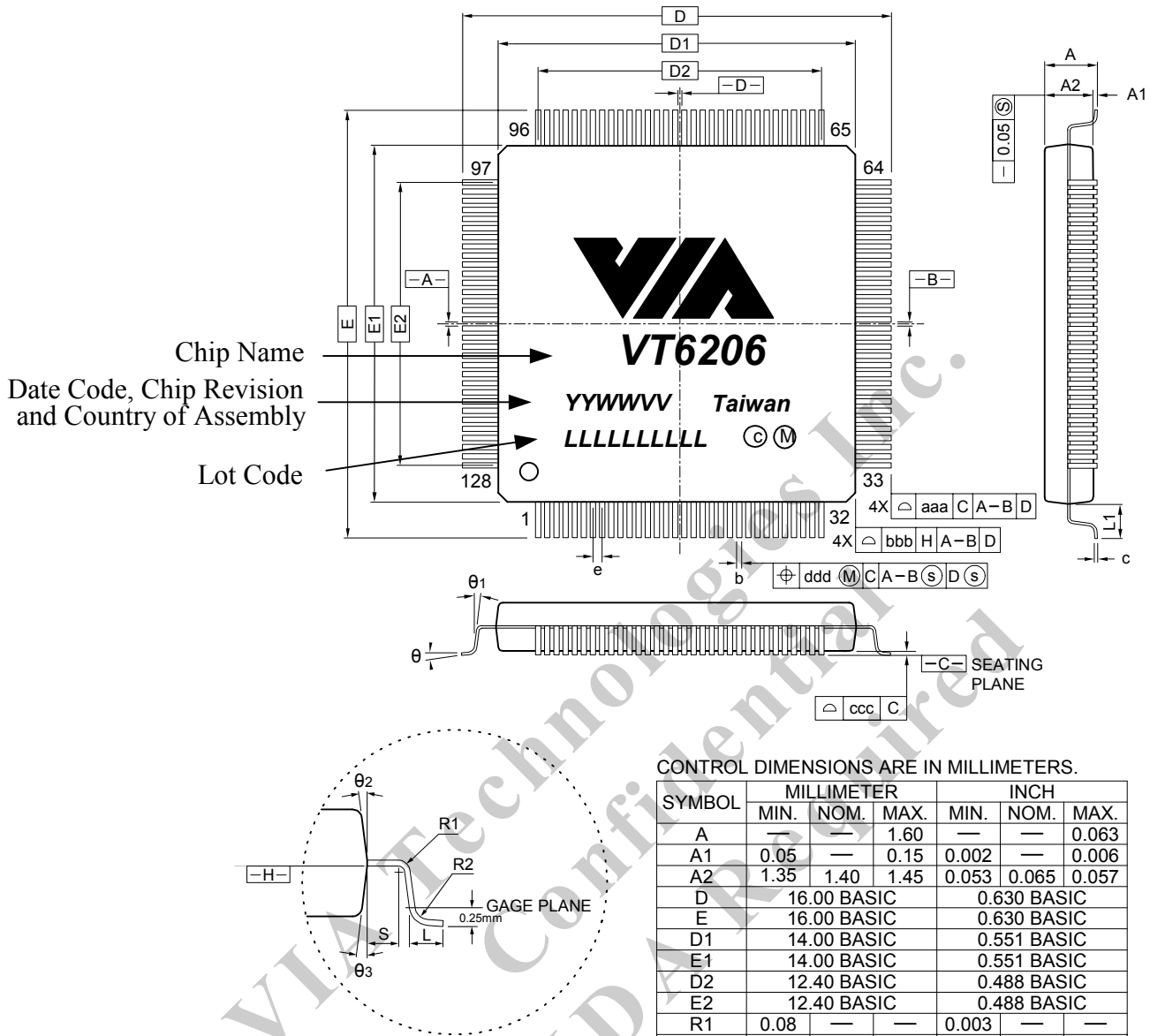
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
$\theta$	0 $\square$	3.5 $\square$	7 $\square$	0 $\square$	3.5 $\square$	7 $\square$
$\theta_1$	0 $\square$	—	—	0 $\square$	—	—
$\theta_2$	11 $\square$	12 $\square$	13 $\square$	11 $\square$	12 $\square$	13 $\square$
$\theta_3$	11 $\square$	12 $\square$	13 $\square$	11 $\square$	12 $\square$	13 $\square$
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 4. Mechanical Specification – 48-pin LQFP Pack



Chip Name  
Date Code, Chip Revision  
and Country of Assembly  
Lot Code

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.065	0.057
D	16.00 BASIC			0.630 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	12.40 BASIC			0.488 BASIC		
E2	12.40 BASIC			0.488 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
theta	0	3.5	7	0	3.5	7
theta1	0	—	—	0	—	—
theta2	11	12	13	11	12	13
theta3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BASIC			0.016 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 5. Mechanical Specification – 128-pin LQFP Pack