



Never
stop thinking



HiPAC™

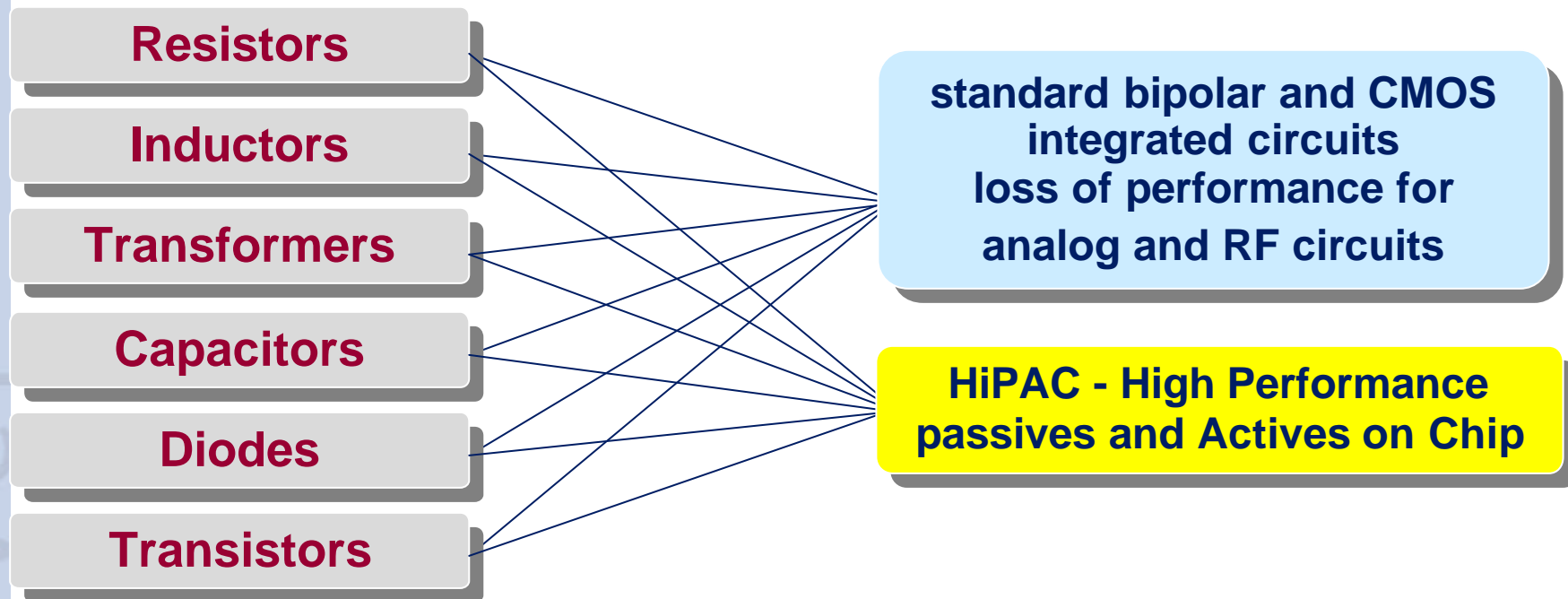
High Performance
Actives & Passives on Chip



Passive Integration on Silicon – Solutions & Target

Components to be integrated

Solutions

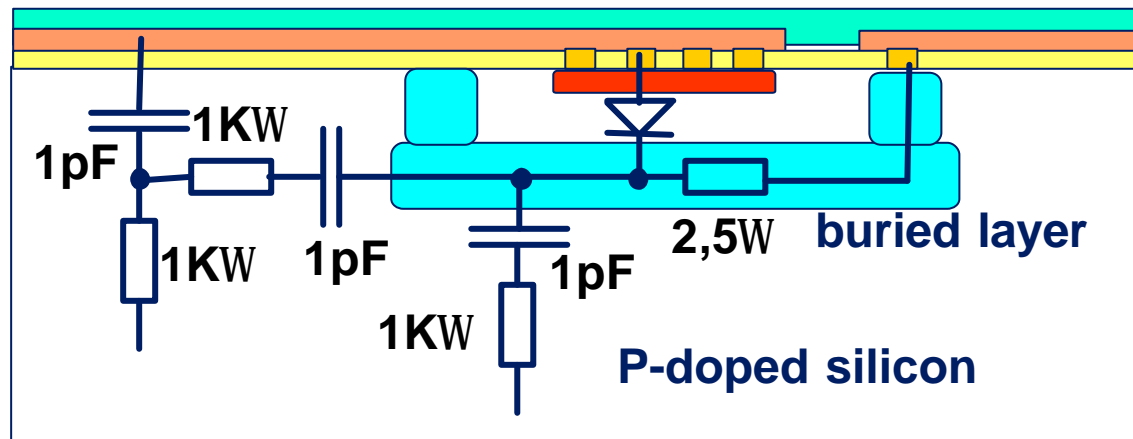


Target HiPAC:

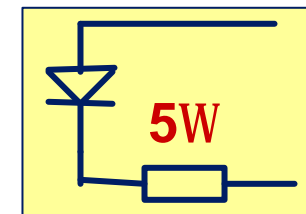
Integration of today's discretes without loss of performance

stop thinking
Never

Integration of RF Diodes with Standard Bipolar Process



@ $f > 100$ MHz:



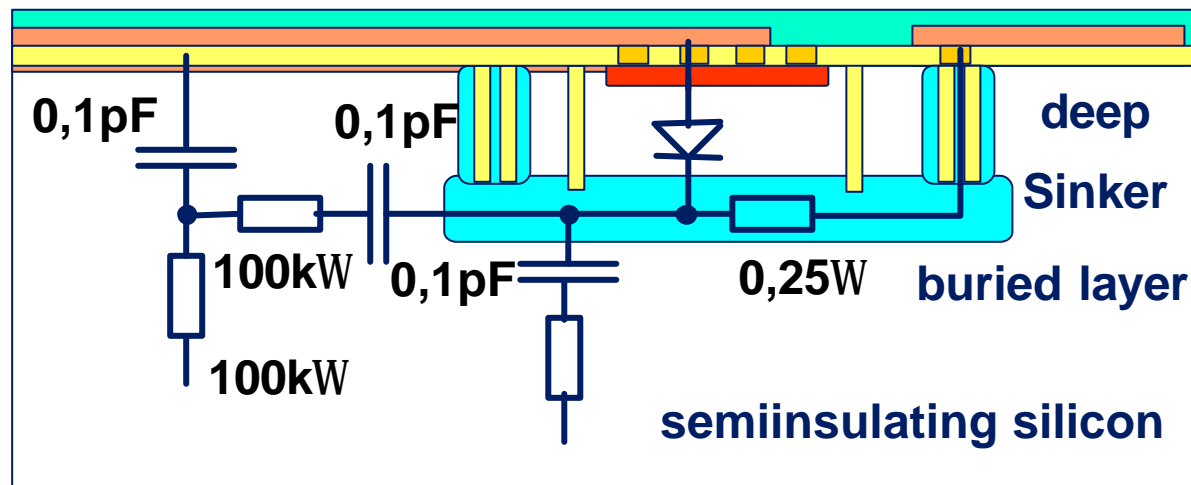
Q = 10 in 50W circuits

Limitations

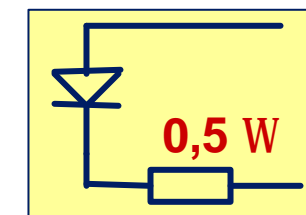
- High series resistance of diode
 - Additional parasitics
- ⇒ Loss of RF performance

Never stop thinking

Integration of RF Diodes with Enhanced HiPAC Process



@ $f > 100\text{MHz}$:



$Q = 100$ in 50W circuits

Advanced technology issues

- semiinsulating silicon with much lower parasitics
- optimized buried layer technology with deep sinker providing very low series resistance

⇒ No loss of RF performance in HiPAC technology

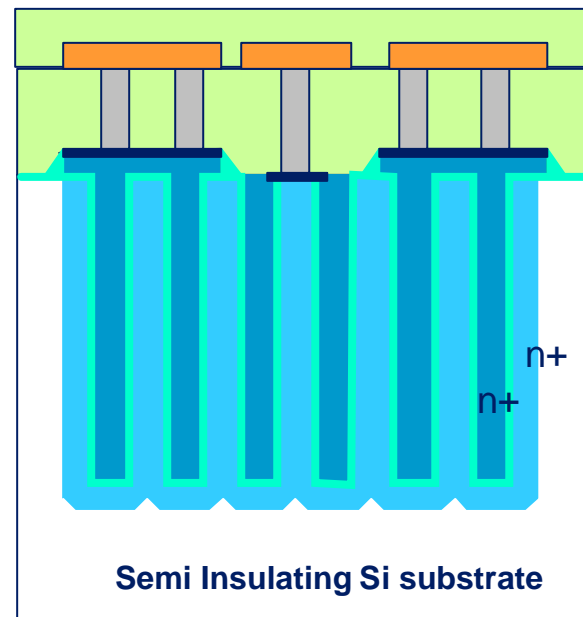
Integration of Capacitors with Enhanced HiPAC Process

High Frequency

- medium value 0,1-200pF
- 10% Tolerance
- 6 μ trench 120V
Q=100@1GHz

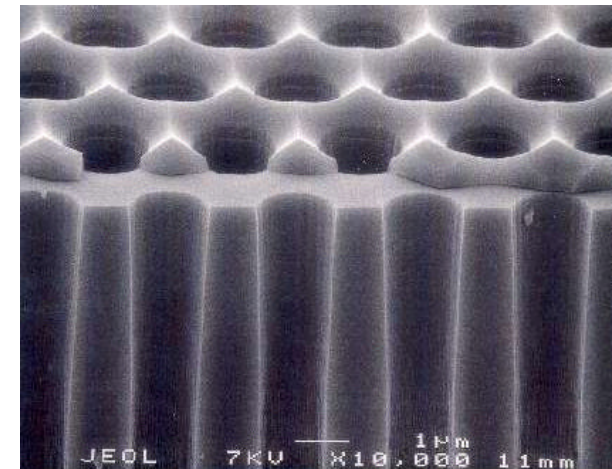
Low Frequency

- Low frequency, high value 0.1-10nF
- 15% Tolerance
- 18 μ trench 30V
Q=200@10MHz



Silcaps

=Silicon capacitor



Integration of Capacitors with Enhanced HiPAC Process

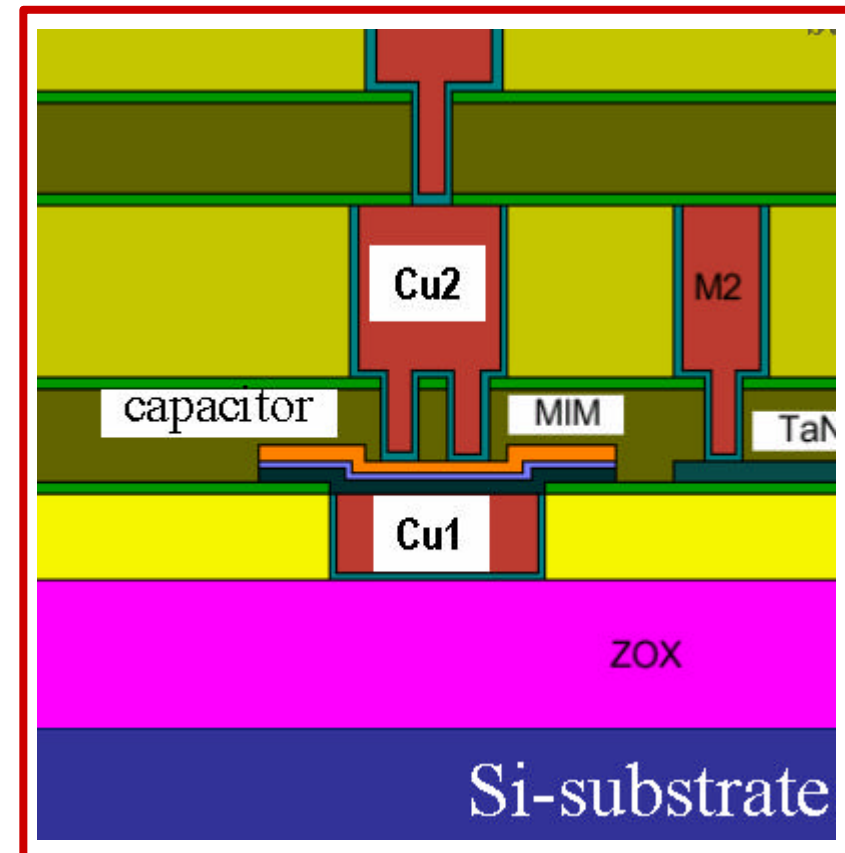
High Frequency

- small value 0,1- 10pF
- 5% Tolerance
- 60V , Q=100@1GHz

MIM ALD Caps

=Metal Insulator Metal

=Atomic Layer Deposition

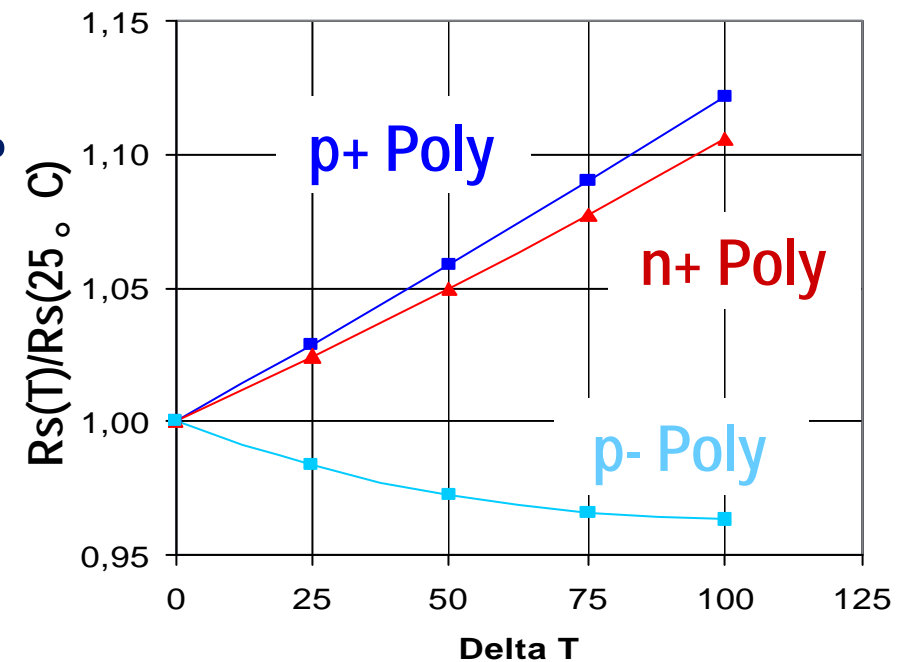


Integration of Resistors with Enhanced HiPAC Process

Technologies in use	Resistivity W/square	Tolerance %	Temperature dependance ppm/K
Poly Si lightly doped	1000	5%	-400
Poly Si medium doped	440	5%	±100
Poly Si highly doped	90	5%	1200
TaN	20	10%	±50

Standard technologies

- tight difference tolerance <0,5%
- 5% Tolerance

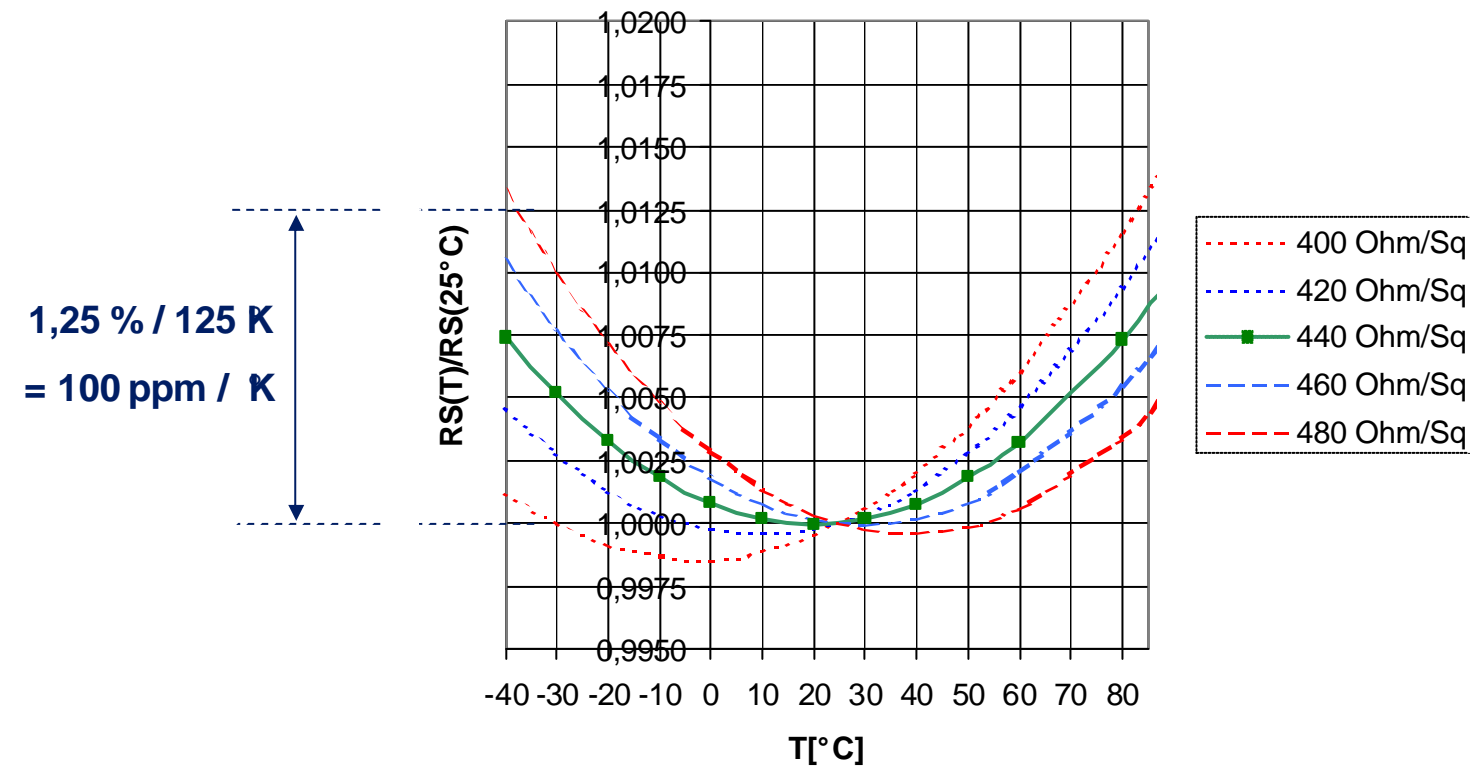


Integration of Resistors with Enhanced HiPAC Process

Temperature compensated poly silicon resistors

- tight difference tolerance <0,5%
- 5% Tolerance

Temperature Dependence

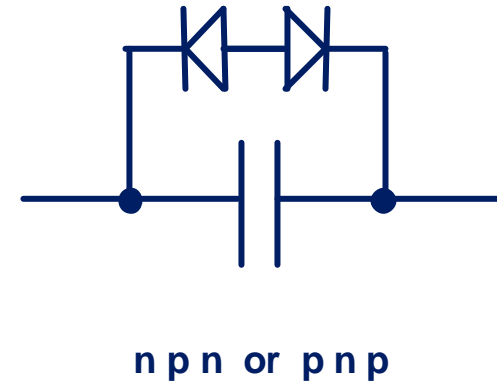
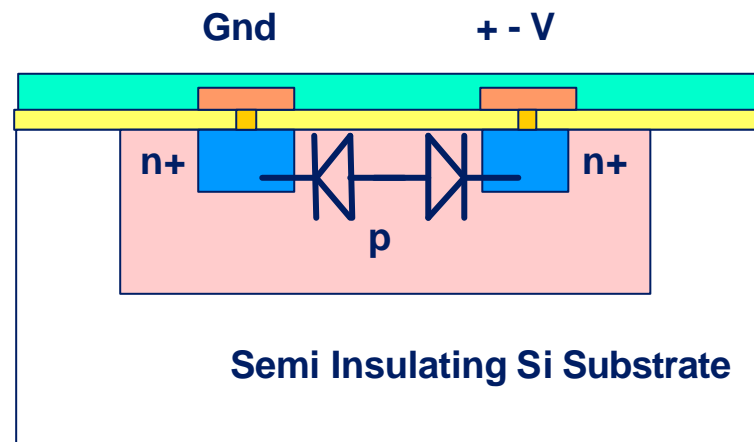


ESD Sensitivity of Integrated Passives

ESD pulse 15KV = 50ns 50A	SilCap 1 nF / 100pF	MIM Cap 10 / 1 pF	Resistor 5 / 1000 Ohm	Coil 5 / 50 nH
Vmax	30 V / 120 V	30V	500 V	500 V
I _{max} (50ns)	10 A	1 A / 0,1 A	6 A / 0,5A	30 A / 30 A

Integrated passives are more sensitive
 to ESD damage than discrete passives
 In most applications they need protection

Improving ESD Hardness with Enhanced HiPAC Protection Devices

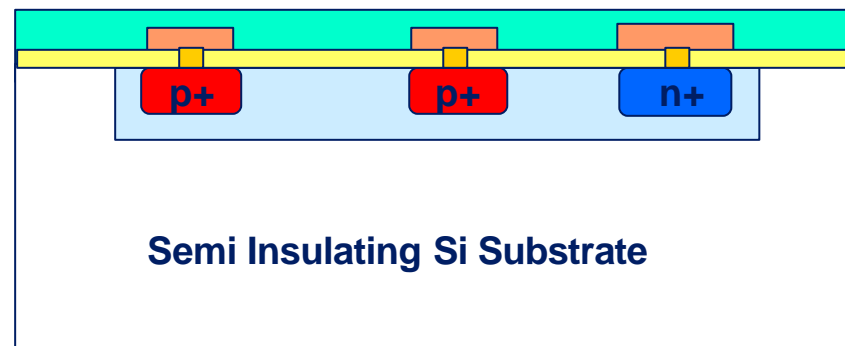


ESD Double Diodes $V_{\sim} = 5V / 14V$ $V_{clamp} = 20V / 30V$

- ESD Source IEC 64k, 15KV, 330W, 150pF
- $C_j = 10pF / 20 pF$ voltage dependent
- Protection of AF data lines and Vcc
- No Bias required

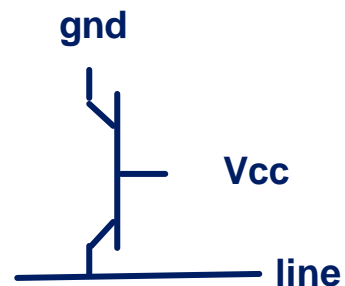
Improving ESD hardness with enhanced HiPAC protection devices

ESD Protection Transistors $V_{\sim} = 25V$ $f > 1MHz$ $V_{clamp} = 75V$



Semi Insulating Si Substrate

n p n or p n p



ESD Source IEC 64k
15KV, 330Ω, 150pF

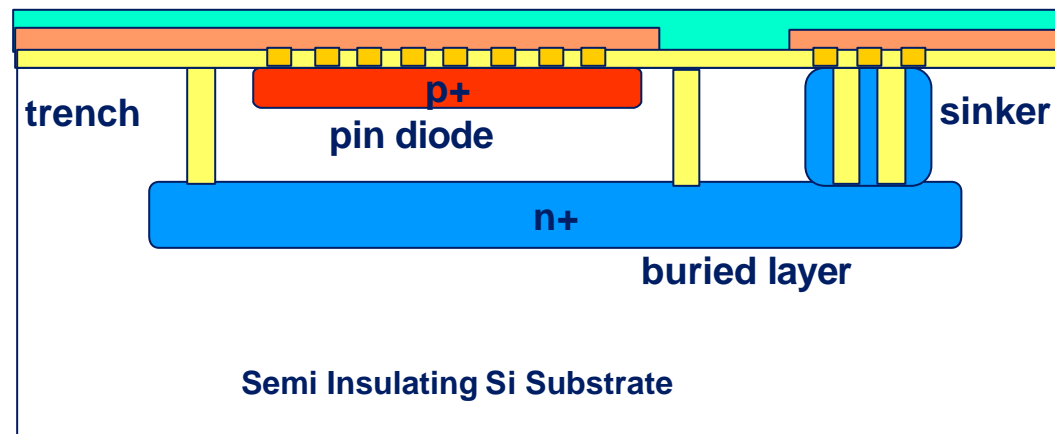
$C_j = 2pF$

Protection of
high speed data lines
up to 1GHz

$IP3 > 70dbm$ with
2.8V bias

Improving ESD Hardness with Enhanced HiPAC Protection Devices

ESD Protection PIN-Diode pair $V_{\sim} = 25V$ $f > 10MHz$ $V_{clamp} = 15V$

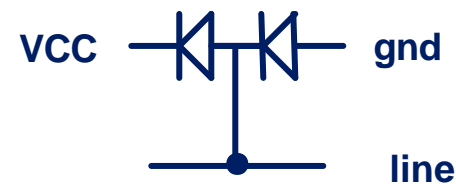


ESD Source IEC 64k
15KV, 330Ω, 150pF

$C_{line} = 0,2pF$

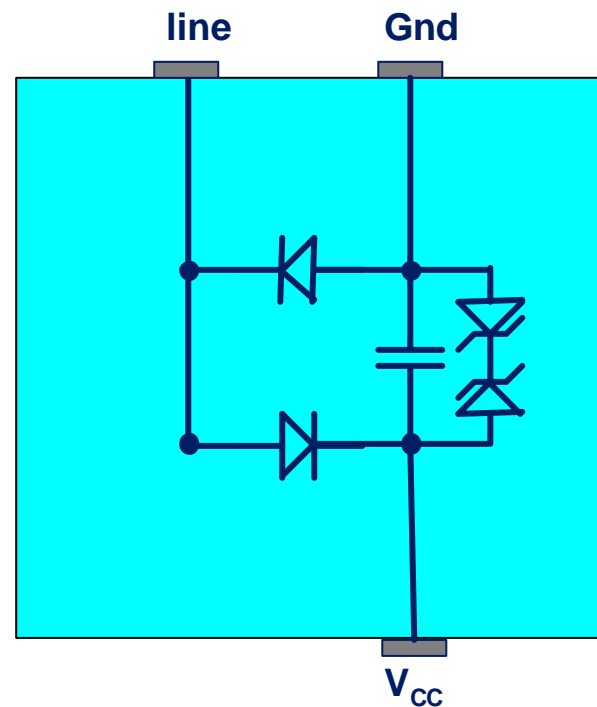
Protection of
high speed data lines
up to 5GHz

IP3 >70dbm with
2.8V positive Bias



Improving ESD Hardness with Enhanced HiPAC Protection Devices

PIN-Diodepair combined with Double Diode



ESD Source IEC 64k
15KV, 330Ω, 150pF

$C_{line} = 0,2pF$

Protection of
high speed data lines
up to 2,5 GHz

IP3 >70dbm with
2.8V positive Bias



Summary of Technology Features

- low tolerance resistors, 20Ω - $200k\Omega$
 $\pm 4\%$ tolerance, $\pm 1\%$ matching
- high capacitance area ratio, $\sim 20\text{fF} / \mu\text{m}^2$
C values up to 100nF , tolerance $\pm 10\%$
low leakage current $< \text{nA}$
- inductors up to $100\text{nH} \pm 2\%$
Q - values 20-40 @2GHz
high current capabilities
- PIN -, Schottky -, Zener diodes
- transistors



Customer Benefits and Target Applications

Target

- component count reduction
- improved overall quality level
- cost reductions
- board space reduction

Applications

- low cost high performance filters
- ESD/EMI protection at reasonable costs
- passive networks providing cost and size optimization
- high performance switching devices
- balun functionality

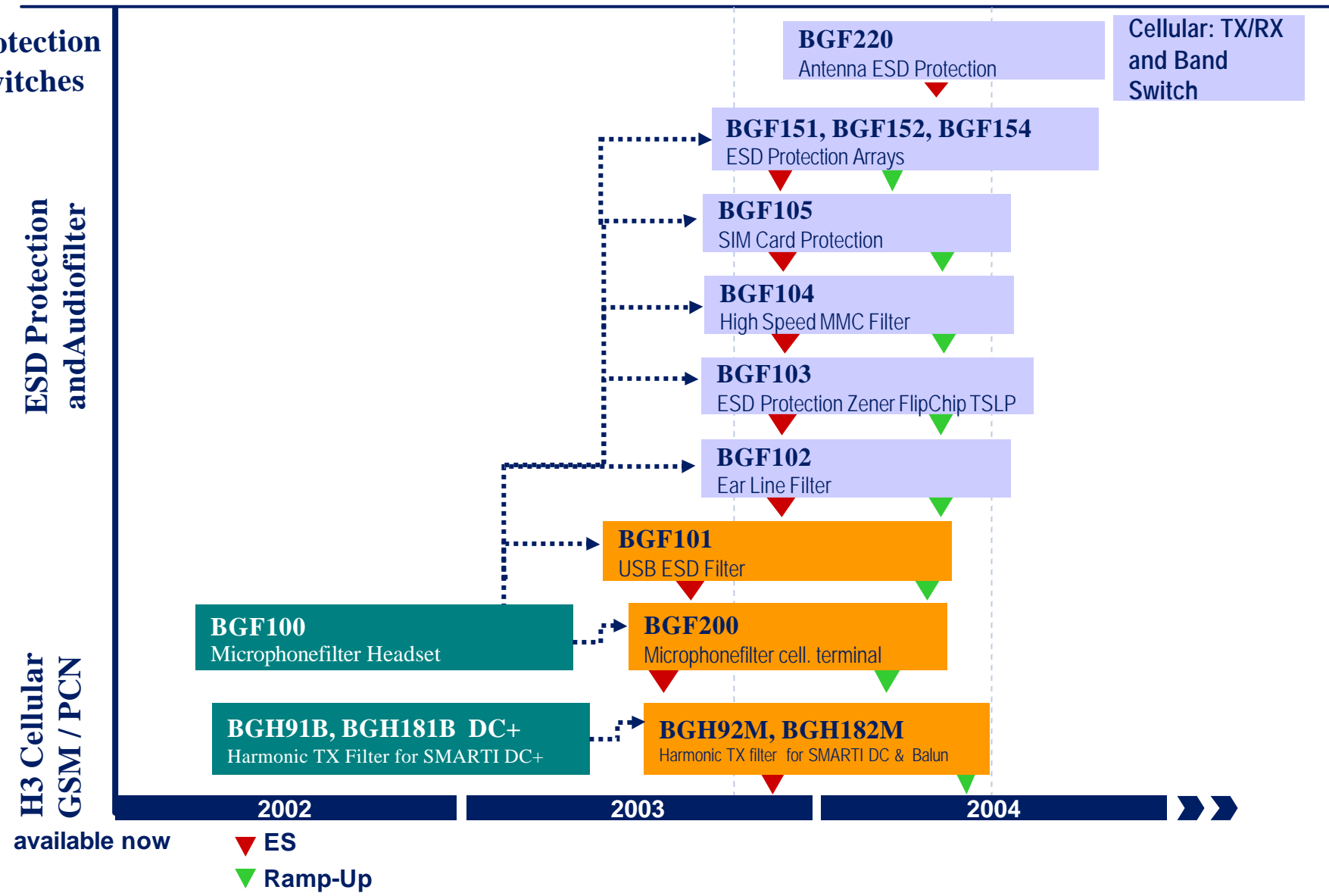


HiPAC-Filters, Switches & ESD protection

RF-Protection
& Switches

ESD Protection
and Audiofilter

H3 Cellular
GSM / PCN



HiPAC for Cellular Phones

Customers

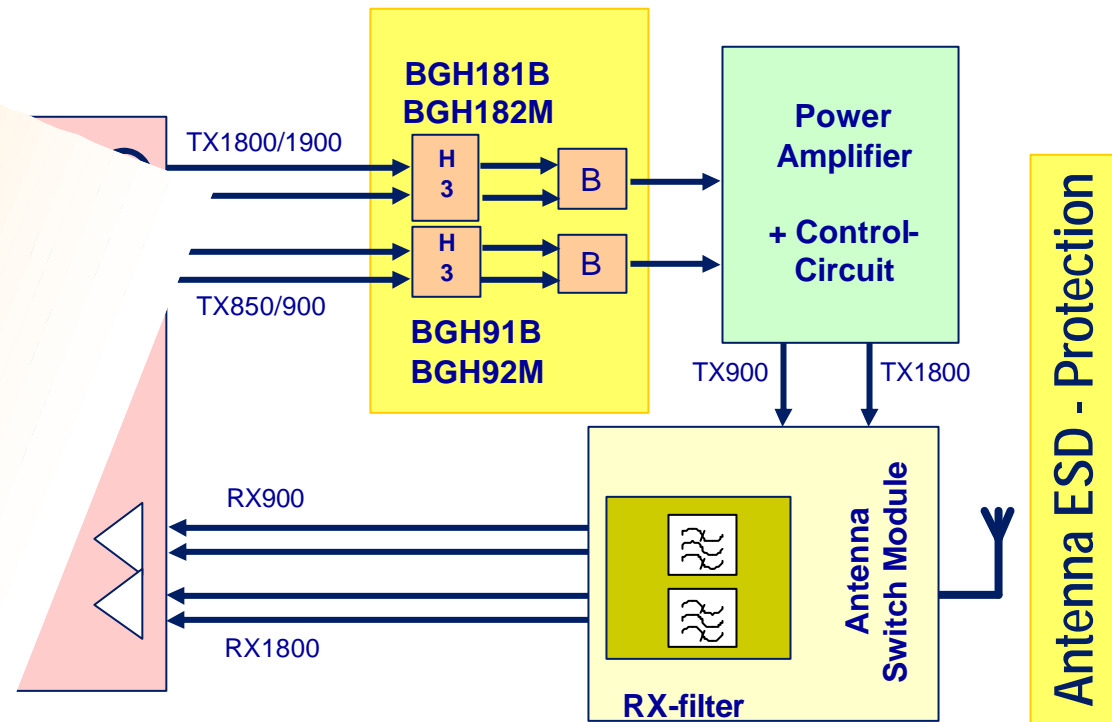
- Nokia
- Motorola
- ICM
- Sony-Ericsson

RF Applications

- H3 Filter
- Antenna ESD

AF Applications

- Microphone
- keypad
- SIM Interface
- earphone
- data connector
- passive networks



- protection against ESD
- filtering of unwanted RF-signals
- passive networks



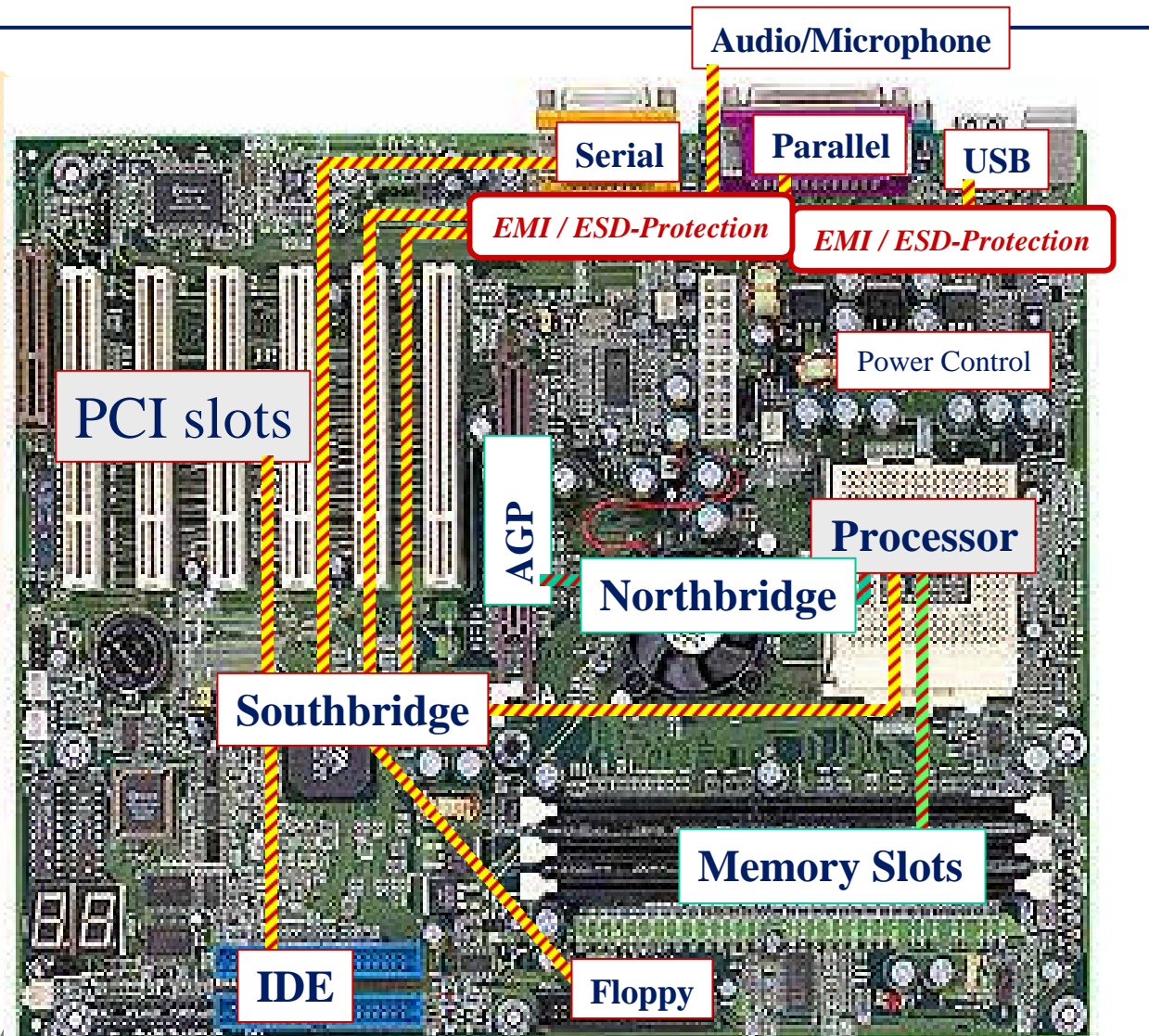
HiPAC for PC & Peripherals

Customers

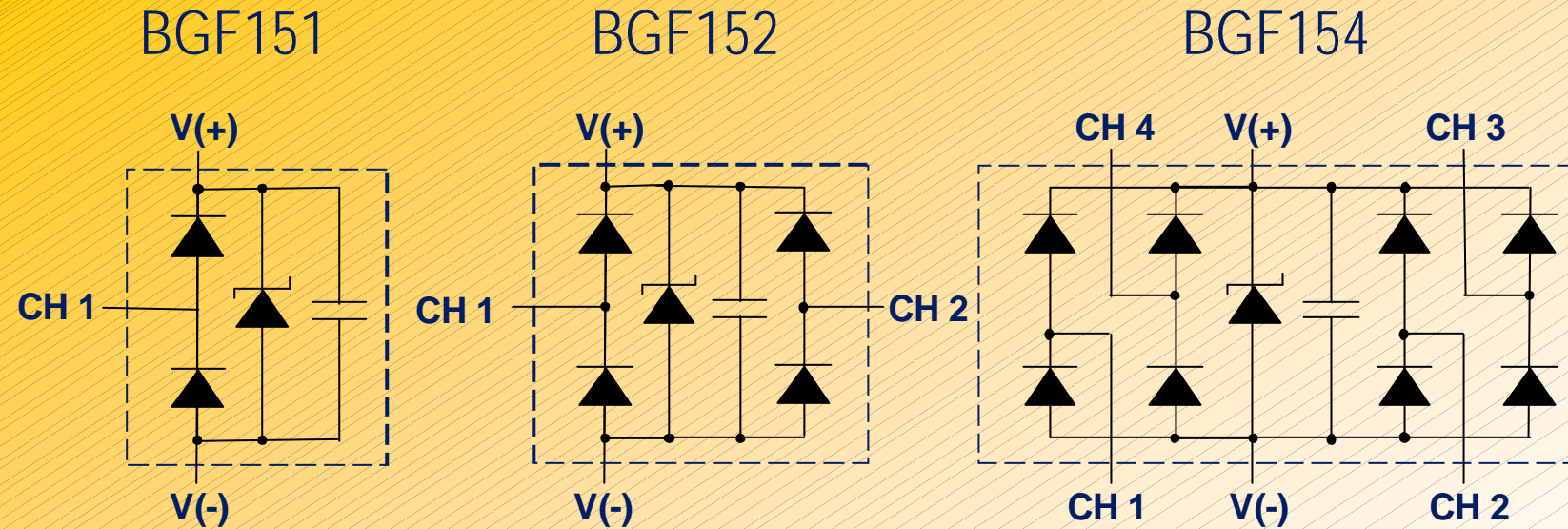
- HP
- Dell
- Intel
- IBM

Applications

- USB 2.0
- IEEE1394 Firewire
- Serial ATA
- DVI
- High-speed data line ESD protection



1,2,4 Channel ESD Protection Arrays



Applications

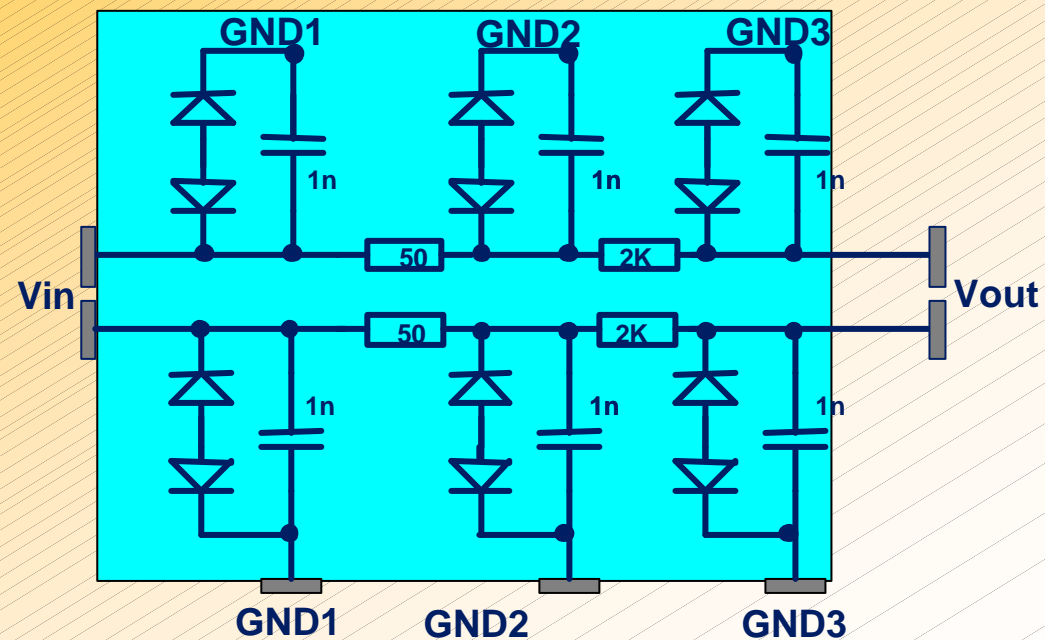
- USB 2.0
- IEEE 1394 Firewire®
- DVI
- Serial ATA
- g. p. high speed data line

Features

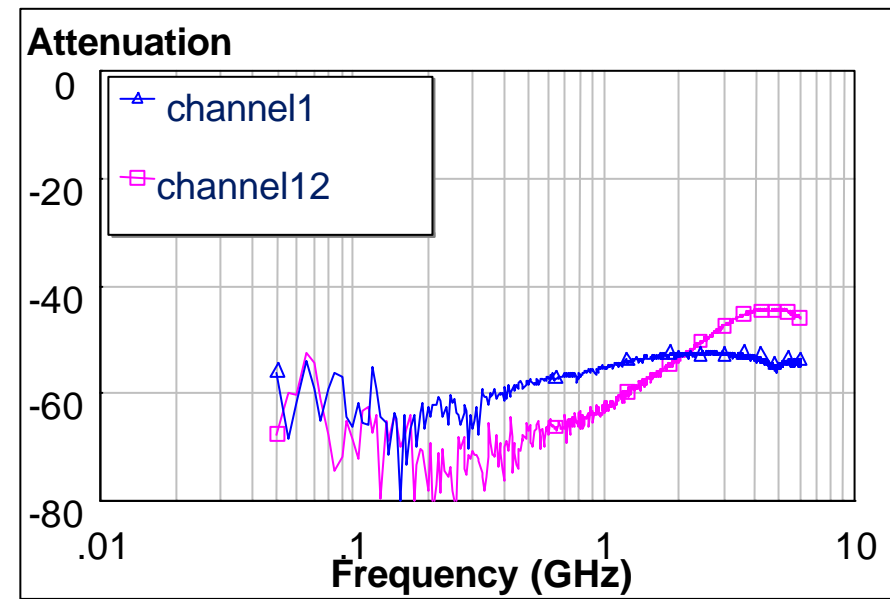
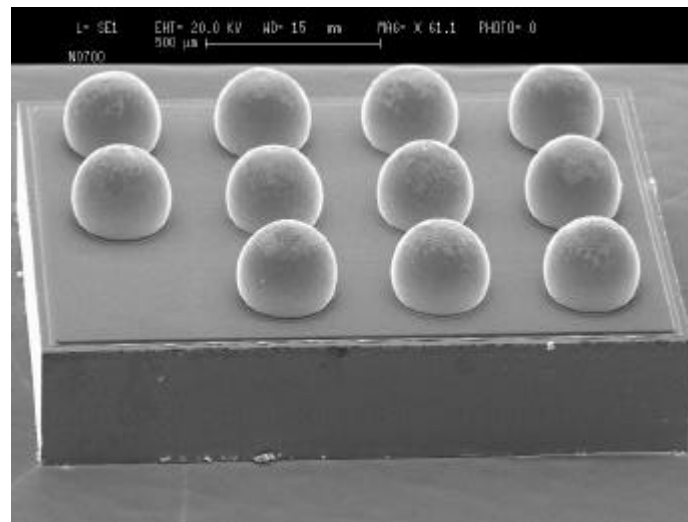
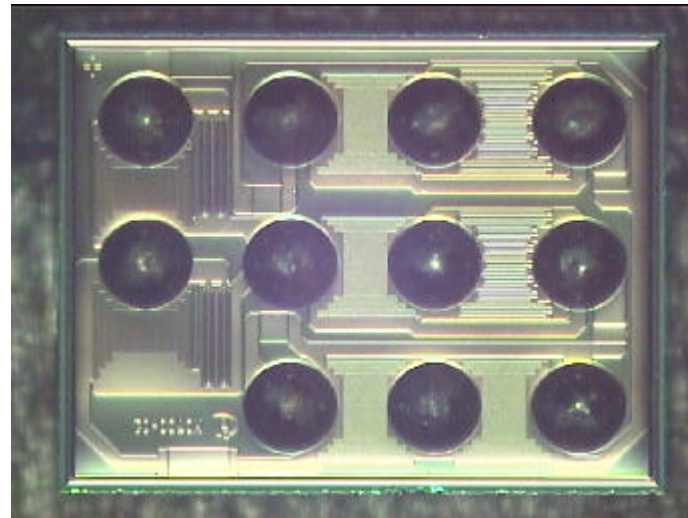
- up to ± 15 kV ESD protection
- low loading capacitance < 1 pF
- 1 channel BGF151 in SOT23
- 2 channel BGF152 in SOT 143
- 4 channel BGF154 in SOT 363

BGF100 Microphone Filter

- 15KV ESD-protection and low pass filter circuit with ESD diodes, R's and C's
- Attenuation: - 44dbm @ 6GHz



BGF100 Microphone Filter



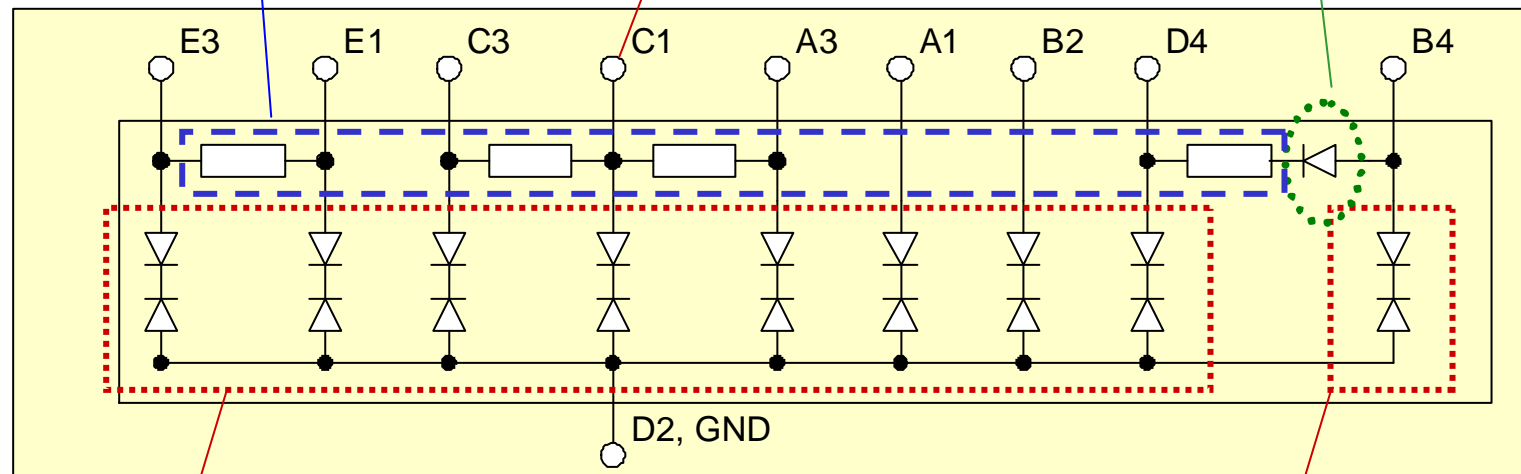
USB ESD Protection BGF101 Schematic

Circuit and Device Specs:

Low TK Resistors
TCR < 100 ppm/K
 $\pm 5\%$

$C_{line} < 50$ pF,
target 40 pF

Schottky Diode
< 0.3 V @ 10 nA



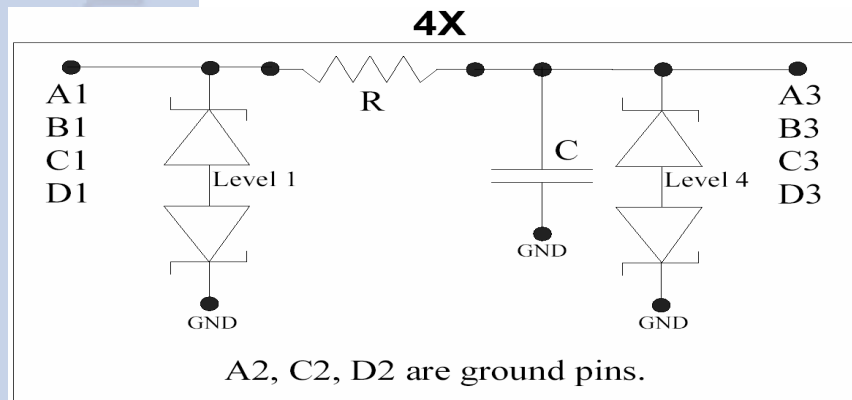
15kV ESD Stability
 $U_{BD} = 7V @ 1mA$
 $I_L < 100nA @ 3V$

2 kV
 $U_{BD} = 7V @ 1mA$
 $I_L < 100nA @ 3V$

stop thinking
Never



Ear Line Filter BGF102 Spec Request



Resistors

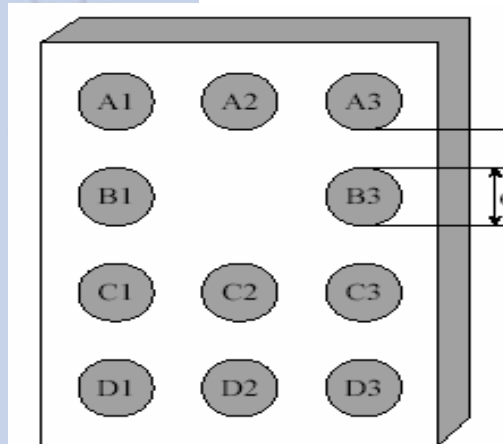
Values	10 Ω
Tolerance	$\pm 30\%$

Zeners

Breakdown voltage	Min. 14V
Capacitance	30 pF

Capacitors

Values	5 nF
Tolerance	$\pm 20\%$



New type of S-WLP-11 package

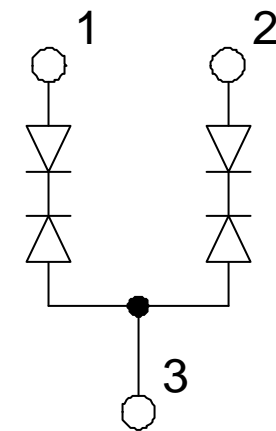
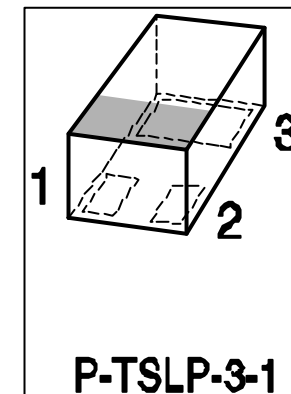
Problem

1. 4 x 5 nF need too much die area, even in P7MI Options (increased C-density)
2. Thus price would be 60% over BGF100!



ESD Protection Diodes BGF103 Performance

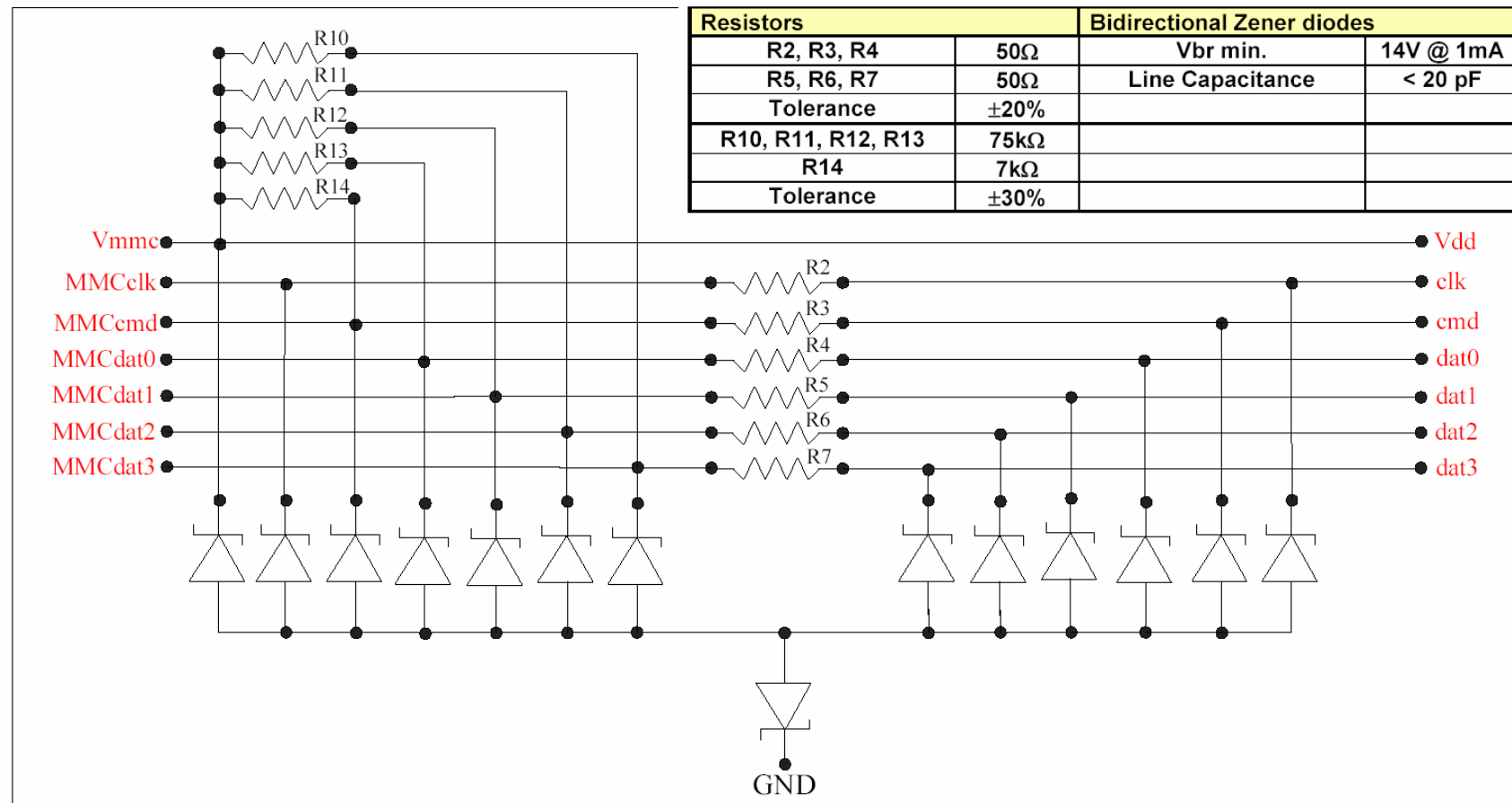
- Cline 10 pF
- ESD 15 kV
- Vbr min ± 14 V
- Leakage current < 100 nA @ 3 V
- First samples feasible in March 2003





High Speed MMC Interface Filter BGF104

NMP Spec



NMP Concept: Common base configuration

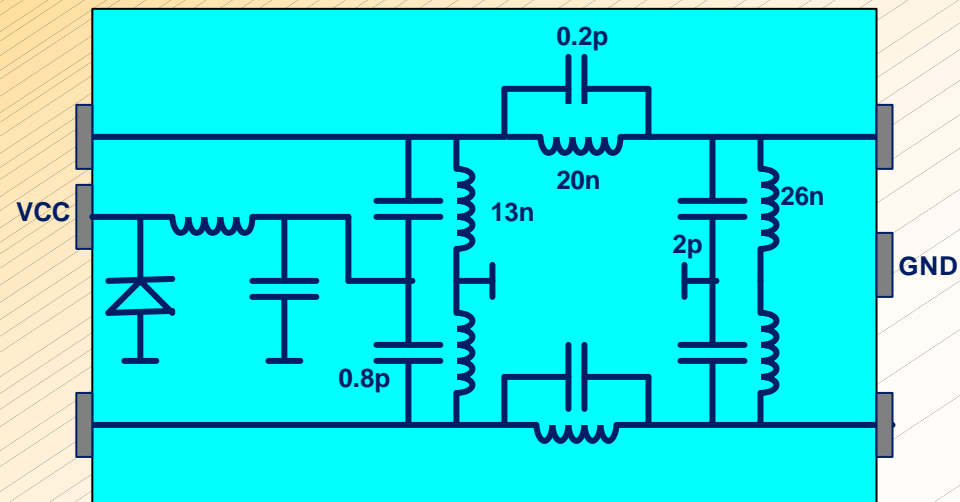
H3 (SiICu) - Filter for Mobile Applications

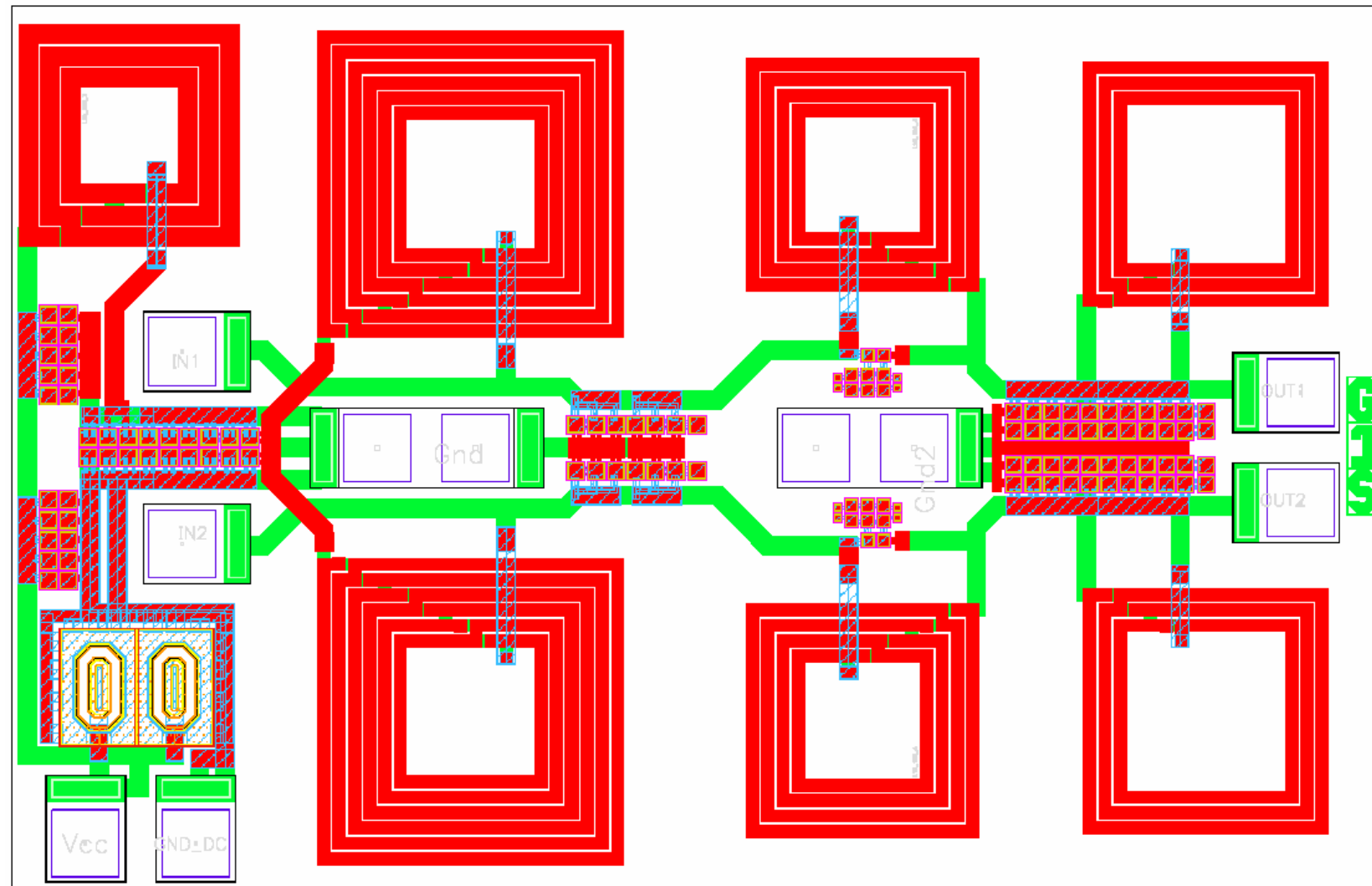
Band pass filter circuit with 1KV ESD protection

- zener diodes , L's and C's

Targets

- replace lowend SAW-filters
higher input power levels compared to SAWs (max. 15dBm)
- replace SMD filter to reduce SMD-partcount





Measurement Results of BGH91B - TX H3-Filter for GSM900

