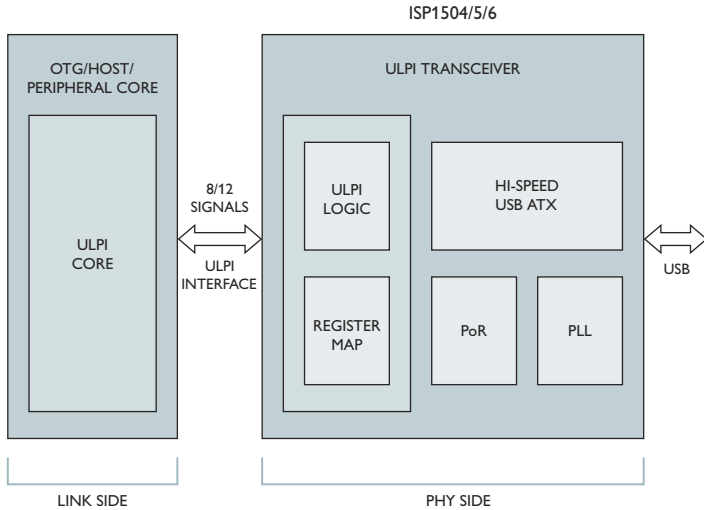


ISP1504, ISP1505, ISP1506

Designed for use with ASICs, FPGAs, and SoCs that have on-board support for Hi-Speed USB, the ISP150x family complies with the ULPI specification to deliver complete analog transceiver functionality in very small, low-pin-count packages.



Key Features

- Fully compliant with
 - Universal Serial Bus Specification Revision 2.0
 - On-The-Go Supplement to the USB Specification Revision 1.0a
 - UTMI+ Low Pin Interface (ULPI) Specification Revision 1.0
- Highly-optimized ULPI transceivers for use with Hi-Speed USB host, peripheral, and OTG cores
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) data transfer rates
- Integrate all USB and OTG analog circuitry (built-in PLL)
- Flexible power supply input of 3.0V to 4.5V
- Independent I/O voltage input of 1.65V to 3.6V
- ISP1504, ISP1506: Internal support for V_{BUS} charge pump regulator
- Integrated resistors 45- Ω high-speed terminations, 1.5-k Ω full-speed device pull-up, and 15-k Ω host terminations
- HVQFN32 (5x5 mm²) or HVQFN24 (4x4 mm²) package

ULPI transceivers for use with Hi-Speed USB host, peripheral, and OTG cores



The ISP1504, ISP1505, and ISP1506 are the first in a family of Hi-Speed Universal Serial Bus (USB) transceivers designed for use with Application-Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs) or System-on-Chips (SoCs) that incorporate a macrocell for Hi-Speed USB host, peripheral, or On-The-Go (OTG) functionality. Meeting Level 3 requirements of the USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Specification Rev. 1.0, ISP150x transceivers provide the analog USB Phy functionality necessary for the digital USB Link in an ASIC, FPGA, or SoC to connect to a Hi-Speed USB peripheral, host, or dual-role OTG device.

The ISP150x family has been verified by major IP vendors to be completely free of interoperability problems and is well suited to consumer electronics applications such as set-top boxes, MP3 players, and digital still cameras, as well as mobile phones.

In compliance with the UTMI+ Low Pin Interface (ULPI) specification, ISP150x transceivers are available in very small, low-pin-count packages that save board space. They support high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) data rates.

The ISP150x architecture includes a highly optimized, ULPI-compliant interface that operates at 60 MHz and uses only eight or twelve signals between the core and the transceiver. An integrated Phase-Locked Loop (PLL) supports a 60-MHz input clock as well as a crystal or clock frequency of 12, 13, 19.2, or 26 MHz. The architecture also includes a fully reprogrammable, ULPI-compliant register set and there is an internal power-on reset circuit.

Each ISP150x transceiver has resistors that support 45- Ω high-speed terminations, 1.5-k Ω full-speed device pull-up, and 15-k Ω host terminations.

	ISP1504	ISP1505	ISP1506
Embedded charge pump	Yes	No	Yes
Digital I/O interface	1.65 to 3.6 V	1.65 to 3.6 V	1.65 to 1.95 V
OTG support	Full	SRP	Full
Link-to-Phy pins	12	12	8
Data bus	8-bit	8-bit	4-bit
Packaging	32 pins	24 pins	24 pins

ISP1504, ISP1505, ISP1506

ULPI transceivers for use with Hi-Speed USB host, peripheral, and OTG cores



The transceivers also support bus reset, suspend, resume, and high-speed detection handshake (chirp).

To save power, the suspend current is less than 100 μA and the operating current is less than 50 mA. The input power supply ranges from 3.0 V to 4.5 V. A built-in voltage regulator supplies 3.3 V or 1.8 V.

An integrated V_{BUS} charge pump regulator outputs voltage between 4.4 V and 5.25 V at a current of up to 50 mA and can be tuned using an external capacitor. The transceivers also support an external charge pump or a 5 V supply.

ISP1504 for OTG portable and standalone systems

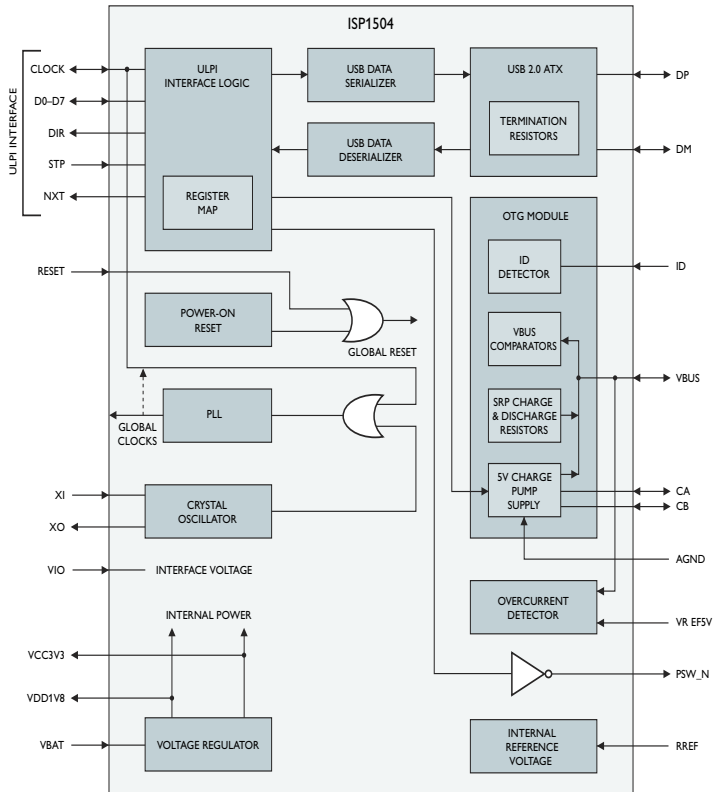
The ISP1504 interfaces to host, peripheral, and dual-role OTG device cores. It is ideal for use in portable devices or systems with a built-in USB OTG dual-role device core. It uses an eight-bit, bidirectional parallel data interface that is compliant with the ULPI Rev. 1.0 specification. The Link-to-Phy interface uses 12 pins and, for more flexible design-in, the interface I/O support voltage from 1.65 V to 3.6 V. The ISP1504 also includes a built-in overcurrent detector for the V_{BUS} and is housed in a 32-pin HVQFN package that measures only 5x5 mm².

ISP1505 for USB standalone or portable systems

Optimized for use in standalone systems, such as set-top boxes or PC peripherals, the ISP1505 provides interfaces to host and peripheral cores. It keeps the same 12-pin Link-to-Phy interface as the ISP1504 but comes in a smaller HVQFN package with only 24 pins. For efficient use of the V_{BUS} , the ISP1505 fully supports the Session Request Protocol (SRP).

ISP1506 for size-constrained OTG systems

For portable applications with tight size constraints, the ISP1506 provides full support for OTG in a 24-pin HVQFN package that measures only 4x4 mm². A four-bit Double Data Rate (DDR) bus means the Link-to-Phy interface in the ISP1506 uses only eight pins. To reduce power consumption in battery-operated systems, the digital I/O voltage interface operates between 1.65 V and 1.95 V.



ISP1504 block diagram

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Philips Semiconductors is a worldwide company with over 100 sales offices in more than 50 countries. For a complete up-to-date list of our sales offices please e-mail sales.addresses@www.semiconductors.philips.com. A complete list will be sent to you automatically. You can also visit our website <http://www.semiconductors.philips.com/sales>.

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