

Preliminary Specifications



4Mbit (512K x8-bit) Flash memory LE28FW4003N-70

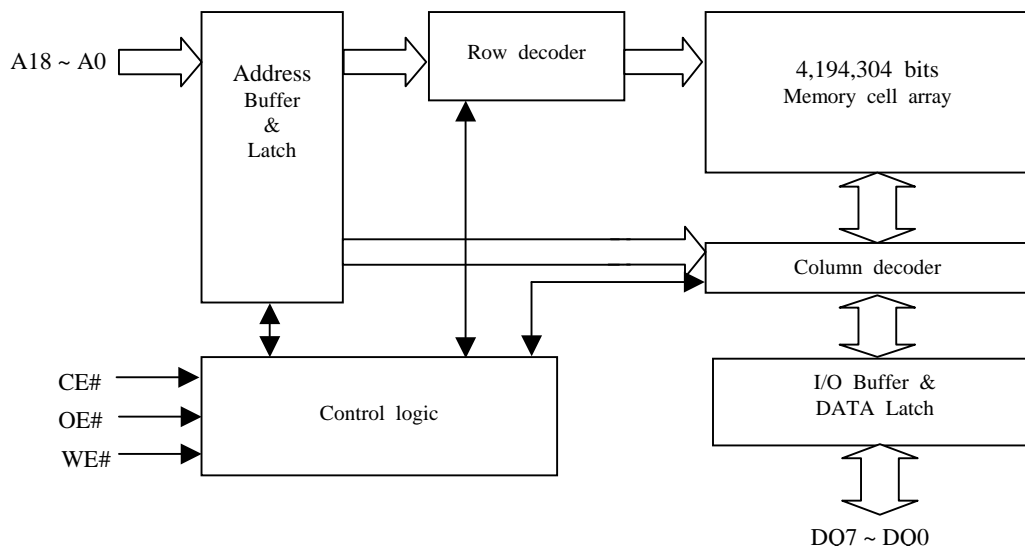
Description

The LE28FW4003 (hereinafter referred to as 'this device') is a flash memory that consists of 4,194,304bits(524,288words x 8bits) and it can erase and program due to a 3V-single supply voltage. This device features erase suspend/resume functions with which the device can suspend and resume erase. During erase is suspended, this device can read or program the cells not to be erased. The erase unit is 65,536 bytes, but erase in a smaller unit, which is 4,096 bytes (a small sector), is also possible. Moreover, this device supports the chip batch erase operation that erases a chip entirely and the multiple sector batch erase operation that selects multiple sectors to erase them at a time.

Features

- **Power supply voltage:** 2.7V ~ 3.6V
- **Access time:** Random access: 70ns (Max.)
- **Hardware ID entry**
 - SDP command entry and A9 High voltage entry.
 - ID read entry by applying high voltage to A9 is possible as well as the same entry by a command input.
- **Power consumption**
 - Operation mode (readout): 25 mA (Max.)
 - Standby mode: 10 μ A (Max.)
- **Detection of program/erase end**
 - Device status can be determined by Hardware Sequence Flag (Toggle bit/ Data polling).
- **Erase unit**
 - Sector: 64k bytes
 - Small sector: 4k byte
 - Chip: all the memory cells
- **Package:** 32-pin PLCC
- **Multiple sector batch erase**
 - After specifying multiple sectors to be erased, all the selected sectors can be erased at a time altogether.
- **Reliability:** W/E endurance: over 10K cycles (Typ. 100K cycles), Data retention period: over 10 years

Figure 1: Function diagram



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4M-Bit Flash Memory

Preliminary Specifications

Figure 2: Pin Assignment

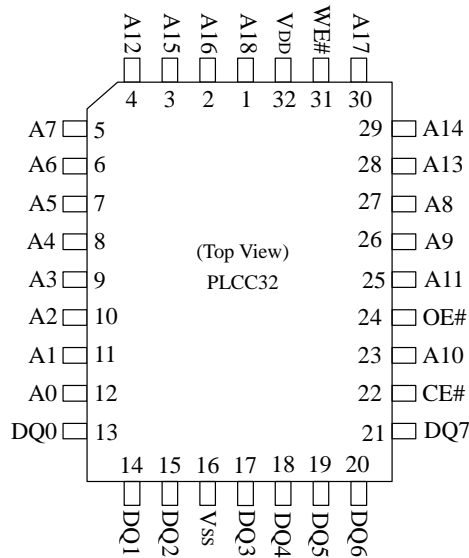


Table 1: Pin descriptions

Symbol	I/O	Function
A18 ~ A0	Input	Pins for address input. These address values are latched inside the device during a write cycle. High voltage (VID) is applied to A9 when “Hardware ID Read Operation” is carried out.
WE#	Input	This pin enables write operation. It’s active, when WE# = Low level.
OE#	Input	This pin enables output buffers. It’s active, when OE# = Low level.
CE#	Input	This pin enables the device. It’s active, when CE# = Low level. It’s in a standby mode, when CE# = High level.
DQ7 ~ DQ0	Input / Output	Data output and input pins. While the device is in a read operation, these pins function as output pins. During a write cycle, these pins function as input pins and are latched inside. When OE# or CE# is set to high, DQ shifts to High impedance.
V _{DD}	Power supply	This pin supplies 3.0 V-power voltage (2.7V ~ 3.6V) .
V _{SS}	Ground	This pin supplies 0V.

Table 2: Pin Input / Output for Each Operation Mode

Operation	CE#	OE#	WE#	A0	A1	A2	A3	A4	A5	A6	A7	A9	DQ7 ~ 0
Manufacturer Code ⁽¹⁾	V _{IL}	V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{ID} ⁽³⁾	(62h)
Device Code ⁽¹⁾	V _{IL}	V _{IL}	V _{IH}	V _{IH}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{IL}	V _{ID} ⁽³⁾	(0Eh)
Read	V _{IL}	V _{IL}	V _{IH}	A0	A1	A2	A3	A4	A5	A6	A7	A9	D _{OUT}
Standby	V _{IH}	X	X	X	X	X	X	X	X	X	X	X	High-Z
Output Disable	X	V _{IH}	V _{IH}	X	X	X	X	X	X	X	X	X	High-Z
Write (Erase/Program)	V _{IL}	V _{IH}	V _{IL}	A0	A1	A2	A3	A4	A5	A6	A7	A9	D _{IN}
Write Disable	X	V _{IL}	X	A0	A1	A2	A3	A4	A5	A6	A7	A9	D _{OUT}
	X	X	V _{IH}	A0	A1	A2	A3	A4	A5	A6	A7	A9	High-Z / D _{OUT}

(1) Reading a device code and a manufacturer code can be done by command input. Refer to **Table 3 Software Command Sequence** for those operations by command input.

(2) “X” in this table indicates V_{IL} or V_{IH}.

(3) V_{ID} indicates High voltage.

Basic Function Description

Refer to the following descriptions, and timing diagrams or algorithms specified in descriptions of each item.

(1) Read Operation

For data readout, both CE# and OE# should be set to a low level. If CE# is set to a high level, the chip gets deselected. OE# functions as a gate to determine whether inner output should be sent to outside. If it is set to a high level, it prohibits output and the output pins turn to a high impedance state. For the details, refer to the **Readout Timing Chart (Figure 3)**.

This device has a self-power save function, with which the device automatically turns to a standby status if address input doesn't change for more than 150ns during normal cell readout. Consequently I_{DD} becomes 2 μ A (typ). Due to this function, the I_{DD} value during readout changes to 1mA / MHz (typ) that corresponds to an operation frequency. Once an address or any input of a control pin has changed, the self-power save is automatically cleared. This self-power save function doesn't lead to a longer access time.

(2) ID read operation

ID read operation reads ID code (manufacturer code and device code). With this function, the device can be identified from outside. This operation is used, for example, to automatically set a program sequence for programming with a PROM writer. Two ways of ID code readout are available in this device. The contents of the code to be read compile with **ID code table (Table 3)**. The readout timing is the same as that of memory cell readout.

-a Hardware ID Read Operation

The hardware ID read operation reads ID code by applying high voltage to A9. (V_{ID}). Typically, this is used when PROM writer executes ID code readout. From the lower address of 00h and 01h, a manufacturer code and a device code are read respectively. By canceling the high voltage in A9, the read operation is restored. For the input waveform at the hardware ID readout, refer to the **Hardware ID read timing chart (Figure 12)**.

-b Software ID read operation

The software ID read operation reads the device code without applying high voltage to a chip. Since ID code can be read without applying high voltage to the address bus, this is effective to identify the device incorporated in the set. To execute the software ID read, command input of 4-bus cycle is required. In the 4th bus cycle, input 00h or 01h to the lower address. From the addresses of 00h and 01h, the manufacturer code and the device code are read respectively. To clear the Software ID read operation, the reset command must be input. For the waveform at the software ID read, refer to the **Software ID read timing chart (Figure 13)**. To clear the software ID read mode and to read regular cells, **Reset Operation ((5)-a, (5)-b)** must be executed

Table 3 :ID code

Type	A7 ~ A0	Code (HEX)
Manufacturer code	00h	62h
Device Code	01h	0Eh

4M-Bit Flash Memory

Preliminary Specifications

Table 4: Software Command Sequence

Command Sequence	Bus Write Cycle	1 st Bus		2 nd Bus		3 rd Bus		4 th Bus		5 th Bus		6 th Bus	
		address	data	address	data	address	data	address	data	address	data	address	data
Read/Reset A**	1	XXXh	F0h	RA ⁽¹⁾	RD ⁽²⁾								
Read/Reset B**	3	555h	AAh	2AAh	55h	555h	F0h	RA ⁽¹⁾	RD ⁽²⁾				
ID Read	3	555h	AAh	2AAh	55h	555h	90h	IA ⁽³⁾	ID ⁽⁴⁾				
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA ⁽⁵⁾	PD ⁽⁶⁾				
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA ⁽⁷⁾	30h
Small Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA2 ⁽⁸⁾	70h
Erase Suspend	1	XXXh	B0h										
Erase Resume	1	XXXh	30h										

note:

- * Valid address pins for inputting command codes are A10 ~ A0. The least significant address is A0, and the valid DQs are DQ7 ~ DQ0.
- * Addressed and data are shown in hexadecimal.
- * XXXh indicates a discretionary address.
- ** Two kinds of read/reset command function are identical, and the both set the device to the readout mode.

Brevity code descriptions of Address/Data

- (1) RA: read address
- (2) RD: output data of readout
- (3) IA: ID read address (A7, A6, A5, A4, A3, A2, A1, A0)
- (4) ID: ID code output (Manufacturer code = 62h Device Code = 0Eh)
- (5) PA: program address
- (6) PD: program input data
- (7) SA: sector address (A18, A17, A16)
- (8) SA2: small sector address (A18, A17, A16, A15, A14, A13, A12)

Table 5: Sector Address Table

Sector	A18	A17	A16	Sector size (K byte)	Range of address
SA0	0	0	0	64	00000h ~ 0FFFFh
SA1	0	0	1	64	10000h ~ 1FFFFh
SA2	0	1	0	64	20000h ~ 2FFFFh
SA3	0	1	1	64	30000h ~ 3FFFFh
SA4	1	0	0	64	40000h ~ 4FFFFh
SA5	1	0	1	64	50000h ~ 5FFFFh
SA6	1	1	0	64	60000h ~ 6FFFFh
SA7	1	1	1	64	70000h ~ 7FFFFh

The address ranges from A18 to A0.

(3) Program Operation

The program operation rewrites a target memory from '1' data to '0' data. In this device, programming can be executed in units of byte (8bits).

-a Byte Program Operation

This device can execute the program operation in units of byte (8bits). This operation is called as the byte program operation. This operation is done by setting OE# to a high level and inputting the byte program command that consists of 4 bus cycles. As the byte program is executed only to the memory cells in the erase status, the target sectors for the byte program must be erased in advance. The target program address is set in units of byte. The address is latched into the memory at falling edge of WE# and the program data is latched at rising edge of WE#. As for the input waveform at the byte program, the contents of input command and outline of the byte program operation, refer to the **Byte Program Timing Chart (Figure 6)**, the **Software Command Sequence (Table 4)** and the **Byte Program Algorithm (Figure 17)** respectively.

To simplify the descriptions, this spec only explains the way of controlling by the rising and the falling edge of WE#. However, the rising and the falling edge of CE# can also realize the same operation.

(4) Erase Operation

The erase operation rewrites the data from 0 to 1. Three kinds of unit for erase are available. The first one is a chip erase operation that erases entire memory of a chip. The second one is a sector erase operation that erases in units of 64k byte, based on a sector address listed in **Sector Address Table (table 5)**. The third one is a small sector erase operation that can erase in units of 4k byte. To execute each erase operation, it is required to set OE# to a high level and to input the SDP erase command that consists of six bus cycles. For details of input at the erase operation, refer to the three kinds of **Erase Timing Charts (Figure 7, Figure 8, and Figure 9)** and the **Software Command Sequence (Table 4)**.

-a Chip Erase Operation

The chip erase operation rewrites the entire data of the flash memory to 1 data, and it starts by inputting of the SDP command sequence of 6 bus cycles. After the command sequence is input, erase is automatically carried out in units of sector within the device. When all the sectors are erased, the operation terminates. For details, refer to the **Chip Erase Timing Chart (Figure 7)**, the **Software Command Sequence (Table 4)** and the **Erase Algorithms (Figure 18)**. This chip erase operation requires no advance programming by users. Thus, the erase time is given by the expression $\text{Chip Erase Time} = \text{Sector Erase Time} \times \text{Sector Count}$.

-b Sector Erase / Multiple Sector Batch Erase Operation

The sector erase operation rewrites data in a given sector (64K byte) or boot sector range to 1. A certain address of the sector addresses from SA0 to SA7 listed in the **Sector Address Table (Table 5)** is rewritten. **The erase operation is automatically executed to a designated sector within the device, which starts by inputting the SDP command sequence of 6 bus cycles.** For details, refer to the **Sector Erase Timing Chart (Figure 8-a)**, **Software Command Sequence (Table 4)** and the **Erase Algorithms (Figure 20)**. The **Multiple Sector Erase** erases multiple sectors simultaneously by repeating the final bus cycle of the sector erase command to input each sector address and the final bus command (30h). For this function, the bus cycle must be repeatedly input during the sector erase hold time (tSEDH). When any command except for the sector erase command (30h) or erase suspend command (B0h) is input during the sector erase hold time, the device resets inner command registers and is set to the read mode. For details, refer to **Multi-Sector Erase Timing Chart (Figure 8-b)**. In this case, the erase time is calculated by the expression $\text{Multiple Sector Batch Erase Time} = \text{Sector Erase Time} \times \text{the number of erase sectors}$.

Same as **Chip Erase (-a)**, the sector erase /multiple sector batch erase requires no advance programming for the target sector by users.

-c Small Sector Erase Operation

The small sector erase operation rewrites data in a given small sector (4K byte) to 1. Each sector from SA0 to SA7 listed in the **Sector Address Table (Table 5)** is 64bytes in size. However, the small erase operation can erase in units of 4K byte regardless of these sector allocation. The way to start by inputting the SDP command sequence of 6 bus cycles is the same as that of the sector erase operation, but the final bus commands are not identical. It is impossible to erase multiple small sectors at a time. For details of the input at the small sector erase operation, refer to the **Small Sector Erase Timing Chart (Figure 9)**, the **Software Command Sequence (Table 4)** and the **Erase Algorithms (Figure 18)**. The small sector erase also requires no advance programming for the target sector.

(5) Reset Operation

The reset operation is available in this device to initialize the read mode.

-b Read Reset

This device has two kinds of read reset commands as listed in the **Software Command Sequence (Table 4)** to set the mode back to the read mode, when an automatic operation ends abortively as the timing limited is exceeded ((8)-c) during its internal operation and consequently the device gets locked. As for the input waveform at the reset operation, refer to the **Read Reset Timing Chart (Figure 14)**. The functions of these two read reset commands are identical. By executing these read reset, it is also possible to shift the ID read mode to the readout mode of normal cells in addition to restore the device from an abortive end of an automatic operation. However, the device cannot be set to the readout mode by suspending program or erase operation. When the read reset is effectively done, this device is set to the read mode.

Table 6: Read Reset Function

Function	Read Reset
Termination of ID Read mode	Possible
Clearing of a command register	Possible
Unlock when an automatic operation ends abortively	Possible
Abortion of an automatic operation	Impossible

(6) Erase Suspend / Resume

This device can execute erase suspend / erase resume only while the device is in the sector erase mode. The erase suspend mode makes it possible to suspend an erase operation, to read from the sectors that are not selected as an erase mode and to execute a program to those sectors. The commands available in the erase suspend mode are **(3)-a Byte program, (2)-b Software ID Readout, (5)-b Read Reset and Resume Command** that aborts the suspend mode.

The erase suspend mode is enabled by inputting an erase suspend command listed in **Software Command Sequence Table(Table.4)** while **(4)-b Sector Erase / Multiple Sector Batch Erase** is being operated, which includes the sector erase hold time(tSEDH). When the erase suspend time (tSUSE) has passed after the erase suspend command is input, the device enters the erase suspend mode. Whether the device enters the erase suspend mode can be checked by **the Hardware Sequence Flag**. As for the input waveform at the erase suspend, see **Erase Suspend Timing Chart (Figure 10)**.

When sectors are continuously read while the erase operation is in progress, DQ6 toggles. On the other hand, when sectors that suspend an erase operation are continuously read in the erase suspend mode, DQ2 toggles instead of DQ6.

During the erase is suspended, **(3)-a Byte Program, (2)-b Software ID Read, and (5)-b Read Reset** can be applied to the sectors not under the erase mode in the same way as usual programs. The erase operation cannot be executed to other sectors during the erase suspend time.

To stop the erase suspend and to resume the erase operation, input an erase resume command listed in **Software Command Sequence Table (Table 4)**. As for the waveform at the erase resume, see **Erase Resume Timing Chart (Figure 11)**. When the erase suspend is executed during the erase hold time, the device enters the erase hold time (tSEDH) again if the resume command is executed and received validly. During the erase hold time, an erase sector of **Multiple Sector Batch Erase Operation** can be added. After the erase hold time, DQ6 restart toggling. When the erasing operation is suspended and the resuming operation is received validly, the device returns to the erase period, DQ6 restarts toggling.

(7) Hardware Data Protection

This device can protect sectors by the hardware and the software. Hardware data protection function protects data from being erased accidentally or unexpected programming, and command input is not necessary.

-a Preventing Low VDD Program Erase

The function of prohibiting programming in the low VDD is to prohibit receiving commands when VDD is 1.5V or less, to stop an inner automatic operation, and to prevent data from being rewritten. This function protects data from an unexpected program that might occur when the power-supply voltage is low.

-b Preventing Gritty Malfunction

To protect data from an unexpected program of the device due to gritty, a pulse below 5ns to be added to WE# is designed to be ignored. When a gritty that exceeds 5ns is input, malfunctions might occur.

-c Preventing Malfunction When Power is Provided

When power is provided, program and erase operations are prohibited by retaining either of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. Be sure to keep this status, when you provide or cut off power.

(8) Software Data Protection (SDP)

In this device, a compatible command of JEDEC-standard type is input to activate program or erase operation. In this method, all the write operation (program/erase) requires multiple inputs of bus commands to be added to address pins and DQ. In a JEDEC-standard command, DQ input is a byte-format (8 bits from DQ0 to DQ7).

While a command is input, which is WE# = H, loading operation of inner commands are suspended. Thus reading is possible during this period.

When a command sequence is rejected: incorrect addresses or data are loaded for instance, the device goes back to the readout mode. In this case, the device returns to the readout mode within t_{RC} after the incorrect addresses or data are input.

(9) Hardware Sequence Flag

This device automatically executes erase and program operations. The hardware sequence flag indicates whether these automatic operations complete correctly based on the output of the data pins. The hardware sequence flag can be read at the same level of reading timing by lowering the CE# and OE# level during writing. For information such as what a certain data indicates or in which pin a certain data is output, see **Hardware Sequence Table (Table 7)**.

When the hardware sequence flag indicates that automatic writing is completed, the device automatically returns to the readout mode.

Actual writing is automatically completed with its inner timer. DATA# polling and a toggle bit occur upon completion of inner writing. After these two occur, this device outputs a status different from the one before the writing through DQ6 and DQ7 to inform outside that writing is completed. Reading twice the address to be written additionally can avoid rejecting the device by the false decision. The fact that in both two cases the data read from these DQ6 or DQ7 is found valid indicates the program cycle is completed correctly. When the data is found otherwise, that indicates the program isn't completed correctly.

4M-Bit Flash Memory

Preliminary Specifications

Table 7: Hardware Sequence Flag Table

Status			DQ7	DQ6	DQ5	DQ3	DQ2	
Automatic Operation	Automatic Program		DQ7#	Toggle	0	0	1	
	Erase mode	Erase hold time ⁽⁶⁾	Selected sector ⁽¹⁾	0	Toggle	0	0	Toggle ⁽⁵⁾
			Non-selected sector ⁽²⁾	0	Toggle	0	0	1
		Erase operation	Selected sector ⁽¹⁾	0	Toggle	0	1	Toggle ⁽⁵⁾
			Non-selected sector ⁽²⁾	0	Toggle	0	1	1
	Erase suspend mode	Readout	Selected sector ⁽³⁾	1	1	0	0	Toggle
			Non-selected sector ⁽⁴⁾	Data	Data	Data	Data	Data
		Program	Selected sector ⁽³⁾	DQ7#	Toggle	0	0	Toggle
			Non-selected sector ⁽⁴⁾	DQ7#	Toggle	0	0	1
	Timeout	Program		DQ7#	Toggle	1	0	1
Erase		0	Toggle	1	1			
Program during erase suspend		DQ7#	Toggle	1	0			

- (1) When the hardware sequence flag is read in the sector to be erased.
- (2) When the hardware sequence flag is read in the sector not to be erased but located in the same bank as the sector to be erased.
- (3) When the hardware sequence flag is read in the sector to be erased and also under suspending.
- (4) When the hardware sequence flag is read in the sector to be erased but not under suspending, and that is located in the same bank as the sector under suspending.
- (5) DQ2 doesn't toggle at the time of the small-sector erase and Security Sector range-sector erase, and H level is output.
- (6) It is only under the sector erase that the hardware sequence flag can be read during the erase hold time.

-a DATA# Polling (DQ7)

When you read the data (See **DATA# Polling Timing Chart (Figure 15)**) during an internal automatic program, the inversed data of the one that finally executed programming is read from DQ7. When you read the data after the inner automatic program is completed, the data that finally executed programming is read from DQ7. The output of DATA# polling becomes valid after the rising edge of WE# (or CE#) of the final bus cycle in the automatic operation command sequence. When you read while the inner automatic erase is operating, 0 is read from DQ7. When you read after the same is completed, 1 is read from DQ7.

-b Toggle Bit (DQ6)

When you repeat reading while this device is in automatic program status or erase status inside, DQ6 outputs 0 and 1 by turns. (**See Toggle Bit Timing Chart (Figure 16)**) When inner automatic operation is completed correctly, outputting by turns stops and this device gets ready for accepting the next operation. The output of toggle bit becomes valid after the rising edge of WE# (or CE#) of the final bus cycle in the automatic operation command sequence.

-c Exceeding Timing Limit (DQ5)

When you read data while a programming or erasing is internally carried out, 0 is output from DQ5. When erase time exceeds the designated value, DQ5 outputs 1 regardless of the contents of cell data that corresponds to DQ5. (Exceeding of timing limit) The fact that DQ5 outputs 1 indicates that inner automatic operation doesn't end properly. Which also indicates that a part of this device might be defective. Once the status signal indicating exceeding of timing limit has been output, the output continues unless you provide power of the device again, or you execute **Hardware Reset ((5)-a)** or **Read Reset ((5)-b)**. Even when the inner erase is done correctly within the designated time, DQ5 sometimes outputs 1. This is because DQ5 outputs the erased data. You could know whether data of 1 output from DQ5 indicates exceeding of timing limit or indicates the read data of a cell by checking whether either DATA# polling or the output signal of the toggle bit indicates the end of writing.

-d Sector Erase Timer (DQ3)

As shown in (4)-b, this device can erase multiple sectors simultaneously by repeating the 6th bus cycle of the sector erase during erase hold time. DQ3 indicates whether the device is in the erase hold status, when multiple sector batch erase is executed. When the 6th bus cycle of the sector erase command is input and the device shifts to the erase hold status, DQ3 outputs 0 indicating that additional address input is acceptable. When the address erase hold time is finished and the device doesn't receive new addresses any more, 1 is output. Then erase operation automatically starts within the device, which means new addresses cannot be accepted any more.

-e Toggle Bit 2 (DQ2)

When you repeat reading in a given sector under sector erase operation or under chip erase operation, DQ2 outputs 0 and 1 by turns. When a sector not to be erased is selected and the sector is continuously read, DQ2 outputs 1. Seeing the output difference of DQ2, you could know if the sector you selected is to be erased or not. In case of small sector erase, DQ2 under erase operation doesn't carry out toggle.

This device has erase suspend/resume function, and you can read the device by suspending an erase operation of a certain sector. When you carry out erase suspend to select and to continuously read a sector under an erase suspend operation (any sector selected to be erase, in case of multiple sector batch erase), not DQ6 but DQ2 toggles. Therefore, it is possible to detect a sector under erase suspend by using DQ2. During erase hold time, Toggle Bit 2 doesn't function.

When you set an erase operation to a sector protected or a boot sector protected and you read DQ2 by appointing those sectors, DQ2 toggles. In this case, actual erase operation doesn't occur.

4M-Bit Flash Memory

Preliminary Specifications

Absolute Maximum Rating

Storage temperature.....-65 °C ~ 150 °C
 D.C. input/output voltage-0.5 V ~ V_{DD}+0.5V
 Over shoot voltage below 20ns-1.0 V ~ V_{DD}+1.0V

Operation conditions recommended

Operation temperature..... 0 °C ~ +70 °C
 V_{DD}.....2.7 V ~ 3.6 V

DC Electric Characteristics

Symbol	Parameter	Limit			Units	Test Condition
		Min.	Typ.	Max.		
I _{DDR}	Operation current at reading		15	25	mA	CE# = OE# = V _{IL} , WE# = V _{IH} All the DQs are open. Address input = V _{IH} / V _{IL} , V _{DD} = V _{DD} max. Operation frequency = 10MHz, OE# = V _{IL}
I _{DDW}	Operation current at writing			35	mA	CE# = WE# = V _{IL} , OE# = V _{IH} , V _{DD} = V _{DD} max.
I _{SB}	CMOS standby current			10	μA	CE# = V _{DD} -0.3V, V _{DD} = V _{DD} max.
I _{LI}	Input leak current			10	μA	V _{IN} = V _{SS} ~ V _{DD} , V _{DD} = V _{DD} max.
I _{LO}	Output leak current			10	μA	V _{OUT} = V _{SS} ~ V _{DD} , V _{DD} = V _{DD} max.
V _{ID}	Input high voltage	11.5	12.0	12.5	V	A9
V _{IL}	Input L-level voltage			V _{DD} *0.2	V	
V _{ILC}	Input L-level voltage (CMOS)			0.2	V	
V _{IH}	Input H-level voltage	V _{DD} *0.8			V	
V _{IHC}	Input H-level voltage (CMOS)	V _{DD} -0.2			V	
V _{OL}	Output L-level voltage			0.2	V	I _{OL} = 100μA, V _{DD} = V _{DD} min.
V _{OH}	Output H-level voltage	V _{DD} -0.2			V	I _{OH} = -100μA, V _{DD} = V _{DD} min.

Power-up Timing

Symbol	Parameter	Maximum	Units
t _{PU_READ}	Time period from power supply to a read operation	200	μs
t _{PU_WRITE}	Time period from power supply to a write operation	200	μs

Capacitance (T_a = 25°C, f = 1MHz)

Symbol	Descriptions	Maximum	Units	Test Condition
C _{DQ}	Input pin capacitance	12	pF	V _{DQ} = 0V
C _{IN}	Input pin capacitance	6	pF	V _{IN} = 0V

4M-Bit Flash Memory

Preliminary Specifications

AC Electric Characteristics

Read cycle

Symbol	Parameter	Limits		Units
		Min.	Max.	
tRC	Read cycle time	70		ns
tCE	CE# access time		70	ns
tAA	Address access time		70	ns
tOE	OE# access time		30	ns
tCLZ	From CE# L to output low impedance	0		ns
tOLZ	From OE# L to output low impedance	0		ns
tCHZ	From CE# H to output high impedance		25	ns
tOHZ	From OE# H to output high impedance		25	ns
tOH	Retaining time of output from address change	0		ns

Erase / Program cycle

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
tSSE	Small sector erase time		0.025	3	s
tSCE	Sector erase time		0.025	3	s
tCPE	Chip erase time		0.5	60	s
tBP	Programming time		20	100	μs
tAS	Address setup time	0			ns
tAH	Address hold time	45			ns
tCES	CE# setup time	0			ns
tCEH	CE# hold time	0			ns
tOES	OE# setup time to write pulse	0			ns
tOEH	OE# hold time to write pulse	0			ns
tCP	CE# write pulse width	35			ns
tWP	WE# write pulse width	35			ns
tCPH	CE# standby pulse width	25			ns
tWPH	WE# standby pulse width	25			ns
tDS	Data setup time	35			ns
tDH	Data hold time	0			ns
tSEDH	Sector erase hold time	50			μs
tSUSE	Erase suspend time	10			μs
tVDDR	VDD rise time	0.1		50	ms
tIDA	Read standby time	150			ns

Note: Since this parameter is measured only for initial qualification, it might be affected by design or process changes.

AC Test Conditions

Input voltage..... 0 V ~ 3.0 V
 Input rise / fall time 5 ns
 Input / output timing level..... 1.5 V
 Output load..... 1TTL Gate and CL = 30pF

4M-Bit Flash Memory

Preliminary Specifications

Figure 3: Read Timing Chart

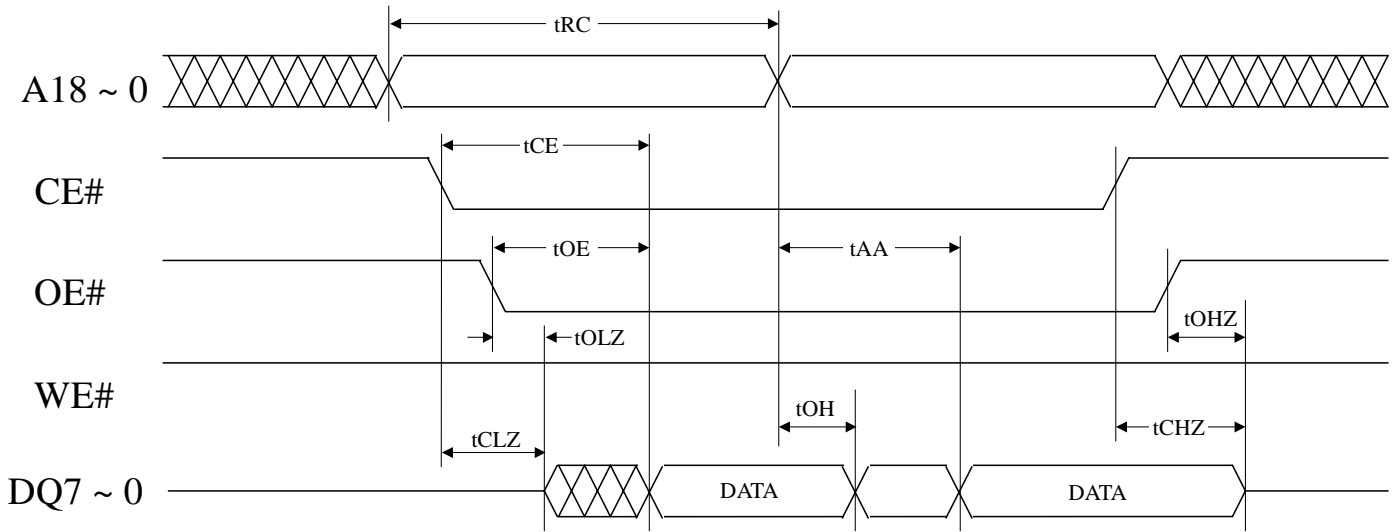


Figure 4: Timing Chart of WE# Control Write Cycle

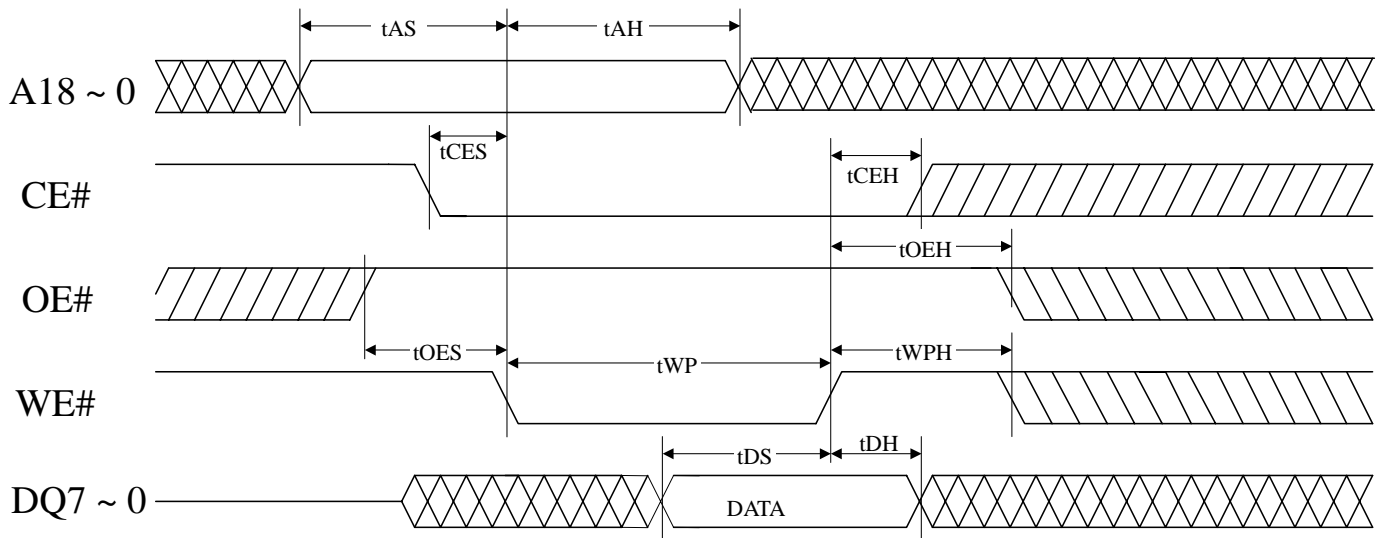


Figure 5: Timing Chart of CE# Control Write Cycle

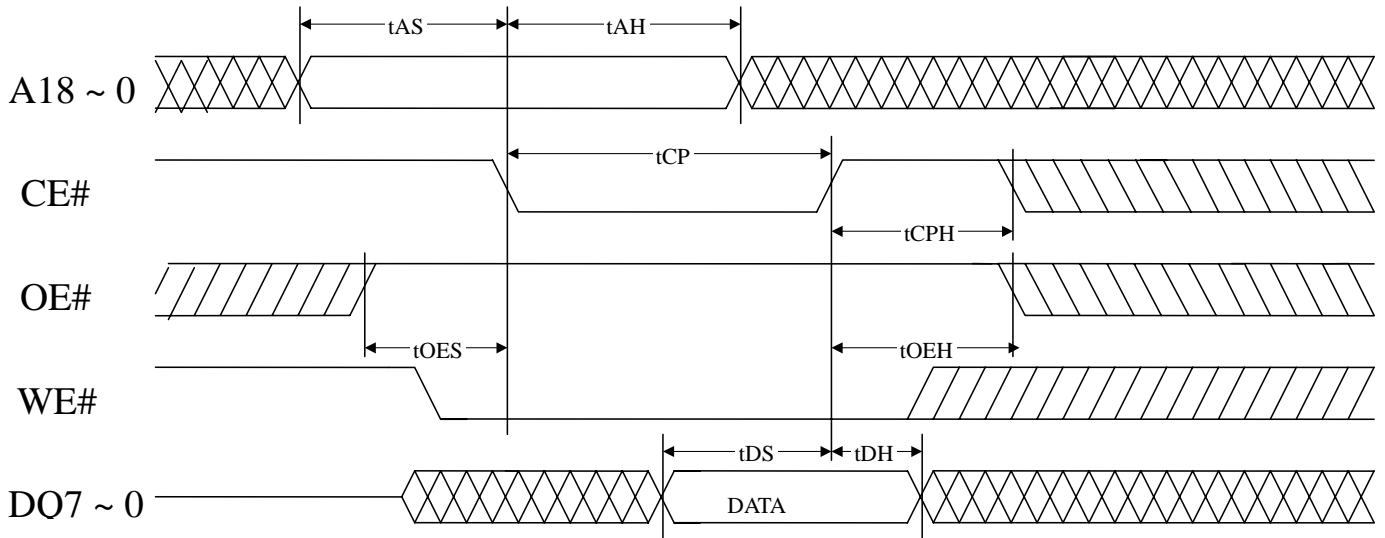
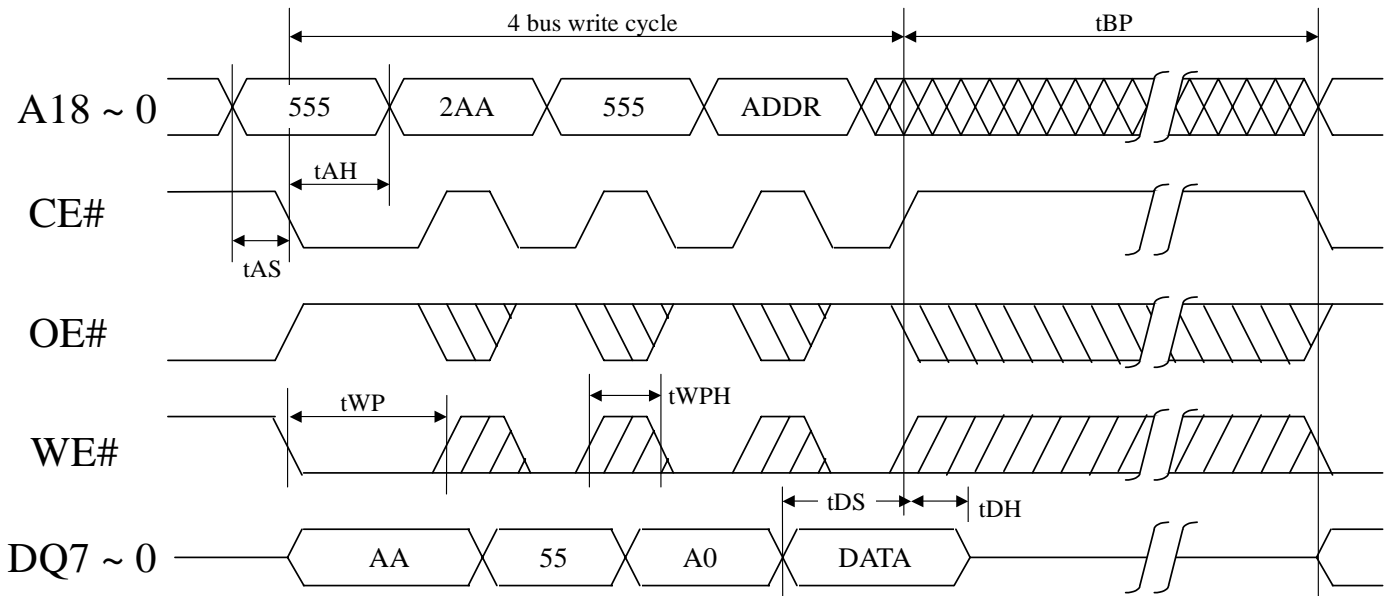


Figure 6: Byte Program Timing Chart



4M-Bit Flash Memory

Preliminary Specifications

Figure 7: Chip Erase Timing Chart

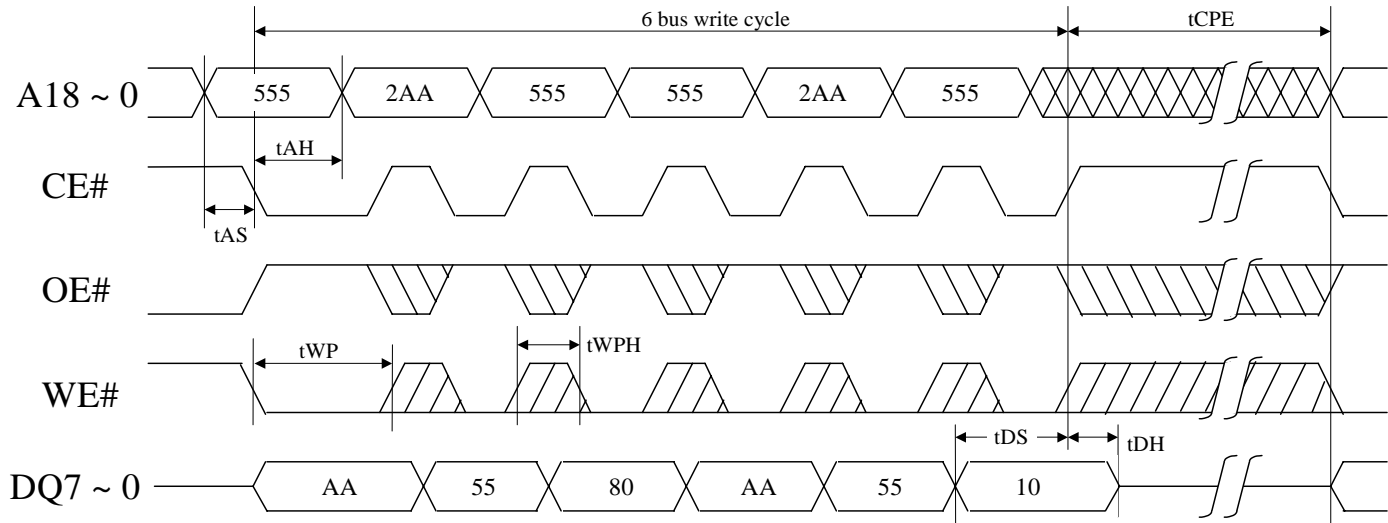


Figure 8-a: Sector Erase Timing Chart

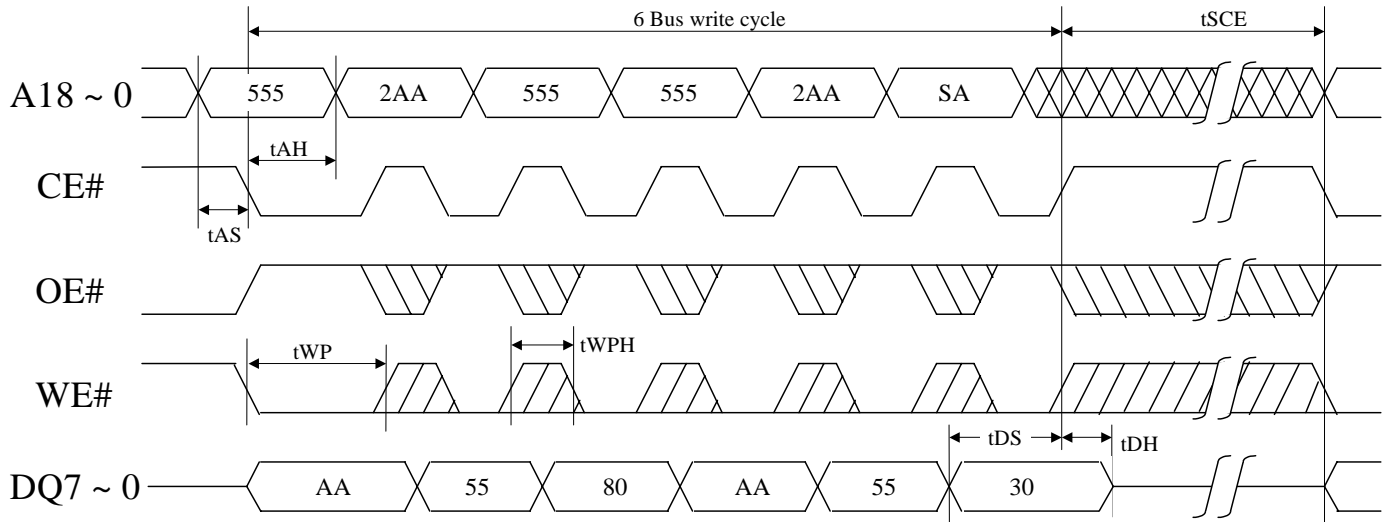


Figure 8-b: Multi Sector Erase Timing Chart

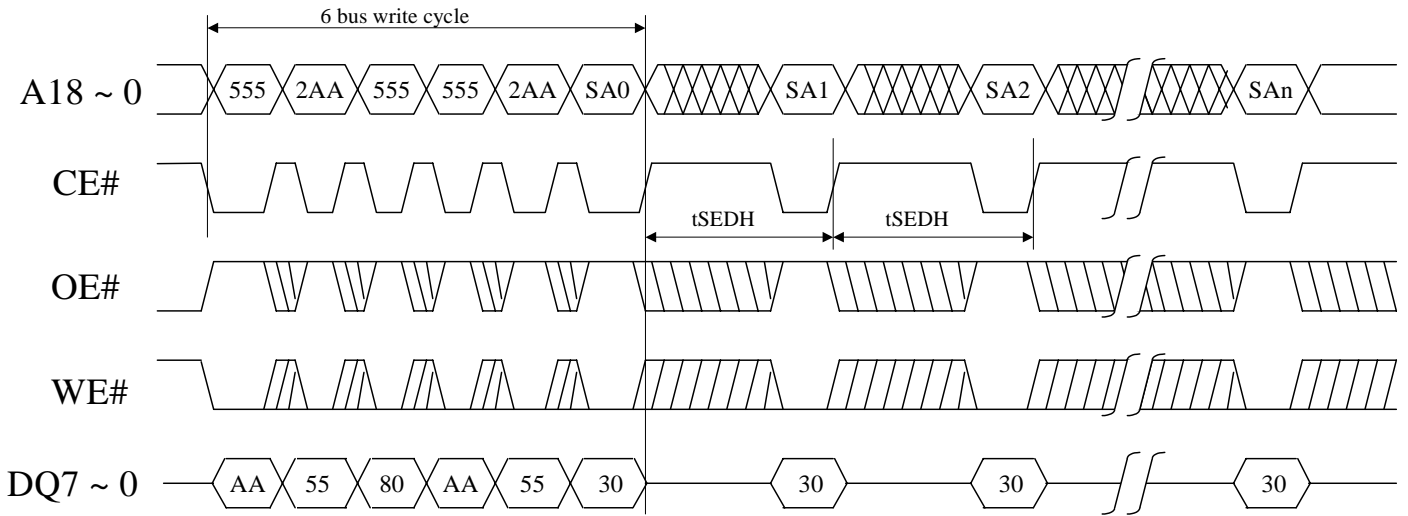


Figure 9: Small Sector Erase Timing Chart

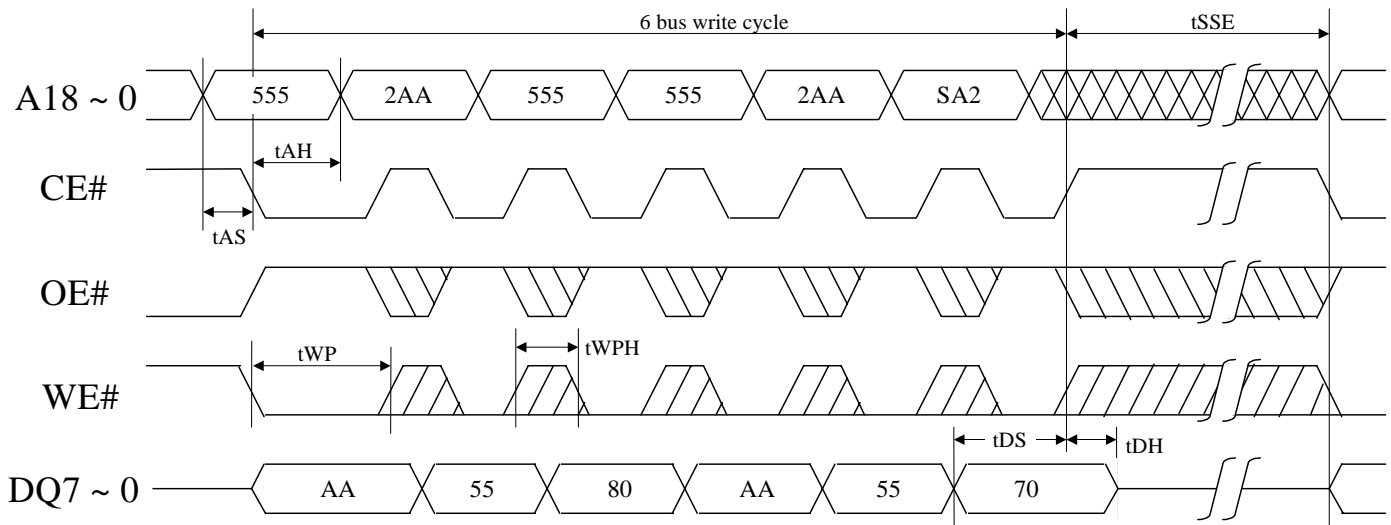


Figure 10: Erase Suspend Timing

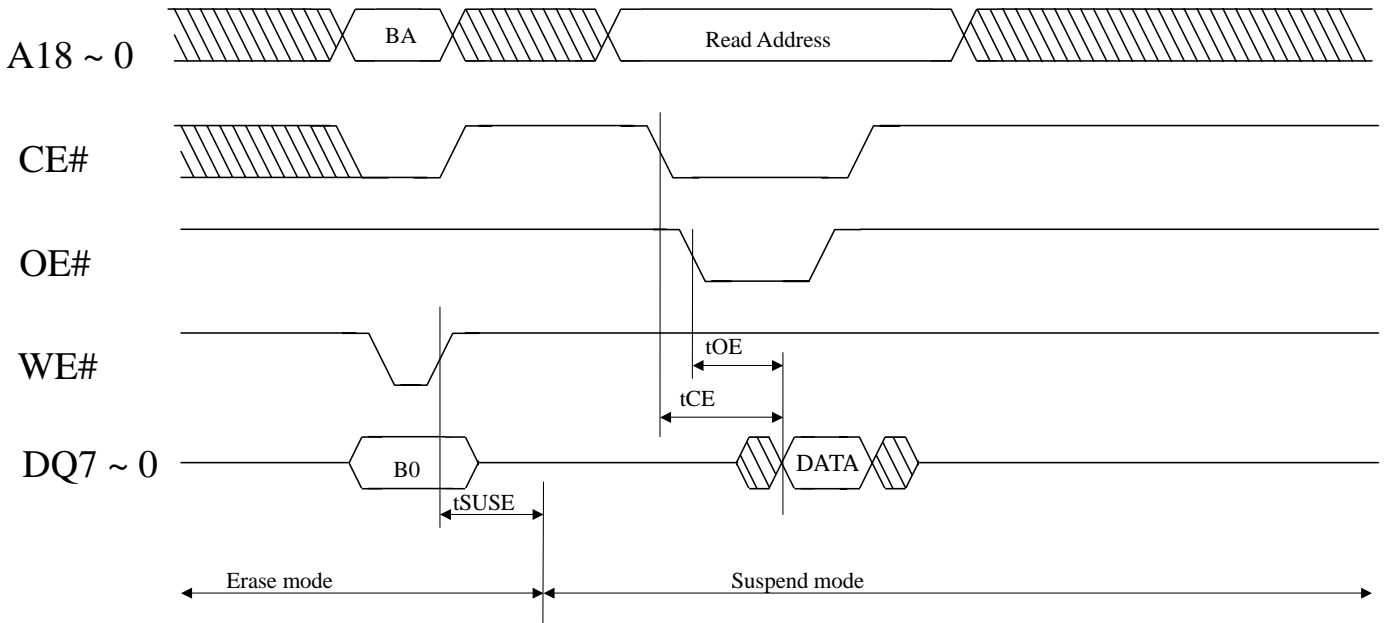


Figure 11: Erase Resume Timing Chart

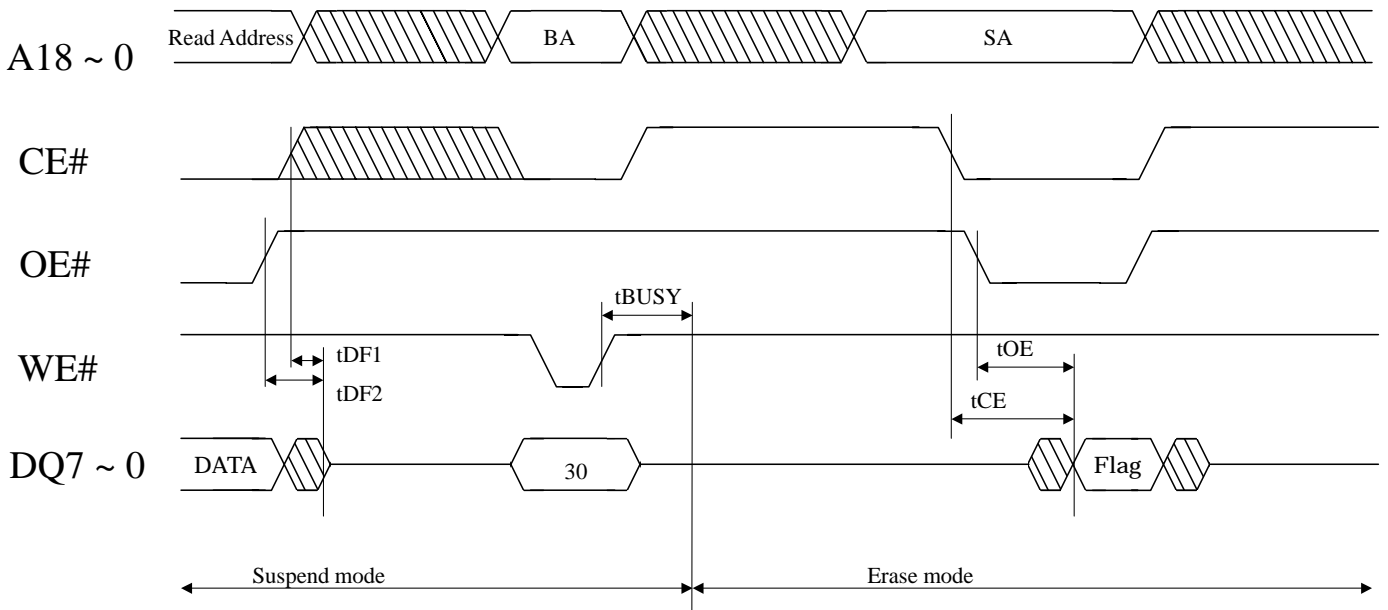


Figure 12: Hardware ID Read Timing Chart

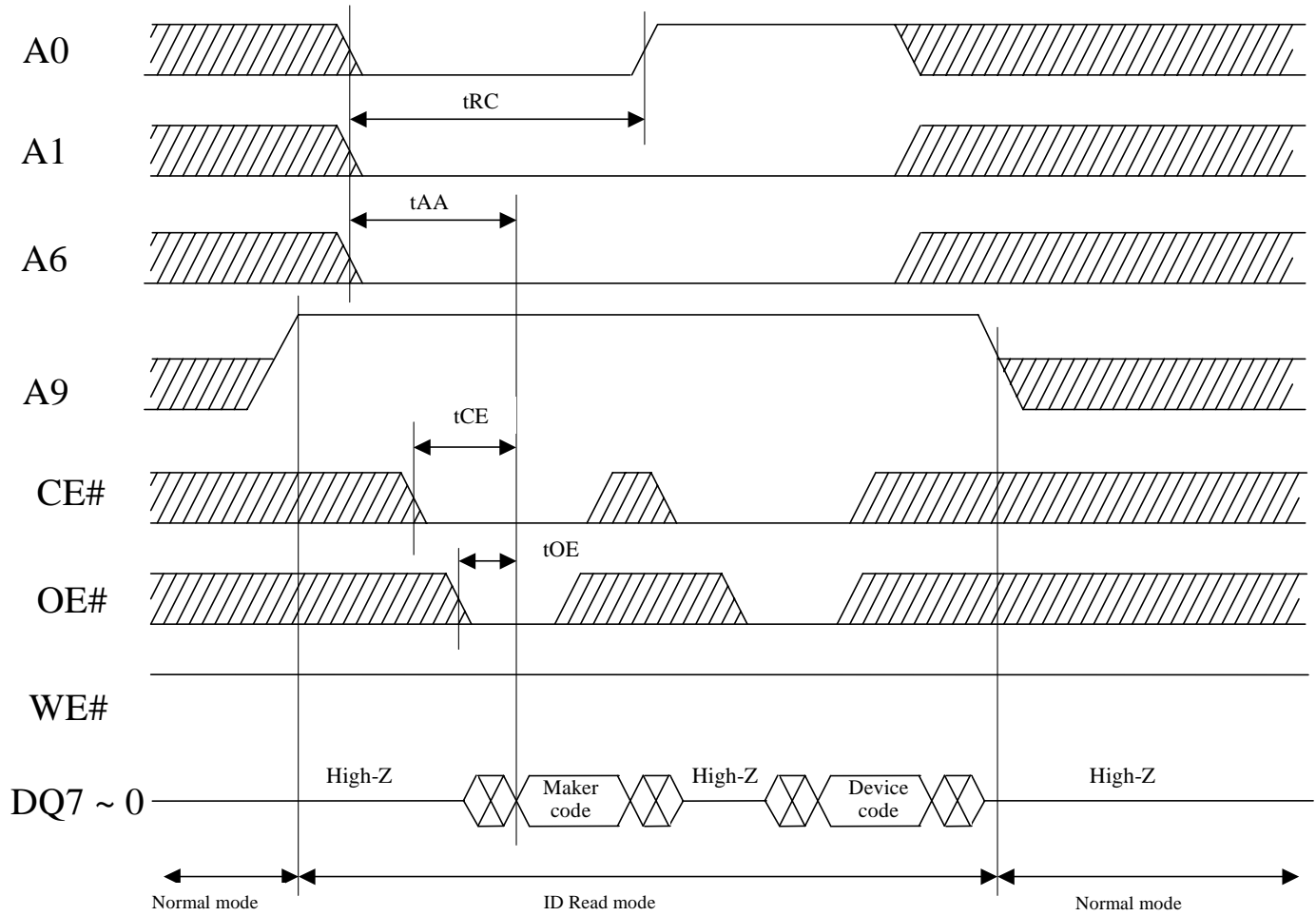


Figure 13: Software ID Read Timing Chart

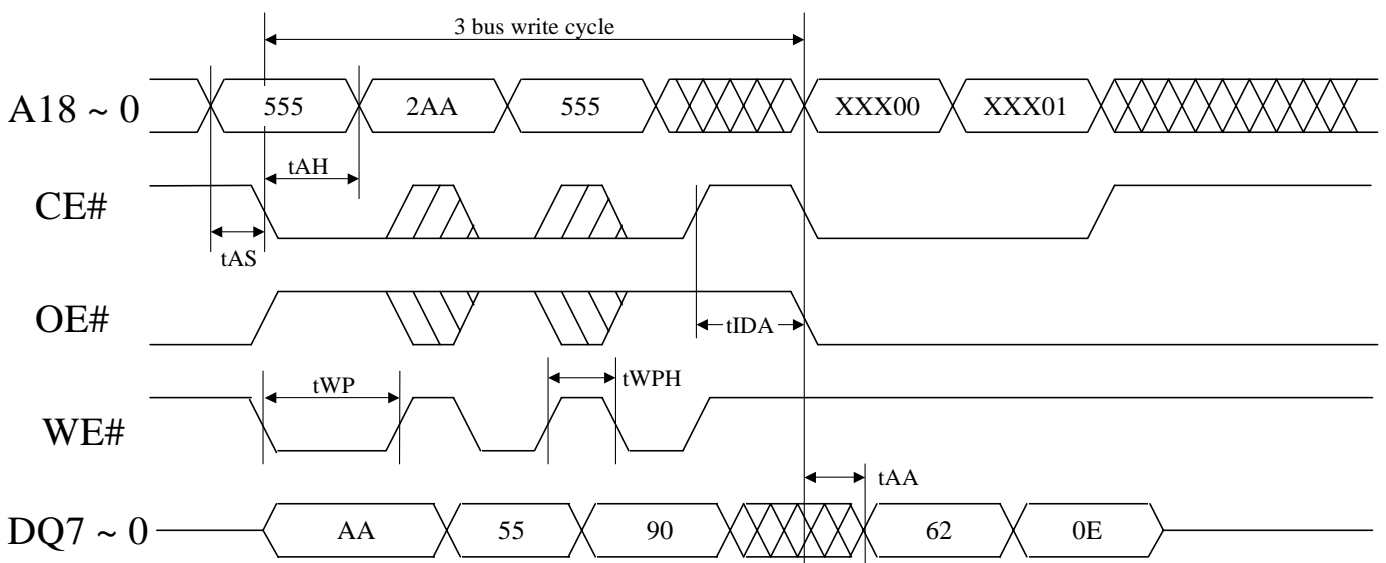


Figure 14-a: Read Reset (Read Reset A) Timing Chart

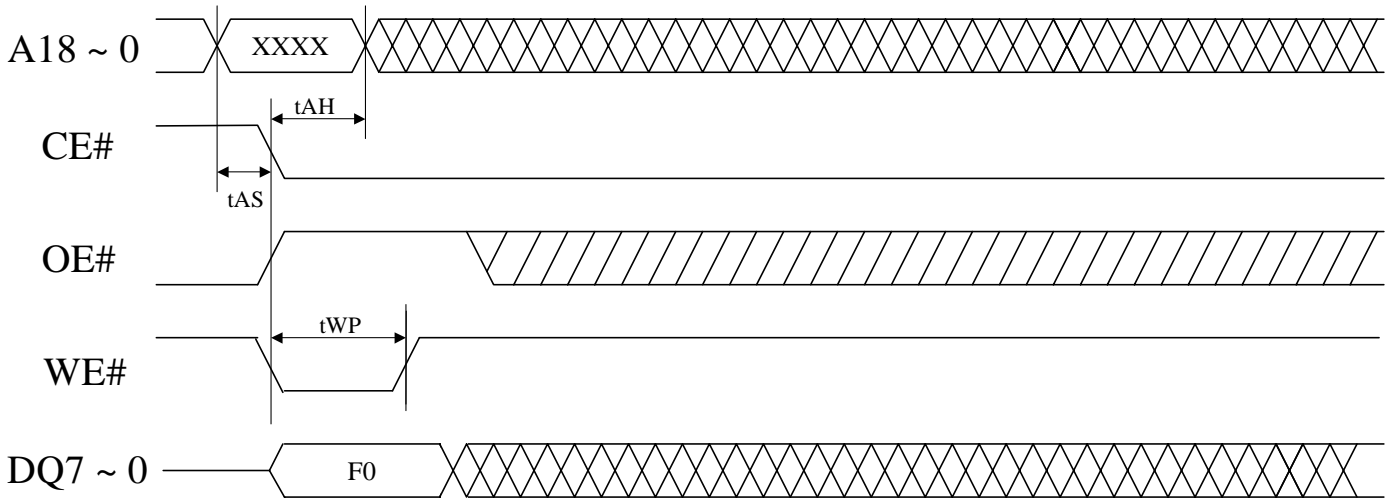


Figure 14-b: Read Reset (Read Reset B) Timing Chart

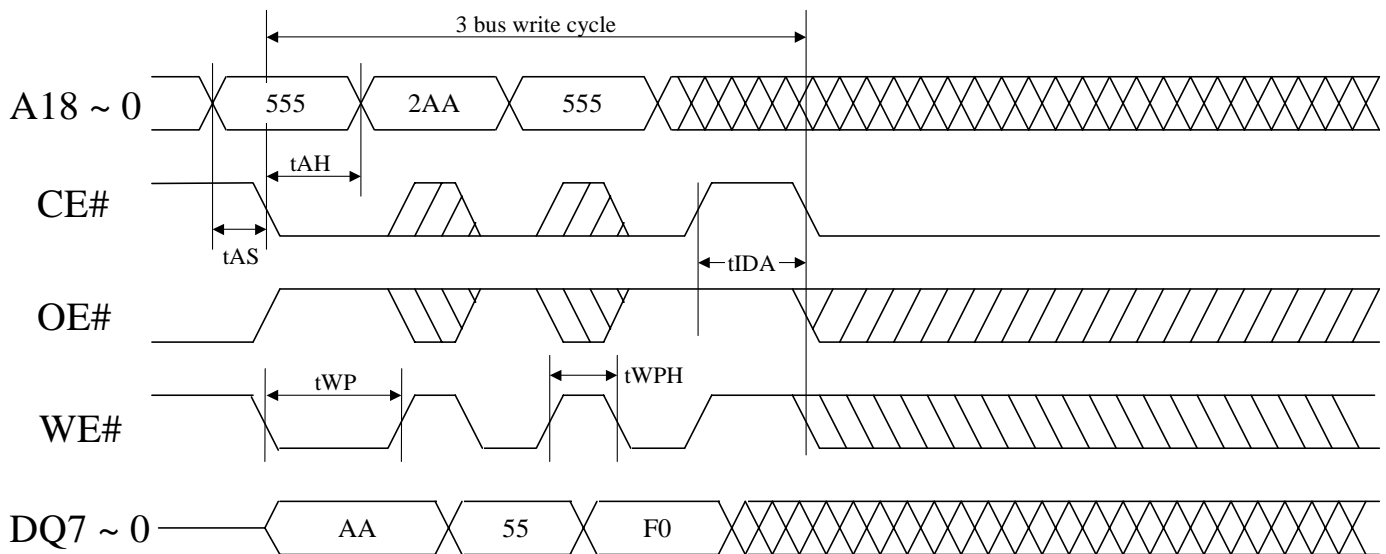


Figure 15: DATA# Polling Timing Chart (DQ7)

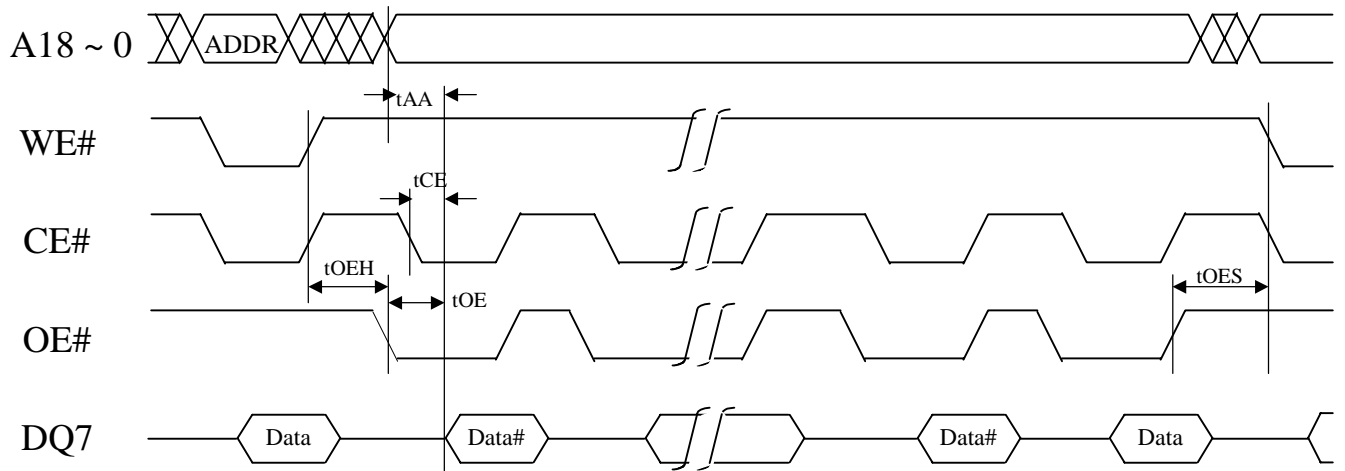
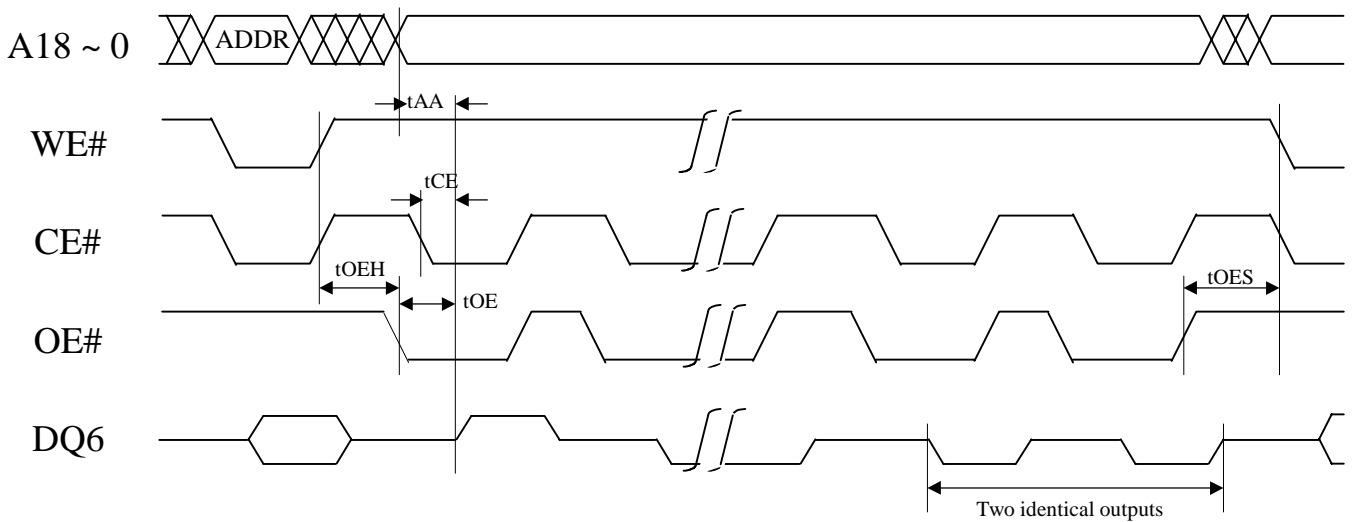
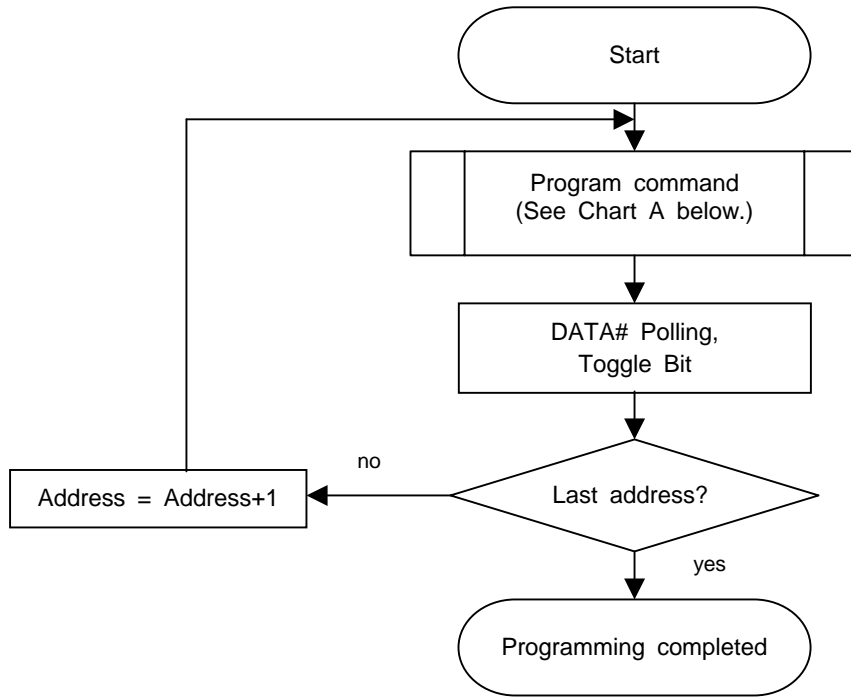


Figure 16: Toggle Bit Timing Chart (DQ6)



Note: Toggle bit output starts 1 "H" all the time.

Figure 17: Byte Program Algorithm



A: Program Command Sequence (Address / Command)

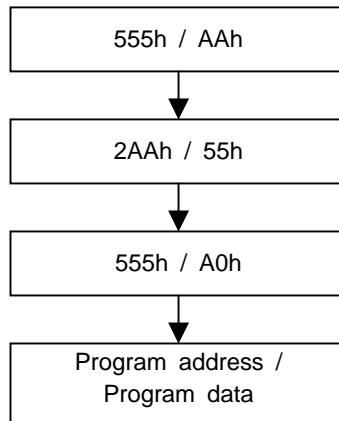
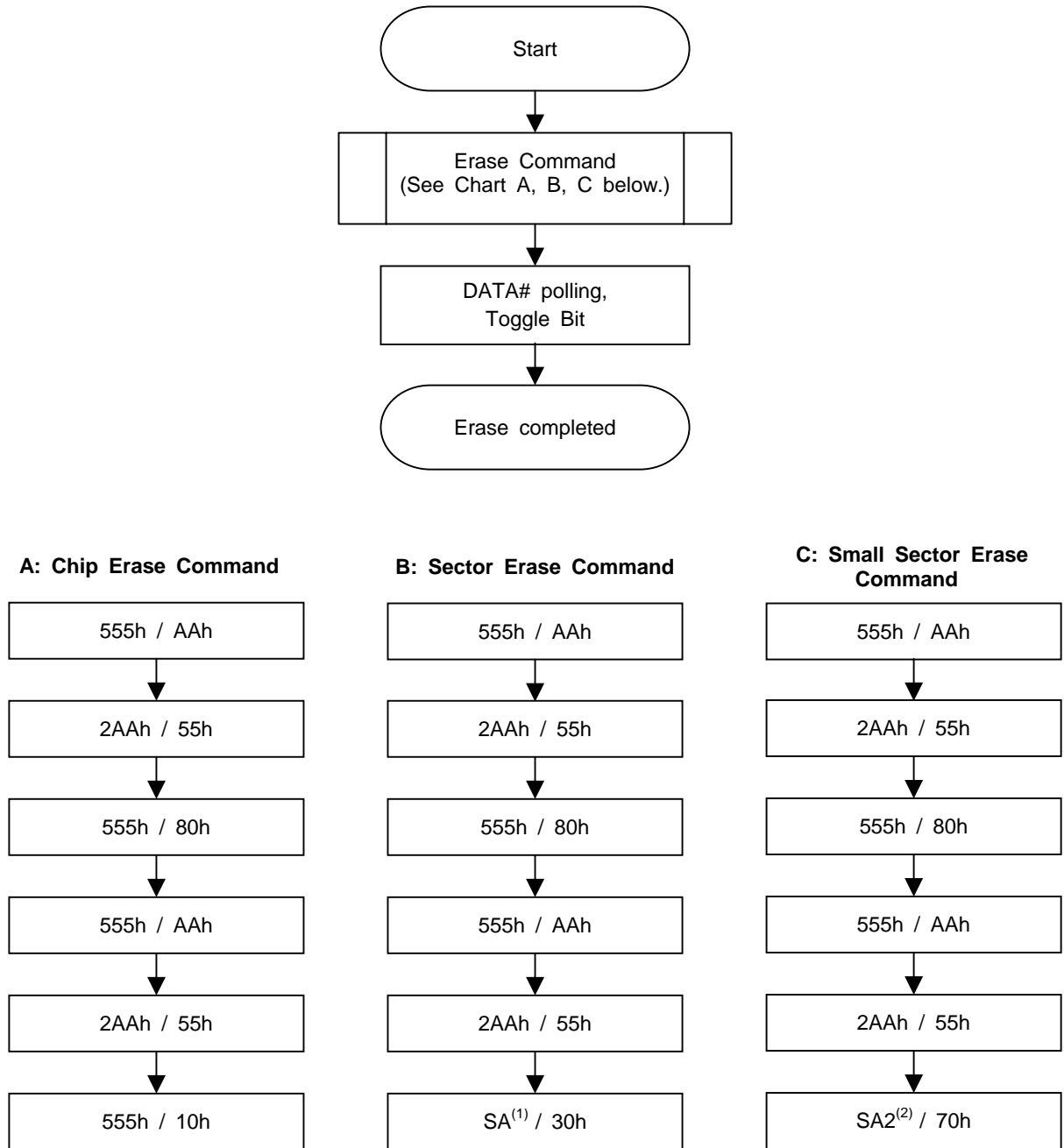


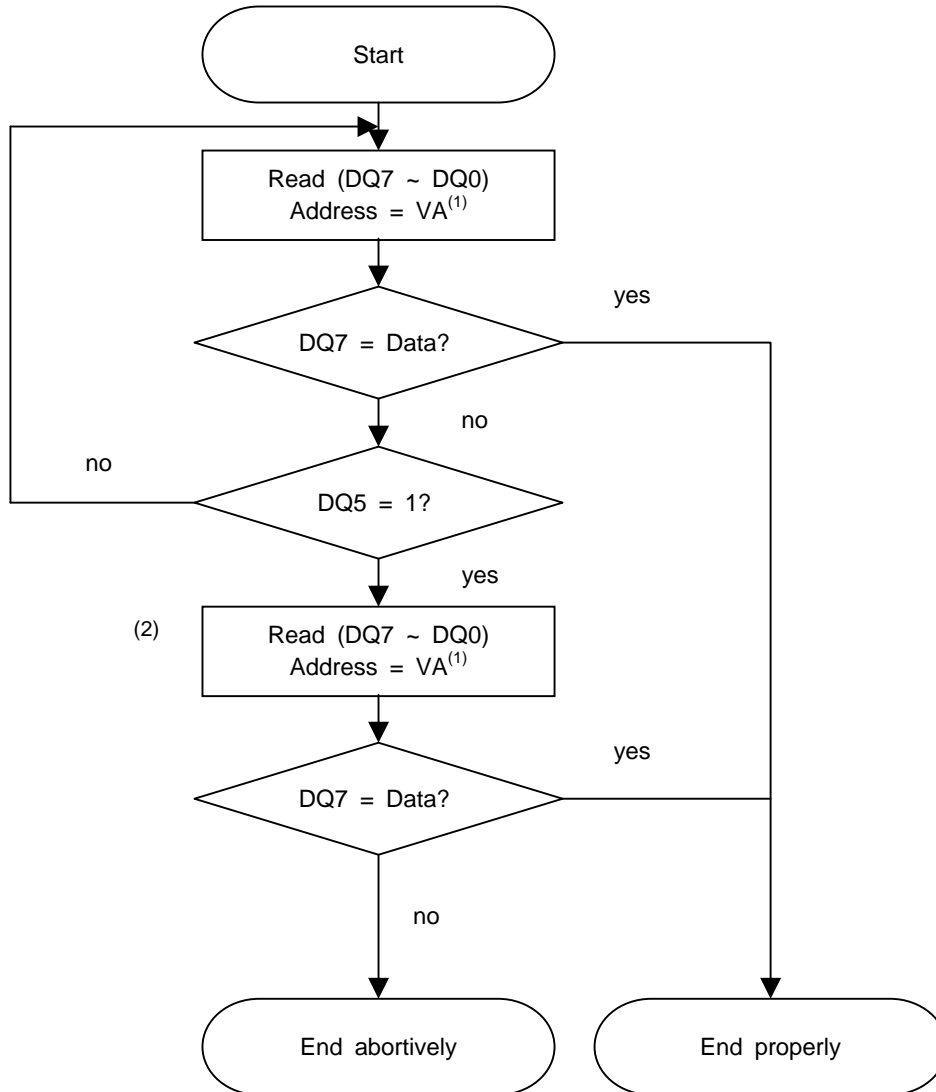
Figure 18: Erase Algorithm



(1) SA: Sector Address = A18 ~ A16

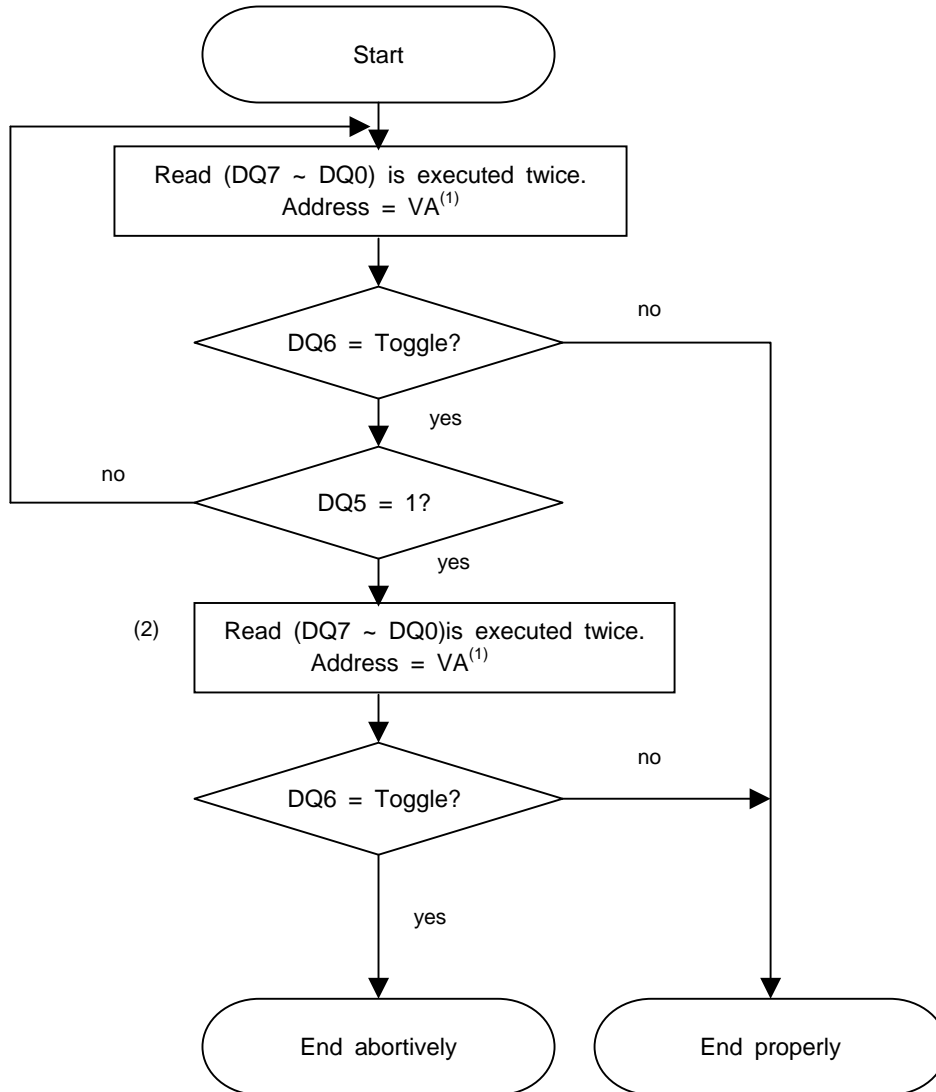
(2) SA2:Small Sector Address = A18 ~ A12

Figure 19: DATA# Polling Algorithm



- (1) VA:
 Programming time: the address that executes programming
 Chip Erase time: a discretionary address
 Sector Erase time: a sector address that executes erasing
 Small Sector Erase time: a small sector address that executes erasing
- (2) The reason why DQ5 outputs 1 might be either the timing limit is exceeded or the erased data is read.
 When DQ5 outputs 1, check DQ7 again to see if it's completed abortively.

Figure 20: Toggle Bit Algorithm



- (1) VA:
 Programming time: the address that executes programming
 Chip Erase time: a discretionary address
 Sector Erase time: a sector address that executes erasing
 Small Sector Erase time: a small sector address that executes erasing
- (2) The reason why DQ5 outputs 1 might be either the timing limit is exceeded or the erased data is read. When DQ5 outputs 1, check DQ6 again to see if it's completed abortively.