Preliminary Specifications

8Mbit (512K ×16-bit / 1024 ×8-bit) Flash memory
LE28FW8203

Description

The LE28FW8203 (hereinafter referred to as 'this device') is a flash memory that consists of 8,388,608bits(524,288Words x 16bits) and it can erase and program due to a 3V-single supply voltage. This device features erase suspend/resume functions with which the device can suspend and resume erase. During erase is suspended, this device can read or program the cells not to be erased. The erase unit is basically 32,768 Words/65,536 Bytes, but erase in a smaller unit, which is 2,048 Words/4,096 Bytes (a small sector), is also possible. Moreover, this device supports the chip batch erase operation that erases a chip entirely and the multiple sector batch erase operation that selects multiple sectors to erase them at a time.

Features

- **Power supply voltage:** 2.7V ~ 3.6V
- **Access time:** Random access: 70ns (Max.)
- **Hardware ID entry**
  SDP command entry and A9 High voltage entry.
  ID read entry by applying high voltage to A9 is possible as well as the same entry by a command input.
- **Power consumption**
  Operation mode (readout): 25 mA (Max.)
  Standby mode: 10 µA (Max.)
- **Detection of program/erase end**
  Device status can be determined by Hardware Sequence Flag (Toggle bit/ Data polling) and RY/BY#.
- **Erase unit**
  Sector: 32K Words/64K Bytes (Sector volume of the boot sector is different.)
  Small sector: 2K Words/4K Byte
  Chip: all the memory cells
- **Package**
  48-pin TSOP (12 mm × 20 mm) Type I Normal bend
  48-ball FBGA (6 mm × 8 mm)
- **Sector protection:** Program/erase can be prohibited in unit of sector in a given range.
- **Multiple sector batch erase**
  After specifying multiple sectors to be erased, all the selected sectors can be erased at a time altogether.
- **Security Sector range**
  2K Word/4K Byte Security sector range are available in total except for the memory cell range
- **Reliability:** W/E endurance: over 10K cycles (Typ. 100K cycles), Data retention period: over 10 years
- **Product Combination**

Part Number	Boot	Package
LE28FW8203T-70T	Top	TSOP48
LE28FW8203T-70B	Bottom	TSOP48
LE28FW8203F-70T	Top	FBGA48
LE28FW8203F-70B	Bottom	FBGA48

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Figure 1: Function diagram

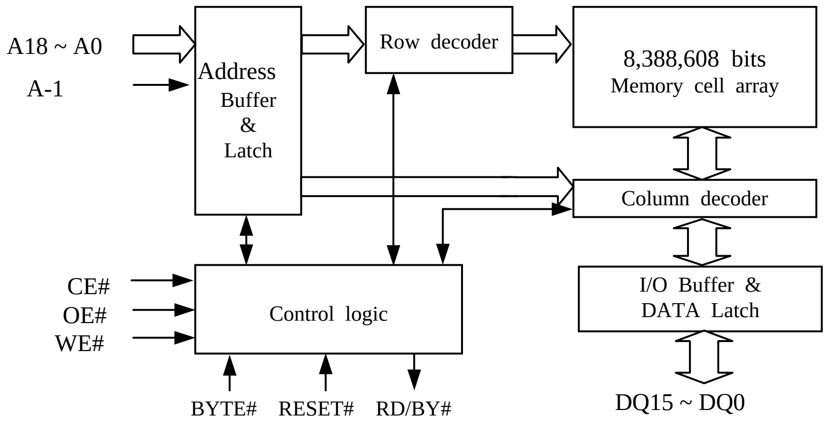
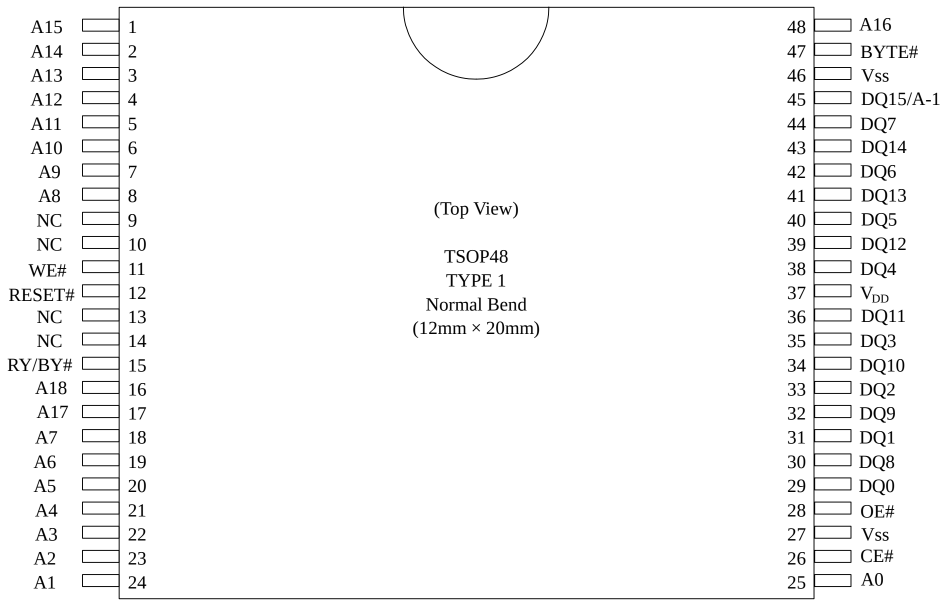


Figure 2: Pin Assignment



(Top View)

	A	B	C	D	E	F	G	H
6	A13	A12	A14	A15	A16	BYTE#	DQ15 /A-1	VSS
5	A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
4	WE#	RESET#	NC	NC	DQ5	DQ12	VDD	DQ4
3	RY /BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
2	A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
1	A3	A4	A2	A1	A0	CE#	OE#	VSS

FBGA48 (6x8)

Table 1: Pin descriptions

Symbol	I/O	Function
A18 ~ A0 A-1	Input	Pins for address input. These address values are latched inside the device during a write cycle. High voltage (VID) is applied to A9 when "sector protection 1" is carried out.
WE#	Input	This pin enables write operation. It's active, when WE# = Low level.
OE#	Input	This pin enables output buffers. It's active, when OE# = Low level. High voltage (VID) is applied to this pin when "sector protection 1" is carried out.
CE#	Input	This pin enables the device. It's active, when CE# = Low level. It's in a standby mode, when CE# = High level.
RESET#	Input	This pin resets the device and sets it into a readout mode. The device is reset, when "RESET# = Low" is input.
BYTE#	Input	This pin switches between Word mode and Byte mode.
RY/BY#	Output	Ready/Busy output
DQ15/A-1, DQ14 ~ DQ0	Input / Output	Data output and input pins. While the device is in a read operation, these pins function as output pins. During a write cycle, these pins function as input pins and are latched inside. When OE or CE# is set to high, DQ shifts to High impedance.
V_{DD}	Power supply	This pin supplies 3.0 V-power voltage (2.7V ~ 3.6V) .
V_{SS}	Ground	This pin supplies 0V.
NC		No connection

Table 2: Pin Input / Output for Each Operation Mode

Operation	CE#	OE#	WE#	A0	A1	A2	A3	A4	A5	A6	A7	A9	DQ15 ~ 0	RESET#
Manufacturer Code (1)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{ID} (4)	(0062h)	V_{IH}
Device Code (1)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{ID} (4)	(002Dh)	V_{IH}
Read	V_{IL}	V_{IL}	V_{IH}	A0	A1	A2	A3	A4	A5	A6	A7	A9	D_{OUT}	V_{IH}
Standby	V_{IH}	X	X	X	X	X	X	X	X	X	X	X	High-Z	V_{IH}
Output Disable	X	V_{IH}	V_{IH}	X	X	X	X	X	X	X	X	X	High-Z	V_{IH}
Write (Erase/Program)	V_{IL}	V_{IH}	V_{IL}	A0	A1	A2	A3	A4	A5	A6	A7	A9	D_{IN}	V_{IH}
Write Disable	X	V_{IL}	X	A0	A1	A2	A3	A4	A5	A6	A7	A9	D_{OUT}	V_{IH}
	X	X	V_{IH}	A0	A1	A2	A3	A4	A5	A6	A7	A9	High-Z / D_{OUT}	V_{IH}
Sector Protection 1(1)	V_{IL}	V_{ID} (4)	Low Pulse(3)	V_{IL}	V_{IH}	X	X	X	X	V_{IL}	X	V_{ID} (4)	X	V_{IH}
Readout of Sector Protection Information(1)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	V_{IL}	X	V_{ID} (4)	(Table 3)	V_{IH}
Sector protection suspend (1)	X	X	X	X	X	X	X	X	X	X	X	X	X	V_{ID} (4)
Hardware Reset	X	X	X	X	X	X	X	X	X	X	X	X	High-Z	V_{IL}

(1) Reading a device code and a manufacturer code, protecting sectors, reading sector protection information and suspending sector protection can also be done by command input. Refer to **Table 3 Software Command Sequence** for those operations by command input.

(2) "X" in this table indicates V_{IL} or V_{IH}.

(3) 100μs- low pulses. Refer to **Figure 23**

(4) V_{ID} indicates High voltage.

Basic Function Description

Refer to the following descriptions, and timing diagrams or algorithms specified in descriptions of each item.

(1) Read Operation

For data readout, both CE# and OE# should be set to a low level. If CE# is set to a high level, the chip gets deselected. OE# functions as a gate to determine whether inner output should be sent to outside. If it is set to a high level, it prohibits output and the output pins turn to a high impedance state. For the details, refer to the **Readout Timing Chart (Figure 3)**.

This device has a self-power save function, with which the device automatically turns to a standby status if address input doesn't change for more than 150ns during normal cell readout. Consequently I_{DD} becomes 2μA (typ). Due to this function, the I_{DD} value during readout changes to 1mA / MHz (typ) that corresponds to an operation frequency. Once an address or any input of a control pin has changed, the self-power save is automatically cleared. This self-power save function doesn't lead to a longer access time.

(2) ID read operation

ID read operation reads ID code (manufacturer code and device code). With this function, the device can be identified from outside. This operation is used, for example, to automatically set a program sequence for programming with a PROM writer. Two ways of ID code readout are available in this device. The contents of the code to be read compile with **ID code table (Table 4)**. The readout timing is the same as that of memory cell readout.

-a Hardware ID Read Operation

The hardware ID read operation reads ID code by applying high voltage to A9. (V_{ID}). Typically, this is used when PROM writer executes ID code readout. From the lower address of 00h and 01h, a manufacturer code and a device code are read respectively. By canceling the high voltage in A9, the read operation is restored. For the input waveform at the hardware ID readout, refer to the **Hardware ID read timing chart (Figure 12)**.

-b Software ID read operation

The software ID read operation reads the device code without applying high voltage to a chip. Since ID code can be read without applying high voltage to the address bus, this is effective to identify the device incorporated in the set. To execute the software ID read, command input of 4-bus cycle is required. In the 4th bus cycle, input 00h or 01h to the lower address. From the addresses of 00h and 01h, the manufacturer code and the device code are read respectively. To clear the Software ID read operation, the reset command must be input. For the waveform at the software ID read, refer to the **Software ID read timing chart (Figure 13-a)**. To clear the software ID read mode and to read regular cells, **Reset Operation ((5)-a, (5)-b)** must be executed. The software ID read operation can not be executed when the device is set to the **(3)-b Fast Program Mode** or **(10) Security Sector Mode**.

Table 4 :ID code

Type		BYTE#	A7 ~ A0	A-1	Code (HEX)
Top Boot	Manufacturer code	H	00h	X	0062h
		L		L	62h
	Device Code	H	01h	X	002Dh
		L		L	2Dh
Bottom Boot	Manufacturer code	H	00h	X	0062h
		L		L	62h
	Device Code	H	01h	X	002Eh
		L		L	2Eh

-c Common Flash Interface

This device contains the CFI information to describe the characteristics of the device. To execute the CFI Entry, command input of only 1-bus cycle is required. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in **Table 10-a to 10-d**. For the waveform at the CFI, refer to the **CFI Mode Enrry timing chart (Figure 13-b)**. To clear the CFI mode and to read regular cells, **Reset Operation ((5)-a, (5)-b)** must be executed. The CFI operation can not be executed when the device is set to the **(3)-b Fast Program Mode** or **(10) Security Sector Mode**.

Table 3-a: Software Command Sequence (BYTE# = H Word Mode)

Command Sequence	Bus Write Cycle	1st Bus		2nd Bus		3rd Bus		4th Bus		5th Bus		6th Bus	
		address	data	address	data	address	data	address	data	address	data	address	data
Read/Reset A**	1	XXXh	F0h	RA(1)	RD(2)								
Read/Reset B**	3	555h	AAh	2AAh	55h	555h	F0h	RA(1)	RD(2)				
ID Read	3	555h	AAh	2AAh	55h	555h	90h	IA(3)	ID(4)				
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA(5)	PD(6)				
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA(7)	30h
Small Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA2(8)	70h
Erase Suspend	1	XXXh	B0h										
Erase Resume	1	XXXh	30h										
Sector Protection***	3	XXXh	60h	SPA(9)	60h	SPA(9)	40h	SPA(9)	SPD(10)				
Sector Suspend	4	555h	AAh	2AAh	55h	555h	E0h	XXXh	01h				
Reset of Sector Suspend	4	555h	AAh	2AAh	55h	555h	E0h	XXXh	00h				
Read of Sector Protection Suspended status	3	555h	AAh	2AAh	55h	555h	90h	TA(11)	TD(12)				
Read of Sector Protection Information	3	555h	AAh	2AAh	55h	555h	90h	SPA(9)	SPD(10)				
Fast Program Set	3	555h	AAh	2AAh	55h	555h	20h						
Fast Program	2	XXXh	A0h	PA(5)	PD(6)								
Fast Program Reset	2	XXXh	90h	XXXh	F0h 00h								
Security Sector Entry	3	555h	AAh	2AAh	55h	555h	88h						
Security Sector Program	4	555h	AAh	2AAh	55h	555h	A0h	PA(5)	PD(6)				
Security Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SHRA( )	30h
Security Sector Reset	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h				
CFI Entry	1	555h	98h										

note:

* Valid address pins for inputting command codes are A10 ~ A0. The least significant address is A0, and the valid DQs are DQ7 ~ DQ0.
* Addressed and data are shown in hexadecimal.
* XXXh indicates a discretionary address.
** Two kinds of read/reset command function are identical, and the both set the device to the readout mode.
*** To protect a sector by Software Command Sequence, RESET# must be set to V_{ID} during command input.

Brevity code descriptions of Address/Data
(1) RA: read address
(2) RD: output data of readout
(3) IA: ID read address (A7, A6, A5, A4, A3, A2, A1, A0)
(4) ID: ID code output (Manufacturer code = 0062h Device Code = 002Dh (Top Boot), 002Eh (Bottom Boot))
(5) PA: program address
(6) PD: program input data
(7) SA: sector address (A18, A17, A16, A15, A14, A13, A12)
(8) SA2: small sector address (A18, A17, A16, A15, A14, A13, A12, A11)
(9) SPA: sector protection address (A18, A17, A16, A15, A14, A13, A12, A6, A1, A0)
(10) SPD: readout data of sector protection status
(11) TA: readout address of sector protection suspended status (A6, A1, A0)
(12) TD: readout data of sector protection suspended status

Table 3-b: Software Command Sequence (BYTE# = L Byte Mode)

Command Sequence	Bus Write Cycle	1st Bus		2nd Bus		3rd Bus		4th Bus		5th Bus		6th Bus	
		address	data	address	data	address	data	address	data	address	data	address	data
Read/Reset A**	1	XXXh	F0h	RA(1)	RD(2)								
Read/Reset B**	3	AAAh	AAh	555h	55h	AAAh	F0h	RA(1)	RD(2)				
ID Read	3	AAAh	AAh	555h	55h	AAAh	90h	IA(3)	ID(4)				
Program	4	AAAh	AAh	555h	55h	AAAh	A0h	PA(5)	PD(6)				
Chip Erase	6	AAAh	AAh	555h	55h	AAAh	80h	AAAh	AAh	555h	55h	AAAh	10h
Sector Erase	6	AAAh	AAh	555h	55h	AAAh	80h	AAAh	AAh	555h	55h	SA(7)	30h
Small Sector Erase	6	AAAh	AAh	555h	55h	AAAh	80h	AAAh	AAh	555h	55h	SA2(8)	70h
Erase Suspend	1	XXXh	B0h										
Erase Resume	1	XXXh	30h										
Sector Protection***	3	XXXh	60h	SPA(9)	60h	SPA(9)	40h	SPA(9)	SPD(10)				
Sector Protection Suspend	4	AAAh	AAh	555h	55h	AAAh	E0h	XXXh	01h				
Reset of Sector Protection Suspend	4	AAAh	AAh	555h	55h	AAAh	E0h	XXXh	00h				
Read of Sector Protection Suspended Status	3	AAAh	AAh	555h	55h	AAAh	90h	TA(11)	TD(12)				
Read of Sector Protection Information	3	AAAh	AAh	555h	55h	AAAh	90h	SPA(9)	SPD(10)				
Fast Program Set	3	AAAh	AAh	555h	55h	AAAh	20h						
Fast Program	2	XXXh	A0h	PA(5)	PD(6)								
Fast Program Reset	2	XXXh	90h	XXXh	F0h 00h								
Security Sector Entry	3	AAAh	AAh	555h	55h	AAAh	88h						
Security Sector Program	4	AAAh	AAh	555h	55h	AAAh	A0h	PA(5)	PD(6)				
Security Sector Erase	6	AAAh	AAh	555h	55h	AAAh	80h	AAAh	AAh	555h	55h	SHRA( )	30h
Security Sector Reset	4	AAAh	AAh	555h	55h	AAAh	90h	XXXh	00h				
CFI Entry	1	AAAh	98h										

note:

* Valid address pins for inputting command codes are A10 ~ A0 and A-1. The least significant address is A-1, and the valid DQs are DQ7 ~ DQ0.
* Address and data are shown in hexadecimal.
* XXXh indicates a discretionary address.

** Two kinds of read/reset command function are identical, and the both set the device to the readout mode.

*** To protect a sector by Software Command Sequence, RESET# must be set to V_{ID} during command input.

Brevity code descriptions of Address/Data

(1) RA: read address
(2) RD: output data of readout
(3) IA: ID read address (A7, A6, A5, A4, A3, A2, A1, A0)
(4) ID: ID code output (Manufacturer code = 62h, Device Code = 2Dh (Top Boot), 2Eh (Bottom Boot))
(5) PA: program address
(6) PD: program input data
(7) SA: sector address (A18, A17, A16, A15, A14, A13, A12)
(8) SA2: small sector address (A18, A17, A16, A15, A14, A13, A12, A11)
(9) SPA: sector protection address (A18, A17, A16, A15, A14, A13, A12, A6, A1, A0)
(10) SPD: readout data of sector protection status
(11) TA: readout address of sector protection suspended status (A6, A1, A0)
(12) TD: readout data of sector protection suspended status

(3) Program Operation

The program operation rewrites a target memory from '1' data to '0' data. In this device, programming can be executed in units of word (16bits) or byte (8bits).

-a Word(Byte) Program Operation

This device can execute the program operation in units of word (16bits) or byte (8bits). This operation is called as the word (byte) program operation. This operation is done by setting OE# to a high level and inputting the word (byte) program command that consists of 4 bus cycles. As the word (byte) program is executed only to the memory cells in the erase status, the target sectors for the word (byte) program must be erased in advance. The target program address is set in units of word (byte). The address is latched into the memory at falling edge of WE# and the program data is latched at rising edge of WE#. As for the input waveform at the word (byte) program, the contents of input command and outline of the word (byte) program operation, refer to the **Word(byte) Program Timing Chart (Figure 6)**, the **Software Command Sequence (Table 3)** and the **Word(byte) Program Algorithm (Figure 18)** respectively.

To simplify the descriptions, this spec only explains the way of controlling by the rising and the falling edge of WE#. However, the rising and the falling edge of CE# can also realize the same operation.

-b Fast Word(Byte) Program Operation

This device has a function of fast word (byte) program, aside from a programming method that inputs 4-bus command in units of word (byte) **(-a Word(Byte) Program Operation).** This function omits the first 2 bus cycles in the program so that the program could be finished within two command cycles. Inputting a fast program set command that consists of 4 bus cycles, this device enters the fast word (byte) program operation mode. As a result, the rest of program can be done within 2 bus cycles. As for the command to set the fast word (byte) program and the outline of the operation flow, refer to the **Software Command Sequence (Table 3)** and the **Fast Word(byte) Program Algorithm (Figure 19)** respectively. The fast word (byte) program can be canceled either by inputting the fast program reset command listed in the **Software Command Sequence Table (Table 3)**, by executing the **Hardware Reset ((5) -a)** or by providing power again.

(4) Erase Operation

The erase operation rewrites the data from 0 to 1. Three kinds of word unit for erase are available. The first one is a chip erase operation that erases entire memory of a chip. The second one is a sector erase operation that erases in units of 32K Word/64K Byte (As for a boot sector, the erase unit would be either of 4K Word /8K Byte, 8K Word/16K Byte, or 16K Word/32 K Byte, based on a sector address listed in **Sector Address Table(table 9)**.). The third one is a small sector erase operation that can erase in units of 2K Word/4K Byte. To execute each erase operation, it is required to set OE# to a high level and to input the SDP erase command that consists of six bus cycles. For details of input at the erase operation, refer to the three kinds of **Erase Timing Charts (Figure 7, Figure 8,** and **Figure 9)** and the **Software Command Sequence (Table 3)**.

-a Chip Erase Operation

The chip erase operation rewrites the entire data of the flash memory to 1 data, and it starts by inputting of the SDP command sequence of 6 bus cycles. After the command sequence is input, erase is automatically carried out in units of sector within the device. When all the sectors are erased, the operation terminates. For details, refer to the **Chip Erase Timing Chart (Figure 7),** the **Software Command Sequence (Table 3)** and the **Erase Algorithms (Figure 20)**. This chip erase operation requires no advance programming by users. Thus, the erase time is given by the expression Chip Erase Time = Sector Erase Time × Sector Count.

-b Sector Erase / Multiple Sector Batch Erase Operation

The sector erase operation rewrites data in a given sector (32K Word/64K Byte) or boot sector range to 1. A certain address of the sector addresses from SA0 to SA18 listed in the **Sector Address Table (Table 9)** is rewritten. T**he erase operation is automatically executed to a designated sector within the device, which starts by inputting the SDP command sequence of 6 bus cycles. For details**, refer to the **Sector Erase Timing Chart (Figure 8-a)**, **Software Command Sequence (Table 3)** and the **Erase Algorithms (Figure 20)**. The **Multiple Sector Erase** erases multiple sectors simultaneously by repeating the final bus cycle of the sector erase command to input each sector address and the final bus command (30h). For this function, the bus cycle must be repeatedly input during the sector erase hold time (tSEDH). When any command except for the sector erase command (30h) or erase suspend command (B0h) is input during the sector erase hold time, the device resets inner command registers and is set to the read mode. For details, refer to **Multi-Sector Erase Timing Chart (Figure 8-b).** In this case, the erase time is calculated by the expression Multiple Sector Batch Erase Time = Sector Erase Time × the number of erase sectors.

Same as **Chip Erase (-a)**, the sector erase /multiple sector batch erase requires no advance programming for the target sector by users.

-c Small Sector Erase Operation

The small sector erase operation rewrites data in a given small sector (2K Word/4K Byte) to 1. Each sector from SA0 to SA18 listed in the **Sector Address Table (Table 9)** is from 4k to 32K Words /64K Bytes in size. However, the small erase operation can erase in units of 2K Word /4K Byte regardless of these sector allocation. The way to start by inputting the SDP command sequence of 6 bus cycles is the same as that of the sector erase operation, but the final bus commands are not identical. It is impossible to erase multiple small sectors at a time. For details of the input at the small sector erase operation, refer to the **Small Sector Erase Timing Chart (Figure 9),** the **Software Command Sequence (Table 3)** and the **Erase Algorithms (Figure 20)**. The small sector erase also requires no advance programming for the target sector.

(5) Reset Operation

The reset operation is available in this device to recover from an abortive end of an automatic operation or to initialize the read mode. There are two kinds of reset operation: the hardware reset and the read reset.

-a Hardware Reset

This device can reset its function by setting RESET# to a low level. To complete the hardware reset, RESET# must be kept low at least during the tRP time. While RESET# is in a low level, all of DQ are in the high impedance state. Concerning the input setting at the hardware reset, refer to the **Hardware Reset Timing Chart (Figure 17)**. To start readout after the hardware reset, you need to set RESET# to a high level and wait at least for the tRY time. When the hardware reset is completed, the device is set to **Read mode (1)** regardless of the adjacent mode.

When the hardware reset is carried out during an automatic erase or program operation, its address data get unsettled.

-b Read Reset

This device has two kinds of read reset commands as listed in the **Software Command Sequence (Table 3)** to set the mode back to the read mode, when an automatic operation ends abortively as the timing limited is exceeded **((11)-c)** during its internal operation and consequently the device gets locked. As for the input waveform at the reset operation, refer to the **Read Reset Timing Chart (Figure 14)**. The functions of these two read reset commands are identical. By executing these read reset, it is also possible to shift the ID read mode to the readout mode of normal cells in addition to restore the device from an abortive end of an automatic operation. However, the device cannot be set to the readout mode by suspending program or erase operation. When the read reset is effectively done, this device is set to the read mode. **Table 5** shows the differences between **-a Hardware Reset** and **-b Read Reset**.

Table 5: Difference between Hardware Reset and Read Reset

Function	Read Reset	Hardware Reset
Termination of ID Read mode	Possible	Possible
Clearing of a command register	Possible	Possible
Unlock when an automatic operation ends abortively	Possible	Possible
Abortion of an automatic operation	Impossible	Possible
Reset of sector protection suspend	Impossible	Possible
Termination of readout mode of sector protection information	Possible	Possible
Termination of read mode of sector protection suspend	Possible	Possible

(6) Erase Suspend / Resume

This device can execute erase suspend / erase resume only while the device is in the sector erase mode. The erase suspend mode makes it possible to suspend an erase operation, to read from the sectors that are not selected as an erase mode and to execute a program to those sectors. The commands available in the erase suspend mode are **(3)-a Word(byte) program, (3)-b Fast Word(byte) program, (2)-b Software ID Readout, (5)-b Read Reset** and **Resume Command** that aborts the suspend mode.

The erase suspend mode is enabled by inputting an erase suspend command listed in **Software Command Sequence Table(Table.3**) while **(4)-b Sector Erase / Multiple Sector Batch Erase** is being operated, which includes the sector erase hold time(tSEDH). When the erase suspend time (tSUSE) has passed after the erase suspend command is input, the device enters the erase suspend mode. Whether the device enters the erase suspend mode can be checked by **the Hardware Sequence Flag**. As for the input waveform at the erase suspend, see **Erase Suspend Timing Chart** (Figure 10).

When sectors are continuously read while the erase operation is in progress, DQ6 toggles. On the other hand, when sectors that suspend an erase operation are continuously read in the erase suspend mode, DQ2 toggles instead of DQ6. RY/BY# turns to a high impedance state.

During the erase is suspended, **(3)-a Word (byte) Program, (3)-b Fast Word(byte) Program, (2)-b Software ID Read, and (5)-b Read Reset** can be applied to the sectors not under the erase mode in the same way as usual programs. The erase operation cannot be executed to other sectors during the erase suspend time.

To stop the erase suspend and to resume the erase operation, input an erase resume command listed in **Software Command Sequence Table (Table 3)**. As for the waveform at the erase resume, see **Erase Resume Timing Chart (Figure 11)**. When the erase suspend is executed during the erase hold time, the device enters the erase hold time (tSEDH) again if the resume command is executed and received validly. During the erase hold time, an erase sector of **Multiple Sector Batch Erase Operation** can be added. After the erase hold time, DQ6 restart toggling and RY/BY# outputs 0. When the erasing operation is suspended and the resuming operation is received validly, the device returns to the erase period, DQ6 restarts toggling and RY/BY# outputs 0.

(7) Sector Protection

This device has a sector protection function that prohibits program and erase in units of sector. When sector protection is applied to a certain sector, program and erase become impossible to the protected sector. When shipped, all the sectors of this device are not protected.

-a Sector Protection

There are two ways available to protect sectors. Protection 1 is to apply the high voltage to OE# and A9 to protect sectors. The flow of execution is described in **Sector Protection 1 Algorithm (figure 23).** Protection 2 is to apply the high voltage V_{ID} to RESET# and then to input a sector protection command listed in **Software Command Sequence Table (Table 3).** The flow of execution is described in **Sector Protection 2 Algorithm (figure 24).** Whether the protection is completed can be checked by **–c Reading of Sector Protection Information.** Be aware that this sector protection setting cannot be executed during the fast program mode.

-b Sector Protection Suspend

There are two ways of sector protection suspend available in order to program or erase a protected sector. One is simply to apply the high voltage to RESET# to suspend sector protection. The other is to input a sector protection suspend command that consists of 4 bus cycles listed in **Software Command Sequence Table (Table 3).** By these functions, program and erase can be executed to a protected sector without losing sector protection information. Whether the device is in the sector protection suspended status or not can be checked by **Sector Protection Suspend Read**. This can be executed by inputting the readout command of sector protection suspended status listed in **Software Command Sequence Table (Table 3).** If the sector protection suspend is set by inputting a command, **Sector Protection Suspend Reset** need to be done to get the device back to the sector protection status. For resetting, a reset command of the sector protection suspend listed in **Software Command Sequence Table (Table 3)** is used. When sector protection suspend is set by inputting a command, you need to be careful as the sector protection suspended status continues unless you reset the sector protection suspend, feed power again, or execute **Hardware Reset ((5)-a)**. Consequently, the program and the erase operation can be doneto any protected sector except for the ones in a security sector area. When sector protection is suspended by applying the high voltage to RESET#, the sector protection suspended status is reset by canceling the high-voltage setting to RESET#.

The sector protection suspend by the sector protection suspend command is impossible, if the suspend operation is set in **(3)-b Fast Word (byte) Program** mode or set in **(10) Security Sector** mode. Even if the sector protection suspend is set, the contents of the security sector are retained. Therefore, it is impossible neither to erase the data contained the security sector nor to write additional data to the same.

-c Readout of Sector Protection Information

With the readout function of sector protection information, you can see whether a sector you are going to access is under sector protection. There are two ways available. One is to input the readout command of sector protection information listed in **Software Command Sequence Table (Table 3)**. The other one is to apply the high voltage to A9. Each pin condition is indicated in **Pin Input/Output For Each Operation Mode (Table 2).** The codes to be read are listed in **Readout of Sector Protection Information (Table 6)**.

To cancel the readout mode of sector protection information, you need to feed power again, or execute **Hardware Reset (5)-a** or **Read Reset (5)-b.**

Table 6: Readout of sector protection information

Readout contents	A18 ~ A12	A6	A3	A2	A1	A0	Code(HEX)
Readout of sector protection information	SA(1)	L	L	L	H	L	01h(protection) / 00h(non-protection)(2)
Readout of sector protection Suspend information	Doesn't matter (Any value will do.)	L	L	L	H	H	01h(suspend) / 00h(non-suspend)

(1) Sector address to be read.
(2) The values of lower 8 bits are indicated.

(8) Hardware Data Protection

This device can protect sectors by the hardware and the software. Hardware data protection function protects data from being erased accidentally or unexpected programming, and command input is not necessary.

-a Preventing Low VDD Program Erase

The function of prohibiting programming in the low VDD is to prohibit receiving commands when VDD is 1.5V or less, to stop an inner automatic operation, and to prevent data from being rewritten. This function protects data from an unexpected program that might occur when the power-supply voltage is low.

-b Preventing Gritty Malfunction

To protect data from an unexpected program of the device due to gritty, a pulse below 5ns to be added to WE# is designed to be ignored. When a gritty that exceeds 5ns is input, malfunctions might occur.

-c Preventing Malfunction When Power is Provided

When power is provided, program and erase operations are prohibited by retaining either of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. Be sure to keep this status, when you provide or cut off power.

(9) Software Data Protection (SDP)

In this device, a compatible command of JEDEC-standard type is input to activate program or erase operation. In this method, all the write operation (program/erase) requires multiple inputs of bus commands to be added to address pins and DQ. In a JDEC-standard command, DQ input is a byte-format (8 bits from DQ0 to DQ7), but this device consists of Words from DQ0 to DQ15. When a command is input, the Words from DQ8 through DQ 15 are ignored.

While a command is input, which is WE# = H, loading operation of inner commands are suspended. Thus reading is possible during this period.

When a command sequence is rejected: incorrect addresses or data are loaded for instance, the device goes back to the readout mode. In this case, the device returns to the readout mode within tRC after the incorrect addresses or data are input.

(10) Security Sector Range

This device has a security sector range of 2K Word/4K Byte (32K bits) on the topside apart from a memory cell range. To access the security sector range and to read, to program, or to erase, you need to input a security sector entry command listed in **Software Command Sequence Table (Table 3)** to shift the device mode to a security sector mode. To cancel the security sector mode, you need to input a security sector reset command listed in **Software Command Sequence Table (Table 3)** or provide power again, or execute **Hardware Reset ((5)-a)**.

Readout, program, erase and protecting a security sector range are possible in the security sector mode. Inputting a security sector program listed in **Software Command Sequence Table (Table 3)** and a security sector erase command, program and erase can be executed in the same way as in a usual memory cell range. When program or sector erase are to be done, in case of Top Boot Product, the addresses from A11 through A18 in the final bus cycle must be all set to 1. And in case of Bottom Boot Product, the addresses from A11 through A18 in the final bus cycle must be all set to 0. The address values are overlapped with the ones at accessing the usual memory cell. When a security sector entry is done, the security sector range must be internally accessed. On the contrary, when a security sector entry is not done, the usual memory cell range must be internally accessed.

The address range that can be specified in the security sector mode is shown in **Security Sector Address Table (Table 7)**. The range consists of 2K Word/4K Byte on the topside, but this is treated as 1 sector, which is the unit of erase operation. Therefore, to erase the security sector range means that all the cells within the security sector are erased.

Protecting the security sector range is done in the same way as in the usual cell except for setting RESET# to V_{IH} instead of the high voltage (V_{ID}) in the security sector entry mode. However, it is impossible to suspend protection to the security sector. In short, as far as the security sector is concerned, once protection has been done, rewriting becomes impossible.

During the security sector mode, it is possible to read the sectors except for SA18 (in case of Bottom Boot Product SA0). Be aware that if you specify an address outside of the security sector range during the security sector mode and execute a security sector program and a security sector erase, that action might affect the memory cells outside of the security sector range and the sector protection information.

Table 7: Security Sector Address Table (HRA)

Product	Data width	Address	Capacity
Top Boot	Word mode, when (BYTE# = H)	7F800h ~ 7FFFFh	2K Word
	Byte mode, when (BYTE# = L)	FF000h ~ FFFFFh	4K Byte
Bottom Boot	Word mode, when (BYTE# = H)	00000h ~ 007FFh	2K Word
	Byte mode, when (BYTE# = L)	00000h ~ 00FFFh	4K Byte

(11) Hardware Sequence Flag

This device automatically executes erase and program operations. The hardware sequence flag indicates whether these automatic operations complete correctly based on the output of the data pins. The hardware sequence flag can be read at the same level of reading timing by lowering the CE# and OE# level during writing. For information such as what a certain data indicates or in which pin a certain data is output, see **Hardware Sequence Table (Table 8)**.

When the hardware sequence flag indicates that automatic writing is completed, the device automatically returns to the readout mode.

Actual writing is automatically completed with its inner timer. DATA# polling and a toggle bit occur upon completion of inner writing. After these two occur, this device outputs a status different from the one before the writing through DQ6 and DQ7 to inform outside that writing is completed. Reading twice the address to be written additionally can avoid rejecting the device by the false decision. The fact that in both two cases the data read from these DQ6 or DQ7 is found valid indicates the program cycle is completed correctly. When the data is found otherwise, that indicates the program isn’t completed correctly.

Table 8: Hardware Sequence Flag Table

Status				DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
Automatic Operation	Automatic Program			DQ7#	Toggle	0	0	1	0
	Erase mode	Erase hold time(6)	Selected sector(1)	0	Toggle	0	0	Toggle (5)	0
			Non-selected sector(2)	0	Toggle	0	0	1	0
		Erase operation	Selected sector(1)	0	Toggle	0	1	Toggle (5)	0
			Non-selected sector(2)	0	Toggle	0	1	1	0
	Erase suspend mode	Readout	Selected sector (3)	1	1	0	0	Toggle	High-Z
			Non-selected sector (4)	Data	Data	Data	Data	Data	High-Z
		Program	Selected sector (3)	DQ7#	Toggle	0	0	Toggle	0
			Non-selected sector (4)	DQ7#	Toggle	0	0	1	0
Timeout	Program			DQ7#	Toggle	1	0	1	0
	Erase			0	Toggle	1	1		0
	Program during erase suspend			DQ7#	Toggle	1	0		0

(1) When the hardware sequence flag is read in the sector to be erased.
(2) When the hardware sequence flag is read in the sector not to be erased but located in the same bank as the sector to be erased.
(3) When the hardware sequence flag is read in the sector to be erased and also under suspending.
(4) When the hardware sequence flag is read in the sector to be erased but not under suspending, and that is located in the same bank as the sector under suspending.
(5) DQ2 doesn't toggle at the time of the small-sector erase and Security Sector range-sector erase, and H level is output.
(6) It is only under the sector erase that the hardware sequence flag can be read during the erase hold time.

-a DATA# Polling (DQ7)

When you read the data (See **DATA# Polling Timing Chart (Figure 15))** during an internal automatic program, the inversed data of the one that finally executed programming is read from DQ7. When you read the data after the inner automatic program is completed, the data that finally executed programming is read from DQ7. The output of DATA# polling becomes valid after the rising edge of WE# (or CE#) of the final bus cycle in the automatic operation command sequence. When you read while the inner automatic erase is operating, 0 is read from DQ7. When you read after the same is completed, 1 is read from DQ7.

-b Toggle Bit (DQ6)

When you repeat reading while this device is in automatic program status or erase status inside, DQ6 outputs 0 and 1 by turns. (**See Toggle Bit Timing Chart (Figure 16).)** When inner automatic operation is completed correctly, outputting by turns stops and this device gets ready for accepting the next operation. The output of toggle bit becomes valid after the rising edge of WE# (or CE#) of the final bus cycle in the automatic operation command sequence.

-c Exceeding Timing Limit (DQ5)

When you read data while a programming or erasing is internally carried out, 0 is output from DQ5. When erase time exceeds the designated value, DQ5 outputs 1 regardless of the contents of cell data that corresponds to DQ5. (Exceeding of timing limit) The fact that DQ5 outputs 1 indicates that inner automatic operation doesn't end properly. Which also indicates that a part of this device might be defective. Once the status signal indicating exceeding of timing limit has been output, the output continues unless you provide power of the device again, or you execute **Hardware Reset ((5)-a)** or **Read Reset ((5)-b).** Even when the inner erase is done correctly within the designated time, DQ5 sometimes outputs 1. This is because DQ5 outputs the erased data. You could know whether data of 1 output from DQ5 indicates exceeding of timing limit or indicates the read data of a cell by checking whether either DATA# polling or the output signal of the toggle bit indicates the end of writing.

-d Sector Erase Timer (DQ3)

As shown in (4)-b, this device can erase multiple sectors simultaneously by repeating the 6th bus cycle of the sector erase during erase hold time. DQ3 indicates whether the device is in the erase hold status, when multiple sector batch erase is executed. When the 6th bus cycle of the sector erase command is input and the device shifts to the erase hold status, DQ3 outputs 0 indicating that additional address input is acceptable. When the address erase hold time is finished and the device doesn't receive new addresses any more, 1 is output. Then erase operation automatically starts within the device, which means new addresses cannot be accepted any more.

-e Toggle Bit 2 (DQ2)

When you repeat reading in a given sector under sector erase operation or under chip erase operation, DQ2 outputs 0 and 1 by turns. When a sector not to be erased is selected and the sector is continuously read, DQ2 outputs 1. Seeing the output difference of DQ2, you could know if the sector you selected is to be erased or not. In case of small sector erase, DQ2 under erase operation doesn't carry out toggle.

This device has erase suspend/resume function, and you can read the device by suspending an erase operation of a certain sector. When you carry out erase suspend to select and to continuously read a sector under an erase suspend operation (any sector selected to be erase, in case of multiple sector batch erase), not DQ6 but DQ2 toggles. Therefore, it is possible to detect a sector under erase suspend by using DQ2.

During erase hold time, Toggle Bit 2 doesn't function.

When you set an erase operation to a sector protected or a boot sector protected and you read DQ2 by appointing those sectors, DO2 toggles. In this case, actual erase operation doesn't occur.

-f RY/BY# (ready / busy)

This device has a pin (RY/BY#) that detects the status of an internal automatic operation. Since the structure of this pin is open drain, it needs to be pull up to the V_{DD} pin and or the like to use.

RY/BY# outputs 0 at the rising edge of WE#(CE#) that inputs a final bus cycle of an automatic operation command cycle, and continues to output 0 when the device is under automatically operation. When the inner automatic operation is completed correctly, RY/BY# turns to a high impedance state. When the inner automatic operation is not completed correctly, RY/BY# outputs 0 continuously.

Table 9-a: Sector Address Table (Top Boot, BYTE# = H Word mode)

Sector	A18	A17	A16	A15	A14	A13	A12	Sector size (K Word)	Range of address
SA0	0	0	0	0	X	X	X	32	00000h ~ 07FFFh
SA1	0	0	0	1	X	X	X	32	08000h ~ 0FFFFh
SA2	0	0	1	0	X	X	X	32	10000h ~ 17FFFh
SA3	0	0	1	1	X	X	X	32	18000h ~ 1FFFFh
SA4	0	1	0	0	X	X	X	32	20000h ~ 27FFFh
SA5	0	1	0	1	X	X	X	32	28000h ~ 2FFFFh
SA6	0	1	1	0	X	X	X	32	30000h ~ 37FFFh
SA7	0	1	1	1	X	X	X	32	38000h ~ 3FFFFh
SA8	1	0	0	0	X	X	X	32	40000h ~ 47FFFh
SA9	1	0	0	1	X	X	X	32	48000h ~ 4FFFFh
SA10	1	0	1	0	X	X	X	32	50000h ~ 57FFFh
SA11	1	0	1	1	X	X	X	32	58000h ~ 5FFFFh
SA12	1	1	0	0	X	X	X	32	60000h ~ 67FFFh
SA13	1	1	0	1	X	X	X	32	68000h ~ 6FFFFh
SA14	1	1	1	0	X	X	X	32	70000h ~ 77FFFh
SA15	1	1	1	1	0	X	X	16	78000h ~ 7BFFFh
SA16	1	1	1	1	1	0	0	4	7C000h ~ 7CFFFh
SA17	1	1	1	1	1	0	1	4	7D000h ~ 7DFFFh
SA18	1	1	1	1	1	1	X	8	7E000h ~ 7FFFFh

The address ranges from A18 to A0. The least significant address is A0.

Table 9-b: Sector Address Table (Top Boot, BYTE# = L Byte mode)

Sector	A18	A17	A16	A15	A14	A13	A12	Sector size (K Byte)	Range of address
SA0	0	0	0	0	X	X	X	64	00000h ~ 0FFFFh
SA1	0	0	0	1	X	X	X	64	10000h ~ 1FFFFh
SA2	0	0	1	0	X	X	X	64	20000h ~ 2FFFFh
SA3	0	0	1	1	X	X	X	64	30000h ~ 3FFFFh
SA4	0	1	0	0	X	X	X	64	40000h ~ 4FFFFh
SA5	0	1	0	1	X	X	X	64	50000h ~ 5FFFFh
SA6	0	1	1	0	X	X	X	64	60000h ~ 6FFFFh
SA7	0	1	1	1	X	X	X	64	70000h ~ 7FFFFh
SA8	1	0	0	0	X	X	X	64	80000h ~ 8FFFFh
SA9	1	0	0	1	X	X	X	64	90000h ~ 9FFFFh
SA10	1	0	1	0	X	X	X	64	A0000h ~ AFFFFh
SA11	1	0	1	1	X	X	X	64	B0000h ~ BFFFFh
SA12	1	1	0	0	X	X	X	64	C0000h ~ CFFFFh
SA13	1	1	0	1	X	X	X	64	D0000h ~ DFFFFh
SA14	1	1	1	0	X	X	X	64	E0000h ~ EFFFFh
SA15	1	1	1	1	0	X	X	32	F0000h ~ F7FFFh
SA16	1	1	1	1	1	0	0	8	F8000h ~ F9FFFh
SA17	1	1	1	1	1	0	1	8	FA000h ~ FBFFFh
SA18	1	1	1	1	1	1	X	16	FC000h ~ FFFFFh

The address ranges from A18 to A0. The least significant address is A-1.

Table 9-c: Sector Address Table (Bottom Boot, BYTE# = H Word mode)

Sector	A18	A17	A16	A15	A14	A13	A12	Sector size (K Word)	Range of address
SA0	0	0	0	0	0	0	X	8	00000h ~ 01FFFh
SA1	0	0	0	0	0	1	0	4	02000h ~ 02FFFh
SA2	0	0	0	0	0	1	1	4	03000h ~ 03FFFh
SA3	0	0	0	0	1	X	X	16	04000h ~ 07FFFh
SA4	0	0	0	1	X	X	X	32	08000h ~ 0FFFFh
SA5	0	0	1	0	X	X	X	32	10000h ~ 17FFFh
SA6	0	0	1	1	X	X	X	32	18000h ~ 1FFFFh
SA7	0	1	0	0	X	X	X	32	20000h ~ 27FFFh
SA8	0	1	0	1	X	X	X	32	28000h ~ 2FFFFh
SA9	0	1	1	0	X	X	X	32	30000h ~ 37FFFh
SA10	0	1	1	1	X	X	X	32	38000h ~ 3FFFFh
SA11	1	0	0	0	X	X	X	32	40000h ~ 47FFFh
SA12	1	0	0	1	X	X	X	32	48000h ~ 4FFFFh
SA13	1	0	1	0	X	X	X	32	50000h ~ 57FFFh
SA14	1	0	1	1	X	X	X	32	58000h ~ 5FFFFh
SA15	1	1	0	0	X	X	X	32	60000h ~ 67FFFh
SA16	1	1	0	1	X	X	X	32	68000h ~ 6FFFFh
SA17	1	1	1	0	X	X	X	32	70000h ~ 77FFFh
SA18	1	1	1	1	X	X	X	32	78000h ~ 7FFFFh

The address ranges from A18 to A0. The least significant address is A0.

Table 9-d: Sector Address Table (Bottom Boot, BYTE# = L Byte mode)

Sector	A18	A17	A16	A15	A14	A13	A12	Sector size (K Byte)	Range of address
SA0	0	0	0	0	0	0	X	16	00000h ~ 03FFFh
SA1	0	0	0	0	0	1	0	8	04000h ~ 05FFFh
SA2	0	0	0	0	0	1	1	8	06000h ~ 07FFFh
SA3	0	0	0	0	1	X	X	32	08000h ~ 0FFFFh
SA4	0	0	0	1	X	X	X	64	10000h ~ 1FFFFh
SA5	0	0	1	0	X	X	X	64	20000h ~ 2FFFFh
SA6	0	0	1	1	X	X	X	64	30000h ~ 3FFFFh
SA7	0	1	0	0	X	X	X	64	40000h ~ 4FFFFh
SA8	0	1	0	1	X	X	X	64	50000h ~ 5FFFFh
SA9	0	1	1	0	X	X	X	64	60000h ~ 6FFFFh
SA10	0	1	1	1	X	X	X	64	70000h ~ 7FFFFh
SA11	1	0	0	0	X	X	X	64	80000h ~ 8FFFFh
SA12	1	0	0	1	X	X	X	64	90000h ~ 9FFFFh
SA13	1	0	1	0	X	X	X	64	A0000h ~ AFFFFh
SA14	1	0	1	1	X	X	X	64	B0000h ~ BFFFFh
SA15	1	1	0	0	X	X	X	64	C0000h ~ CFFFFh
SA16	1	1	0	1	X	X	X	64	D0000h ~ DFFFFh
SA17	1	1	1	0	X	X	X	64	E0000h ~ EFFFFh
SA18	1	1	1	1	X	X	X	64	F0000h ~ FFFFFh

The address ranges from A18 to A0. The least significant address is A-1.

Absolute Maximum Rating

Storage temperature..-65 °C ~ 150 °C
D.C. input/output voltage ....-0.5 V ~ V_{DD}+0.5V
Over shoot voltage below 20ns ....-1.0 V ~ V_{DD}+1.0V

Operation conditions recommended

Operation temperature... 0 °C ~ +70 °C
V_{DD}...2.7 V ~ 3.6 V

DC Electric Characteristics

Symbol	Parameter	Limit			Units	Test Condition
		Min.	Typ.	Max.		
I_{DDR}	Operation current at reading		15	25	mA	CE# = OE# = VIL, WE# = VIH All the DQs are open. Address input = VIH / VIL, VDD = VDD max. Operation frequency = 10MHz, OE# = VIL
I_{DDW}	Operation current at writing			35	mA	CE# = WE# = V_{IL}, OE# = V_{IH}, V_{DD} = V_{DD} max.
I_{SB}	CMOS standby current			10	µA	CE# = V_{DD}–0.3V, V_{DD} = V_{DD} max.
I_{LI} I_{LO}	Input leak current Output leak current			10 10	µA µA	V_{IN} = V_{SS} ~ V_{DD}, V_{DD} = V_{DD} max. V_{OUT} = Vss ~ V_{DD}, V_{DD} =V $_{DD}$ max.
V_{ID}	Input high voltage	11.5	12.0	12.5	V	A9, OE#, RESET#
V_{IL} V_{ILC} V_{IH} V_{IHC}	Input L-level voltage Input L-level voltage (CMOS) Input H-level voltage Input H-level voltage (CMOS)	 V_{DD}*0.8 V_{DD}-0.2		V_{DD}*0.2 0.2 	V V V V	
V_{OL} V_{OH}	Output L-level voltage Output H-level voltage	 V_{DD}-0.2		0.2 	V V	I_{OL} = 100µA, V_{DD} = V_{DD} min. I_{OH} = -100µA, V_{DD} = V_{DD} min.

Power-up Timing

Symbol	Parameter	Maximum	Units
tPU_READ	Time period from power supply to a read operation	200	µs
tPU_WRITE	Time period from power supply to a write operation	200	µs

Capacitance (Ta = 25°C, f = 1MHz)

Symbol	Descriptions	Maximum	Units	Test Condition
C_{DQ}	Input pin capacitance	12	pF	V_{DQ} = 0V
C_{IN}	Input pin capacitance	6	pF	V_{IN} = 0V

AC Electric Characteristics

Read cycle

Symbol	Parameter	Limits		Units
		Min.	Max.	
tRC	Read cycle time	70		ns
tCE	CE# access time		70	ns
tAA	Address access time		70	ns
tOE	OE# access time		30	ns
tCLZ	From CE# L to output low impedance	0		ns
tOLZ	From OE# L to output low impedance	0		ns
tCHZ	From CE# H to output high impedance		25	ns
tOHZ	From OE# H to output high impedance		25	ns
tOH	Retaining time of output from address change	0		ns
tRP	RESET# pulse width	500		ns
tRY	RESET# recovery time		20	µs
tRB	From READY# to WE#	0		ns

Erase / Program cycle

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
tSSE	Small sector erase time		0.025	3	s
tSCE	Sector erase time		0.025	3	s
tCPE	Chip erase time		0.5	60	s
tBP	Programming time		20	100	µs
tAS	Address setup time	0			ns
tAH	Address hold time	45			ns
tCES	CE# setup time	0			ns
tCEH	CE# hold time	0			ns
tOES	OE# setup time to write pulse	0			ns
tOEH	OE# hold time to write pulse	0			ns
tCP	CE# write pulse width	35			ns
tWP	WE# write pulse width	35			ns
tCPH	CE# standby pulse width	25			ns
tWPH	WE# standby pulse width	25			ns
tDS	Data setup time	35			ns
tDH	Data hold time	0			ns
tSEDH	Sector erase hold time	50			µs
tSUSE	Erase suspend time	10			µs
tBUSY	RY/BY# delay time			90	ns
tVDDR	VDD rise time	0.1		50	ms
tIDA	Read standby time	150			ns

Note: Since this parameter is measured only for initial qualification, it might be affected by design or process changes.

AC Test Conditions

Input voltage.. 0 V ~ 3.0 V
Input rise / fall time .... 5 ns
Input / output timing level .... 1.5 V
Output load... 1TTL Gate and CL = 30pF

Figure 3: Read Timing Chart

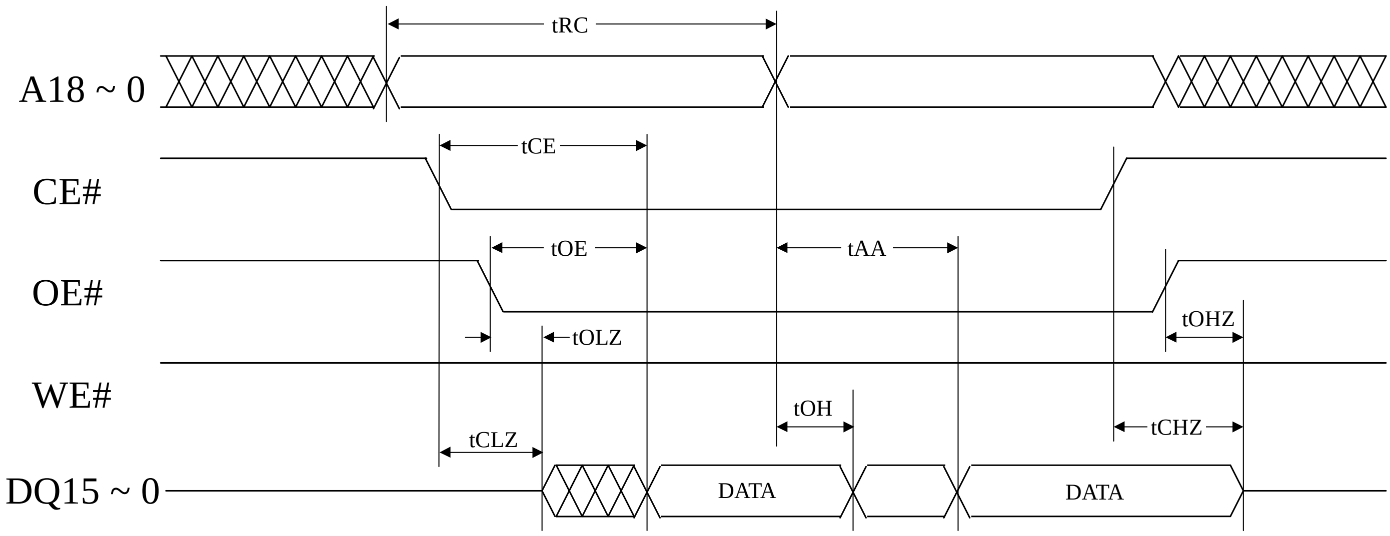


Figure 4: Timing Chart of WE# Control Write Cycle

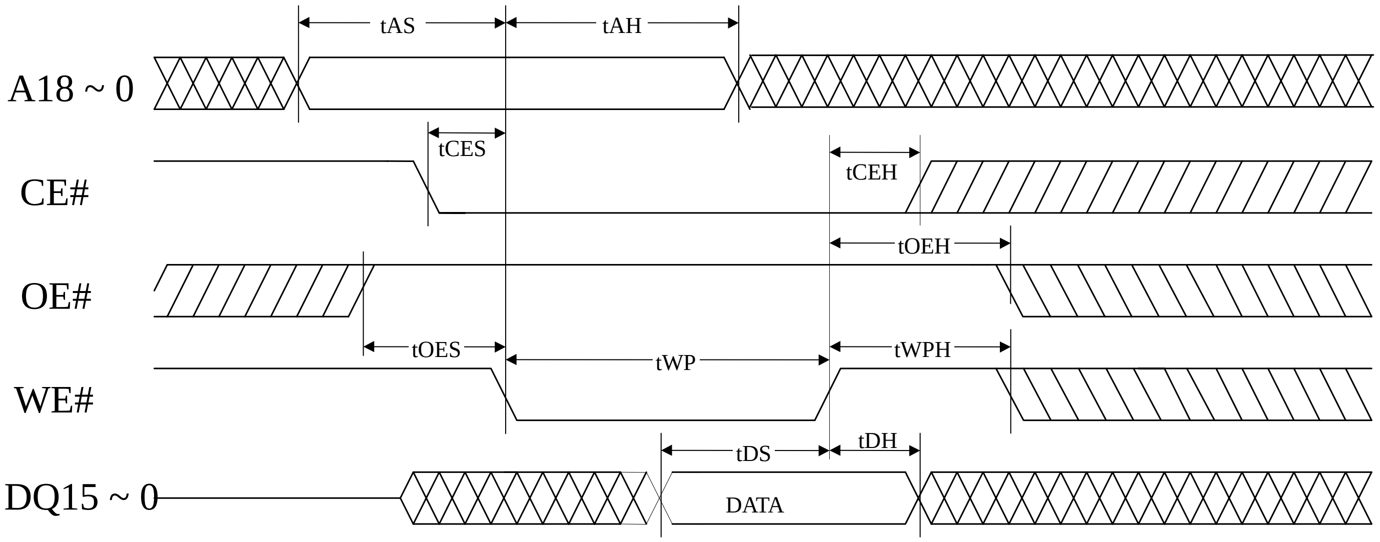


Figure 5: Timing Chart of CE# Control Write Cycle

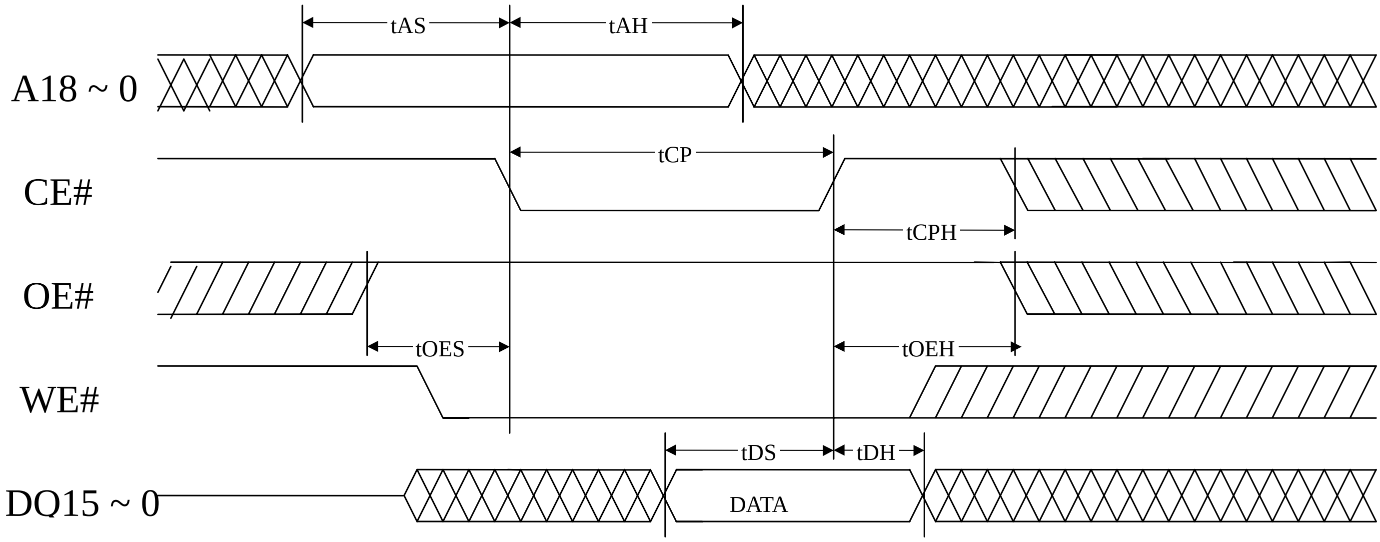


Figure 6: Word (Byte) Program Timing Chart

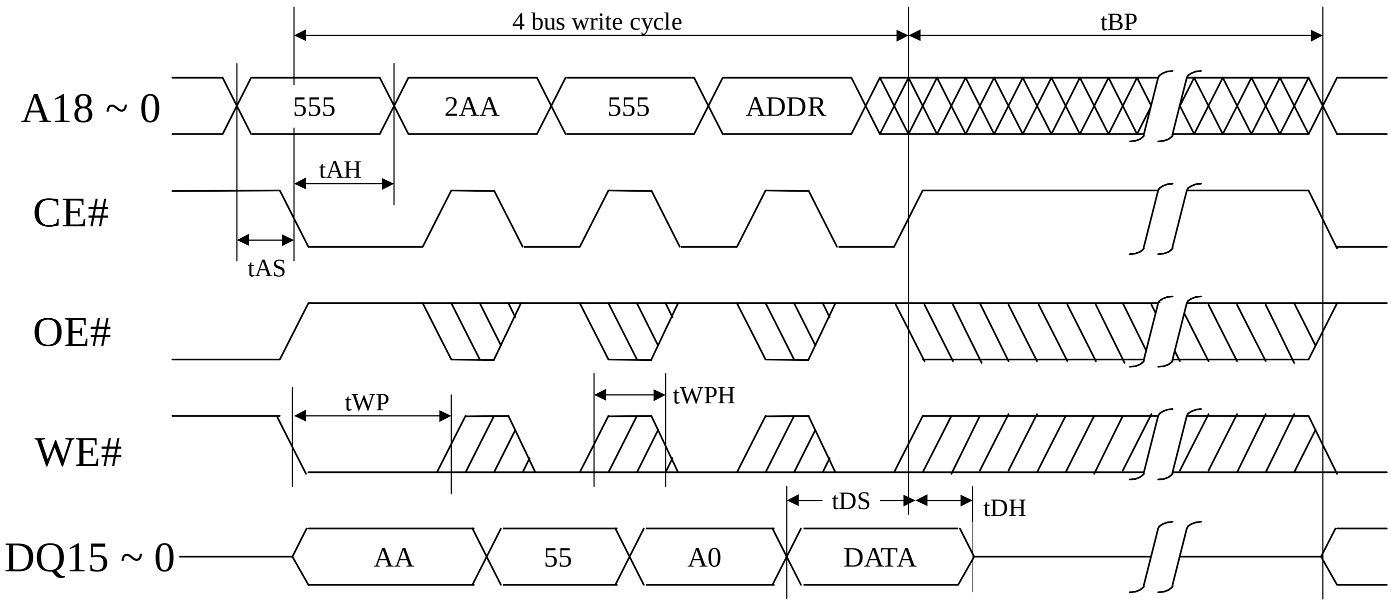


Figure 7: Chip Erase Timing Chart

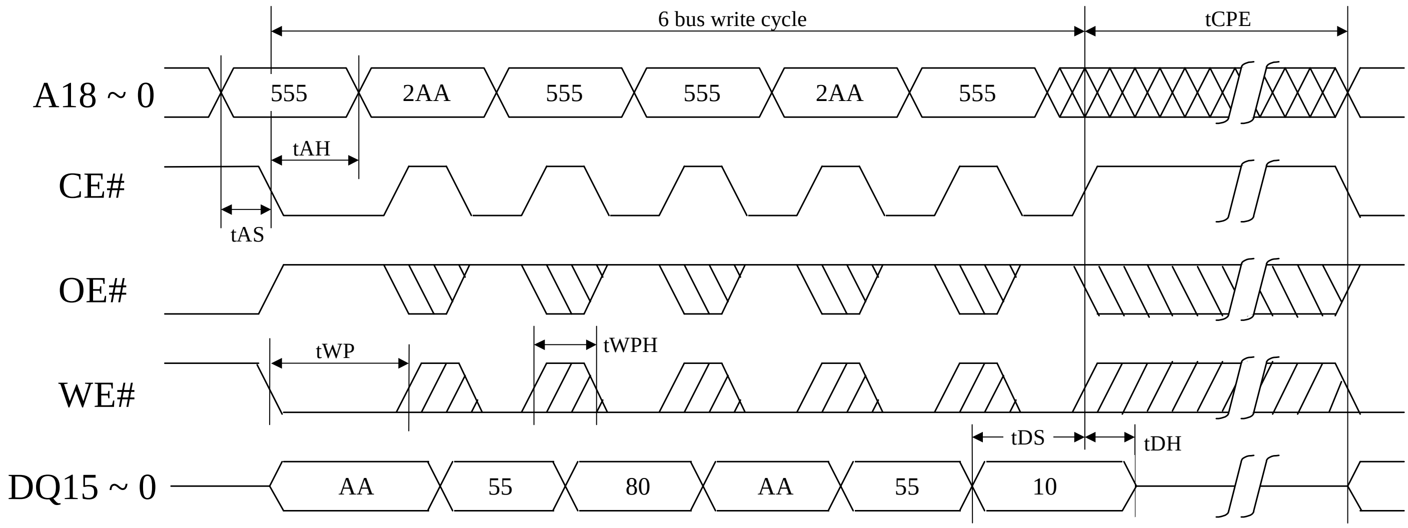


Figure 8-a: Sector Erase Timing Chart

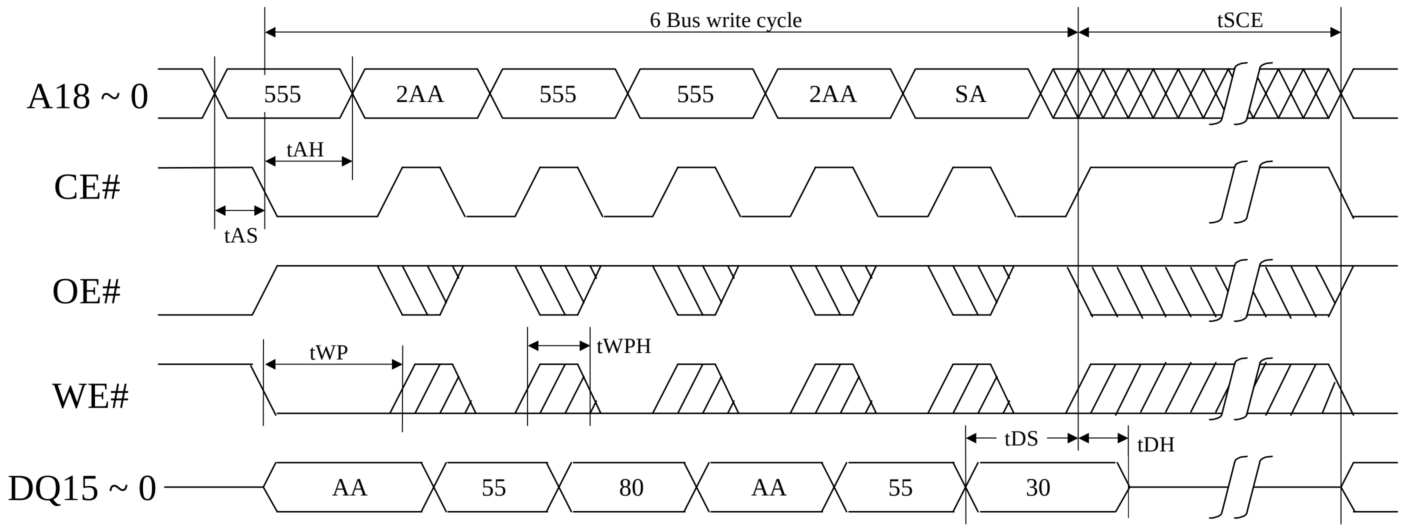


Figure 8-b: Multi Sector Erase Timing Chart

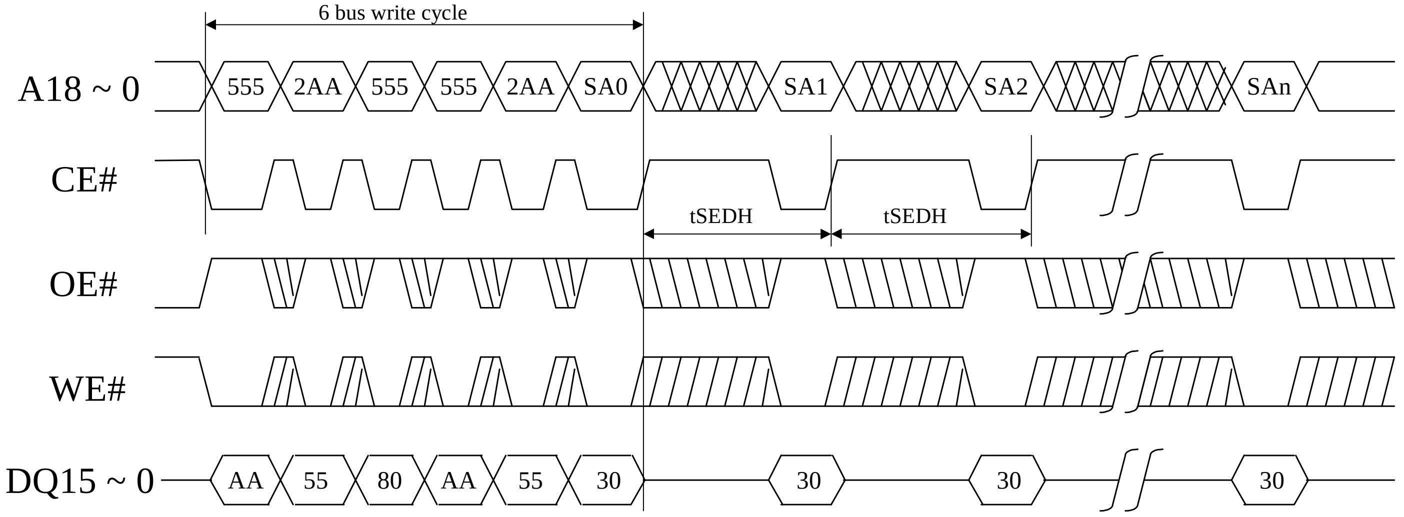


Figure 9: Small Sector Erase Timing Chart

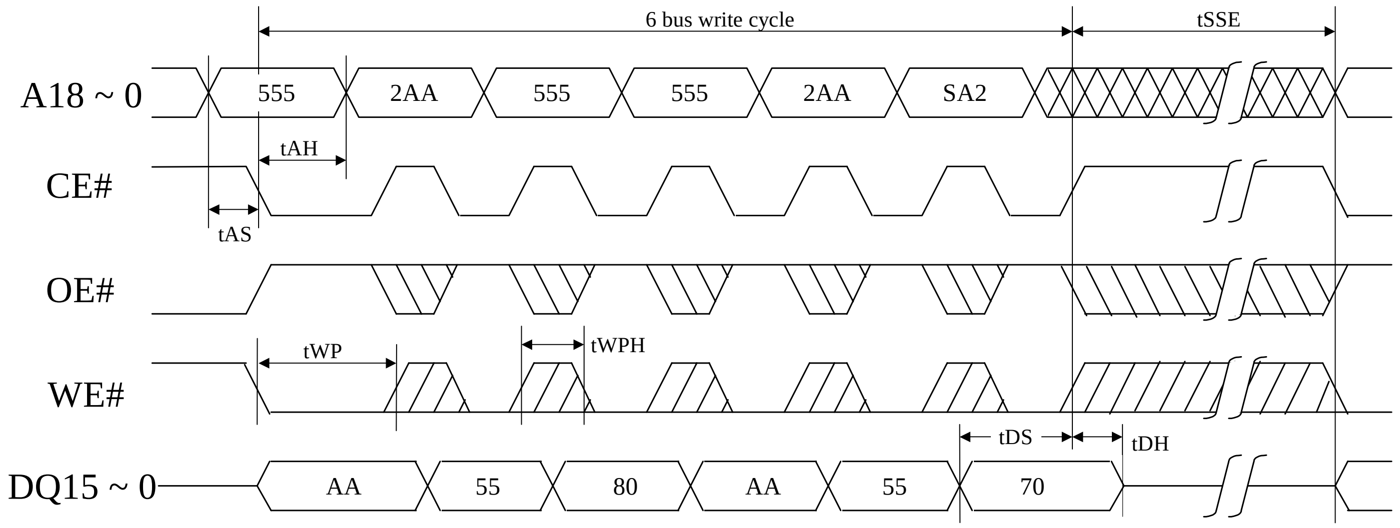


Figure 10: Erase Suspend Timing

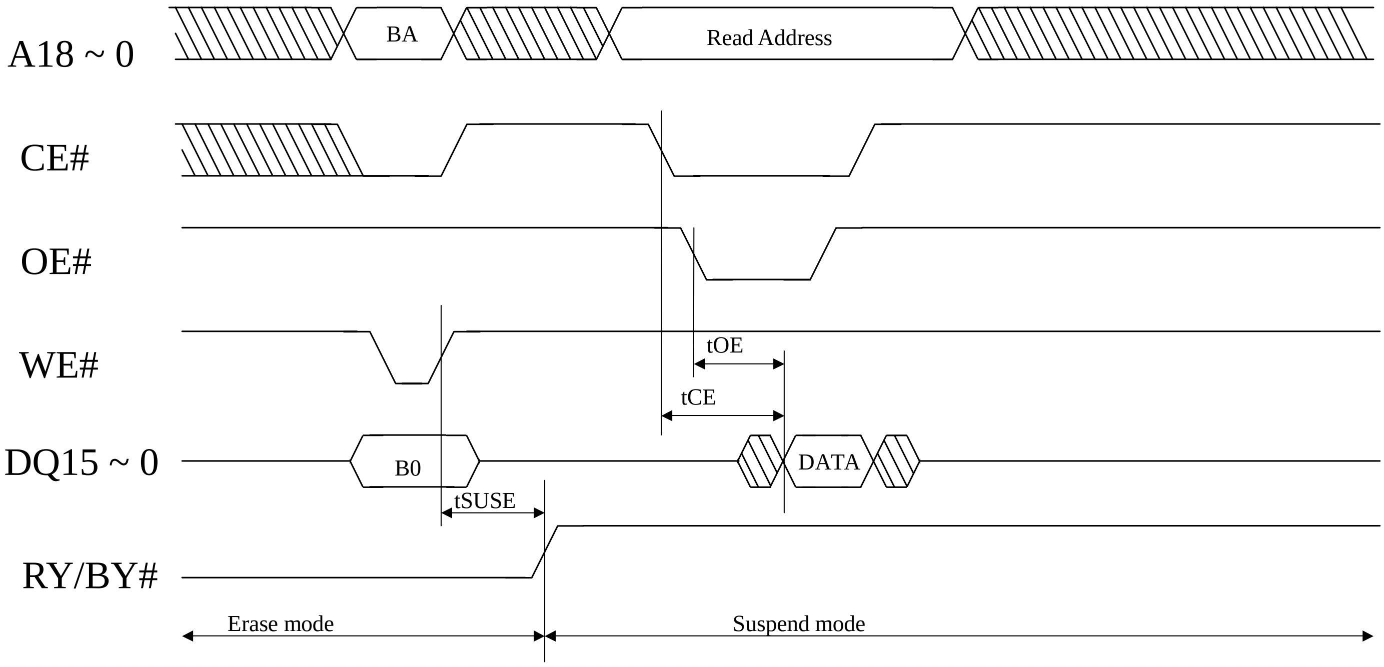


Figure 11: Erase Resume Timing Chart

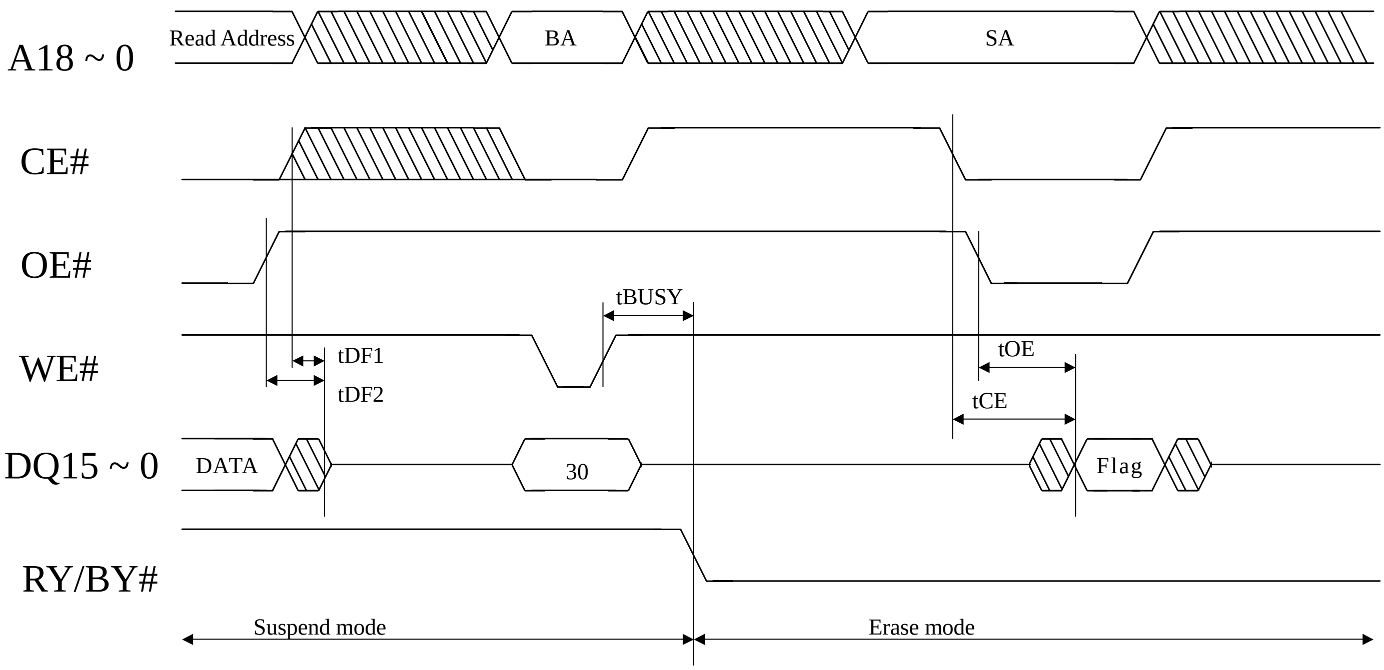


Figure 12: Hardware ID Read Timing Chart

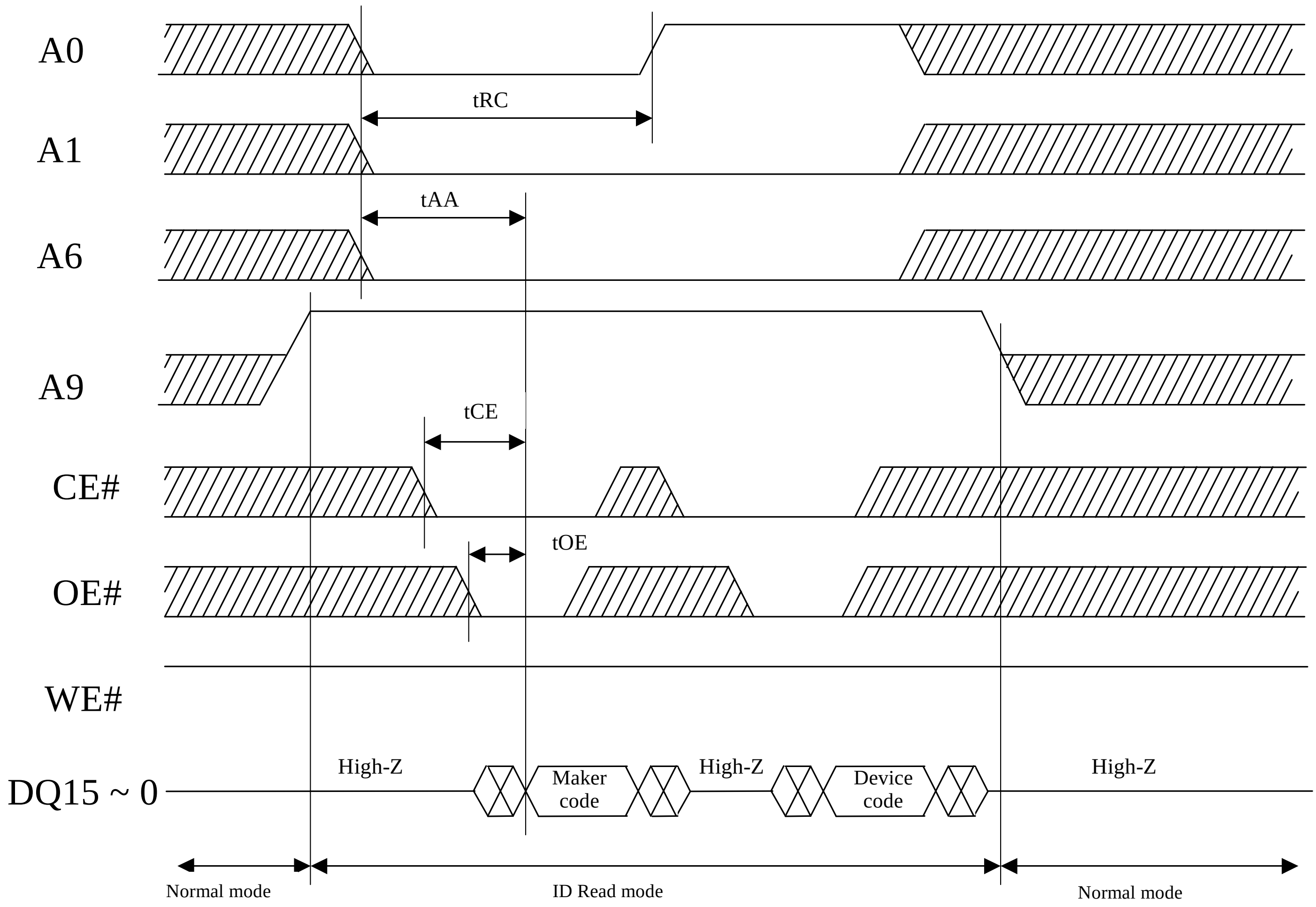


Figure 13-a: Software ID Read Timing Chart

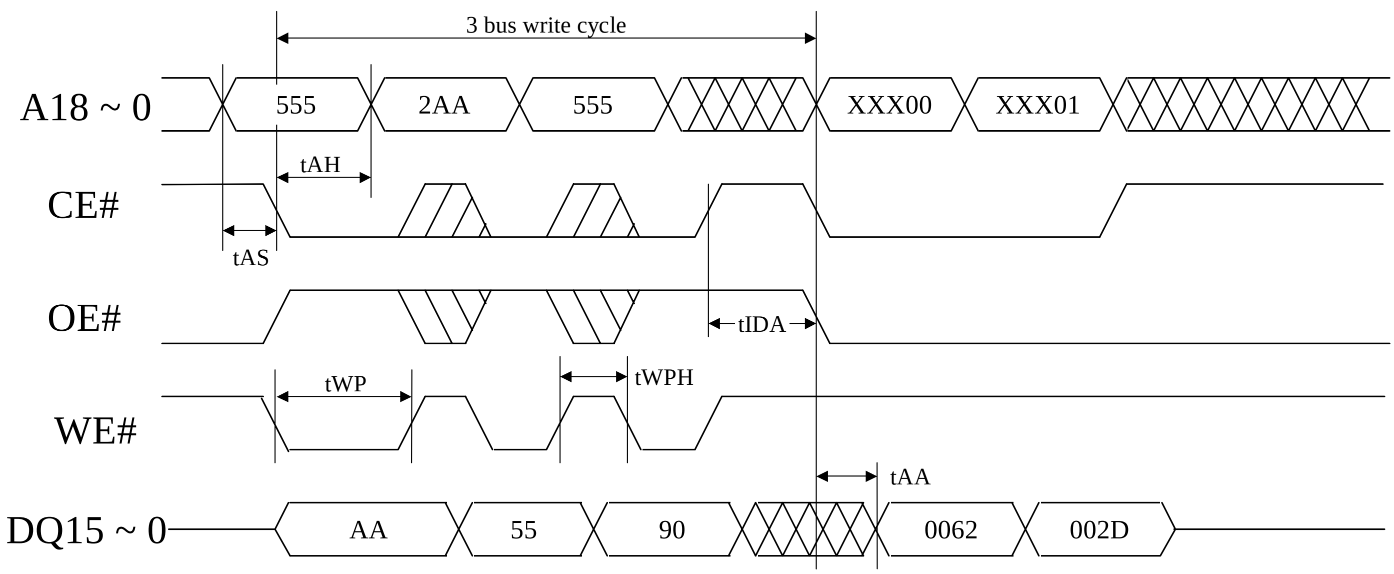


Figure 13-b: CFI Mode Entry Timing Chart

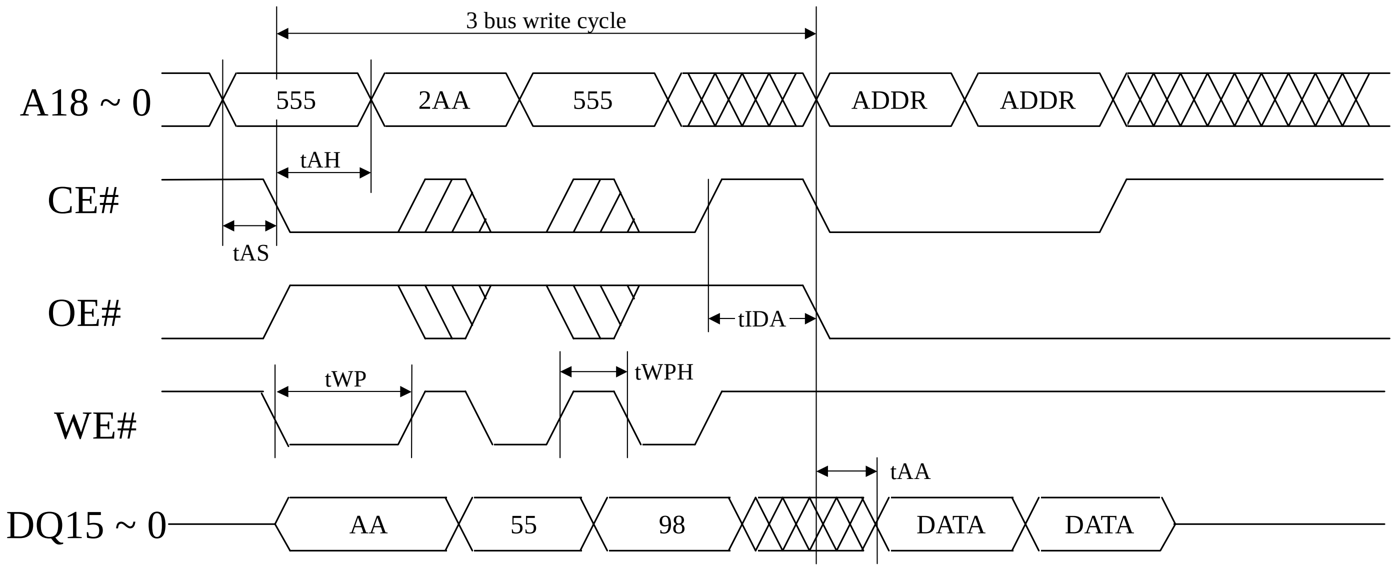


Figure 14-a: Read Reset (Read Reset A) Timing Chart

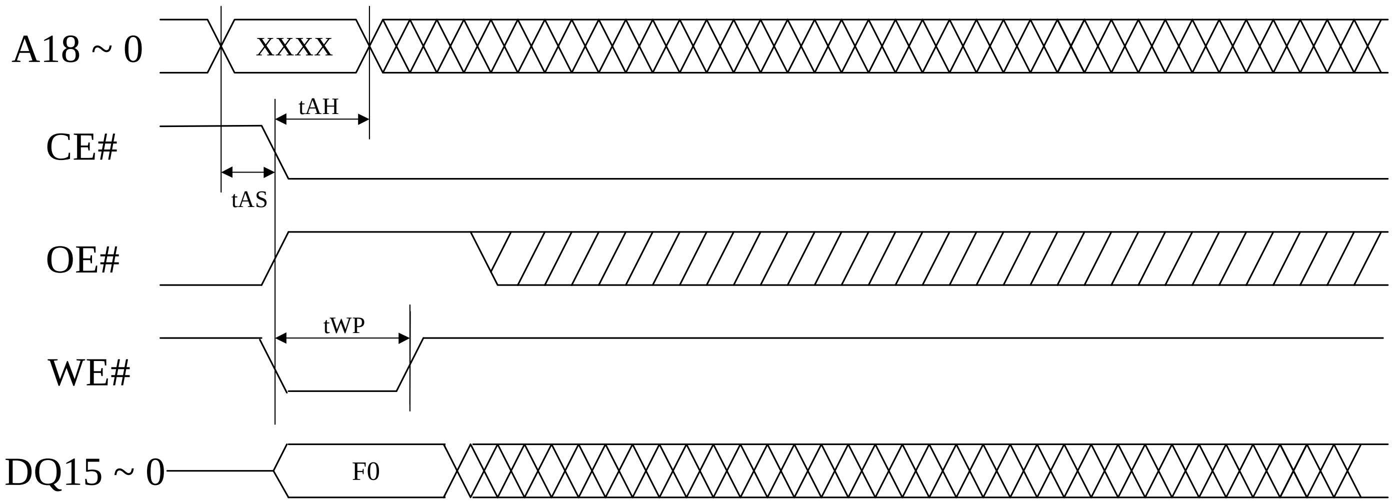


Figure 14-b: Read Reset (Read Reset B) Timing Chart

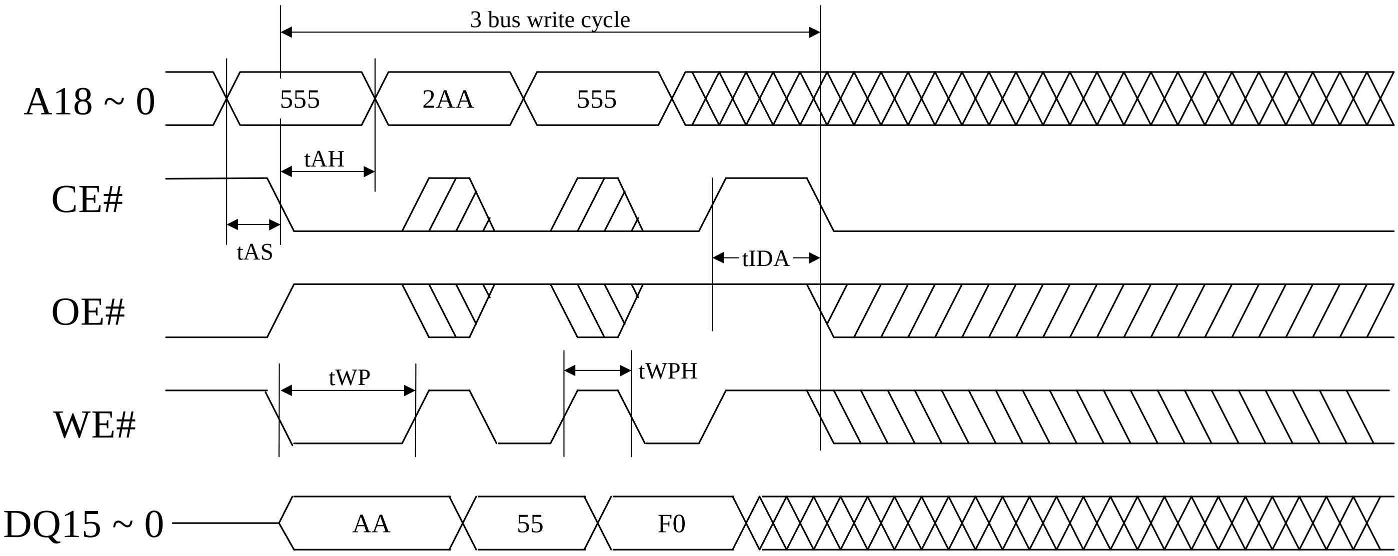


Figure 15: DATA# Polling Timing Chart (DQ7)

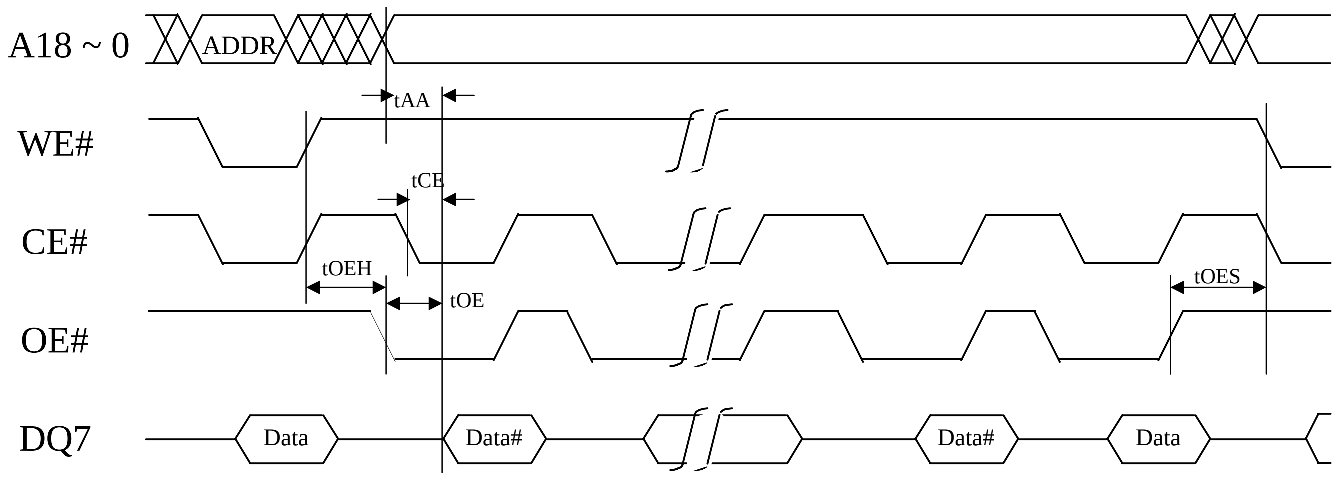
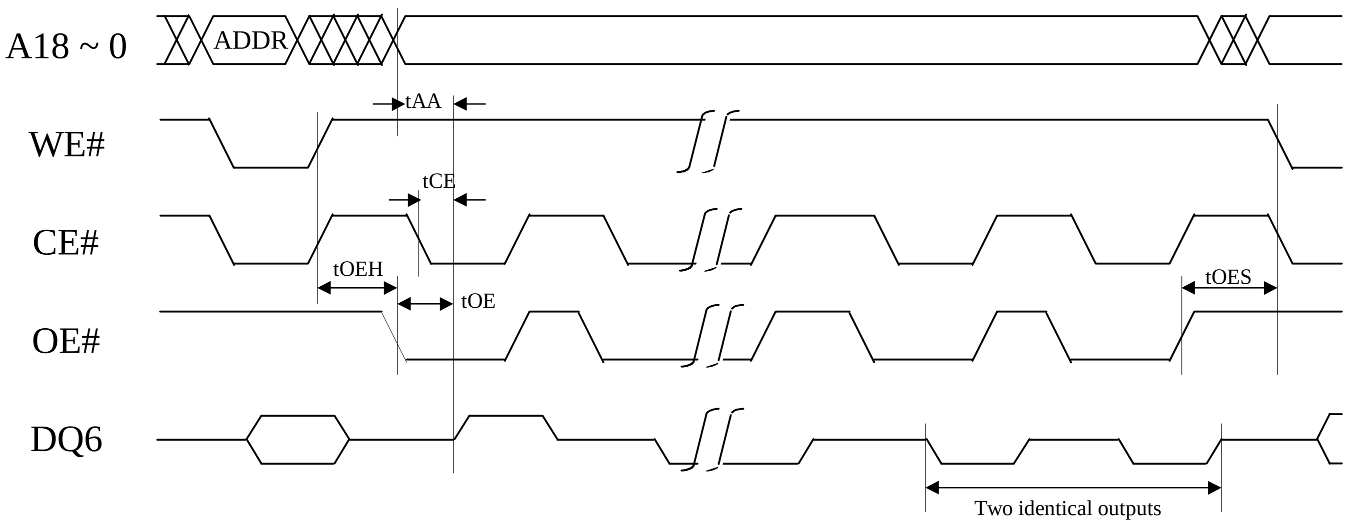


Figure 16: Toggle Bit Timing Chart (DQ6)



Note: Toggle bit output starts 1 “H” all the time.

Figure 17: Hardware Reset Timing Chart

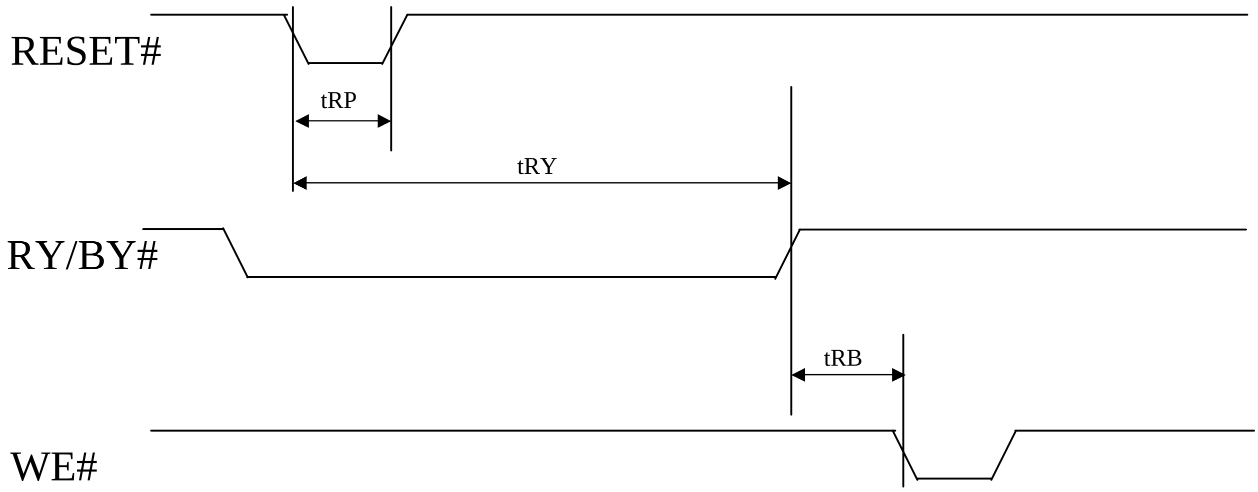
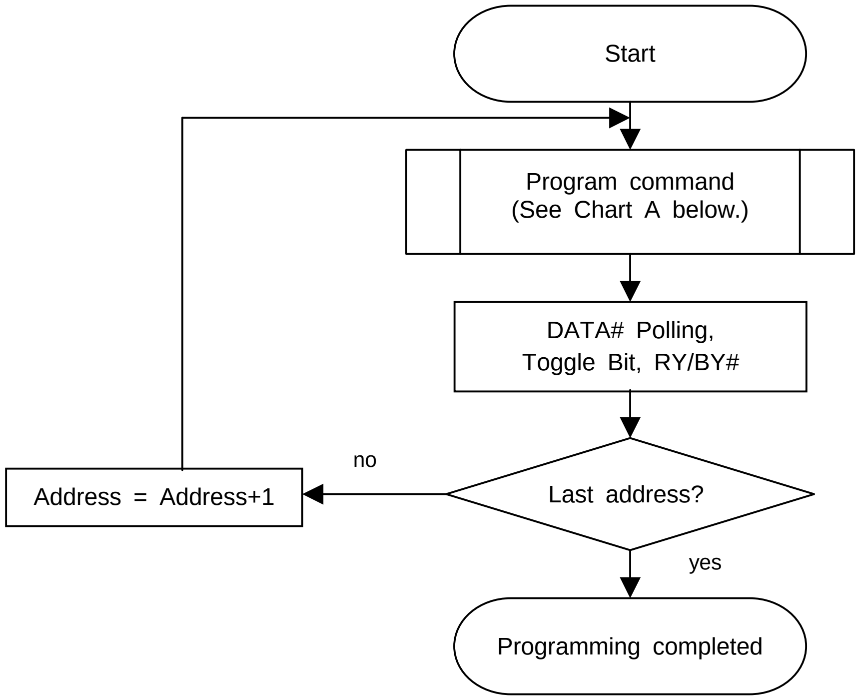


Figure 18: Word (Byte) Program Algorithm



A: Program Command Sequence (Address / Command)

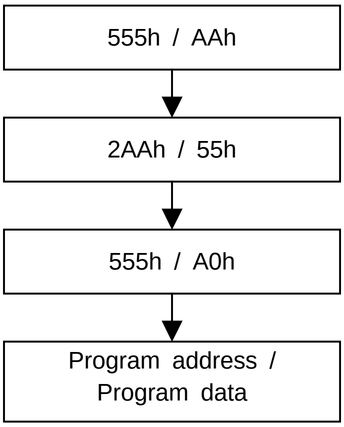
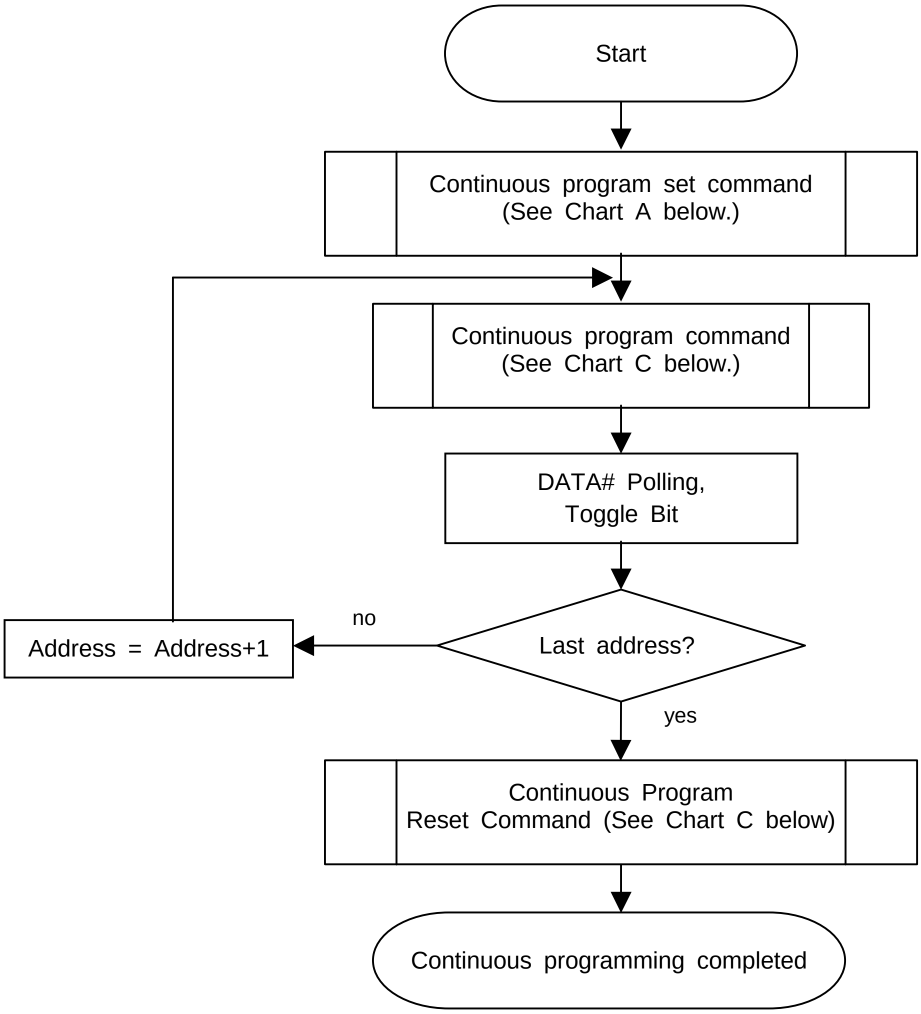
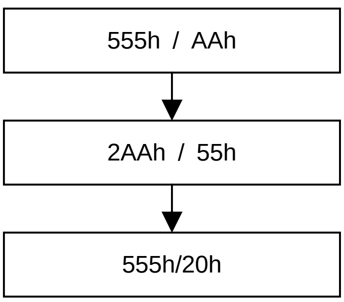


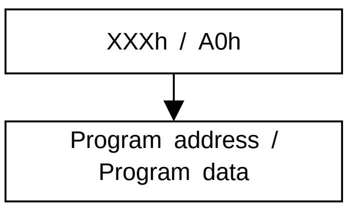
Figure 19: Fast Word (Byte) Program Algorithm



A Continuous program set command



B Continuous program command



C Continuous program reset command

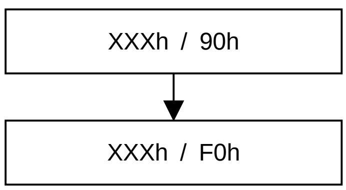
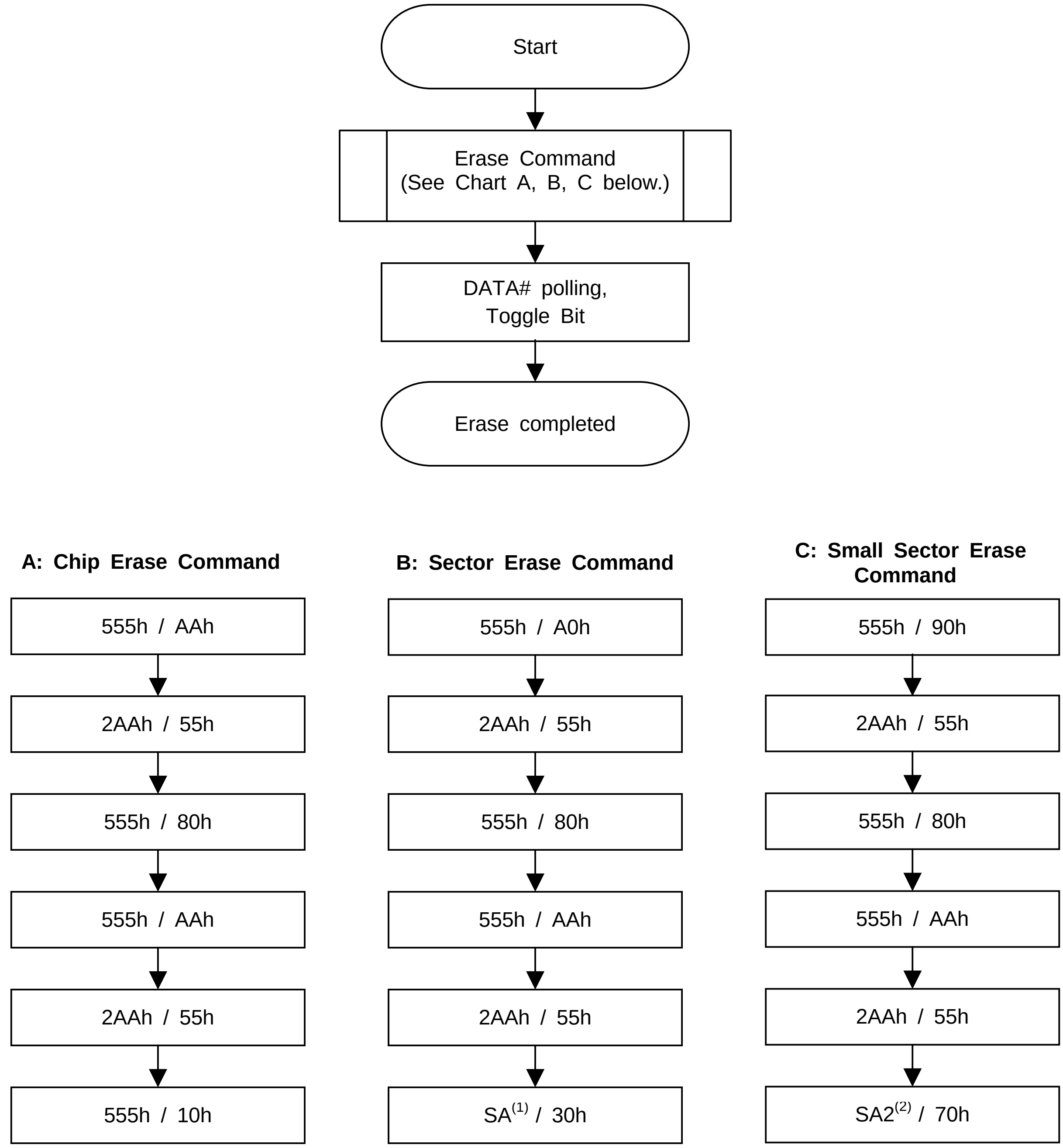
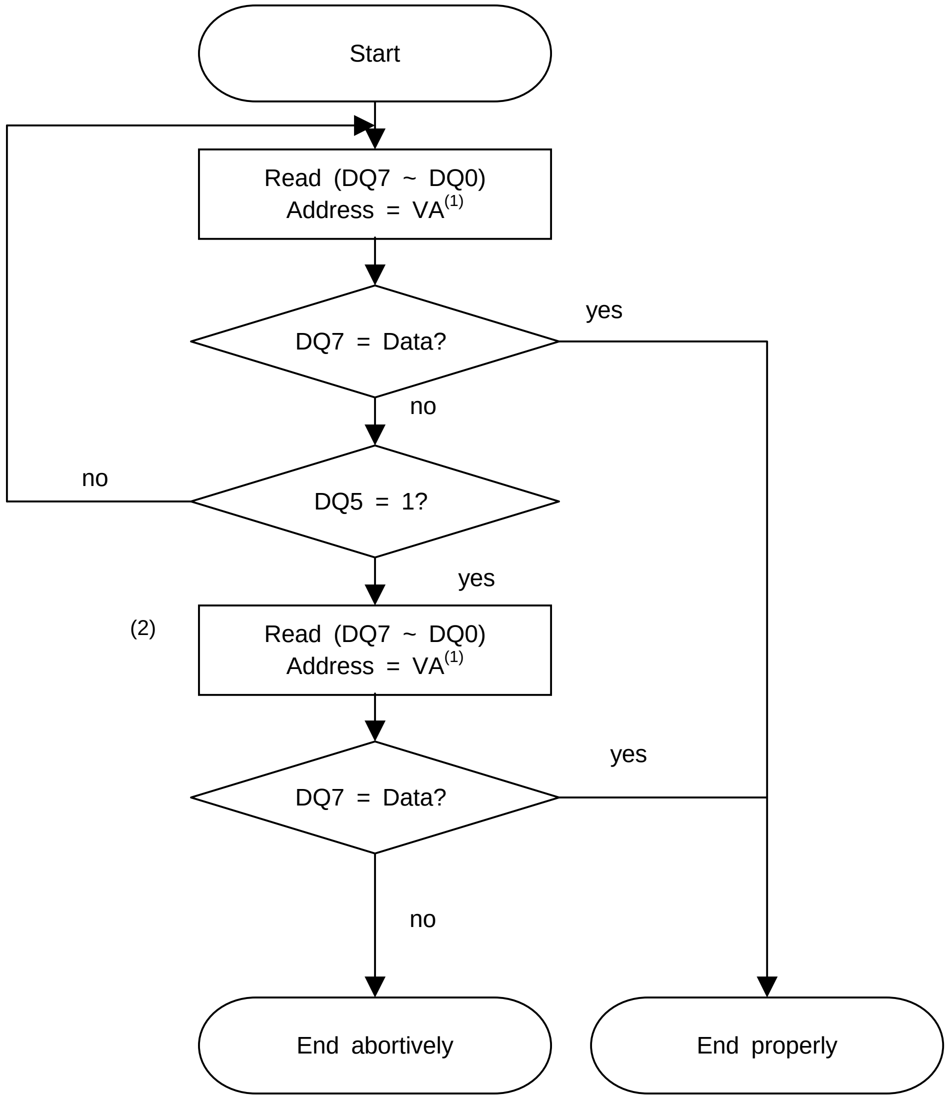


Figure 20: Erase Algorithm



(1) SA: Sector Address = A18 ~ A12
(2) SA2: Small Sector Address = A18 ~ A11

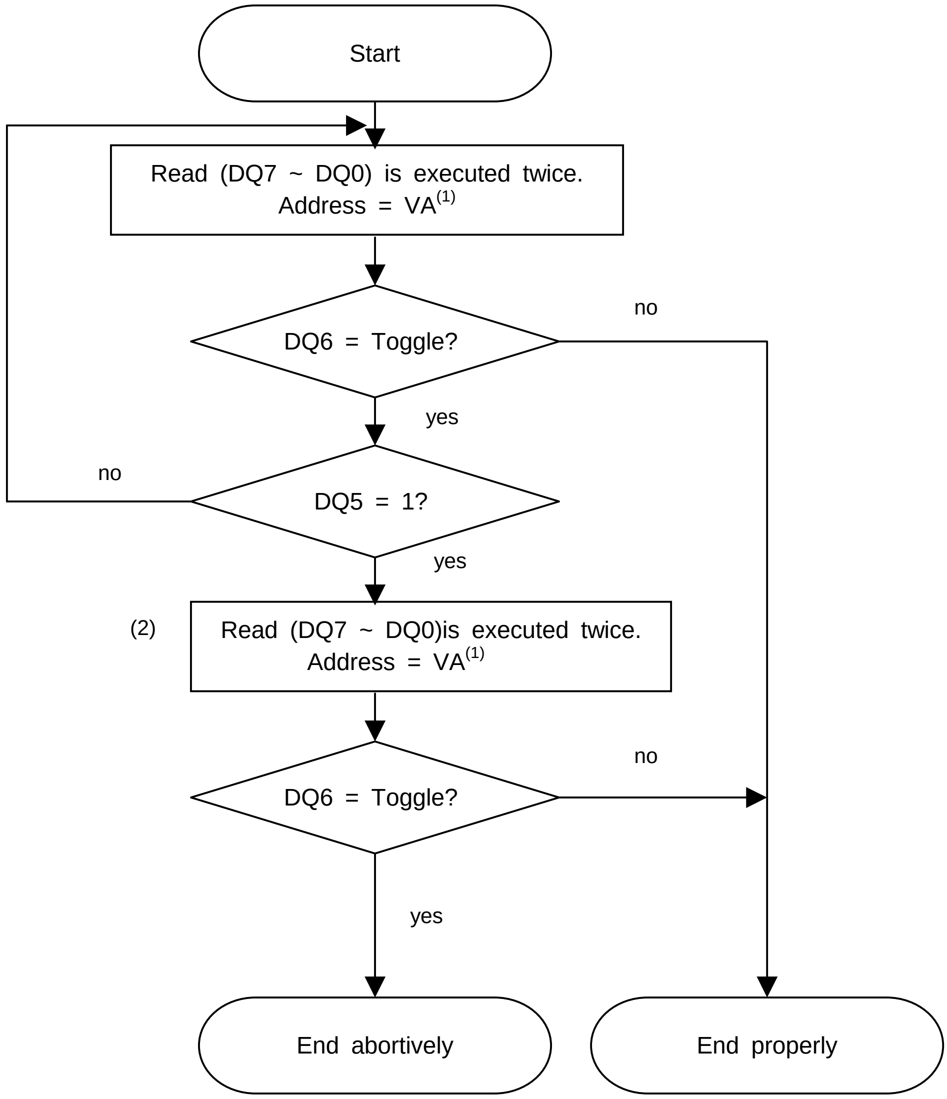
Figure 21: DATA# Polling Algorithm



(1) VA:
Programming time: the address that executes programming
Chip Erase time: a discretionary address
Sector Erase time: a sector address that executes erasing
Small Sector Erase time: a small sector address that executes erasing

(2) The reason why DQ5 outputs 1 might be either the timing limit is exceeded or the erased data is read. When DQ5 outputs 1, check DQ7 again to see if it's completed abortively.

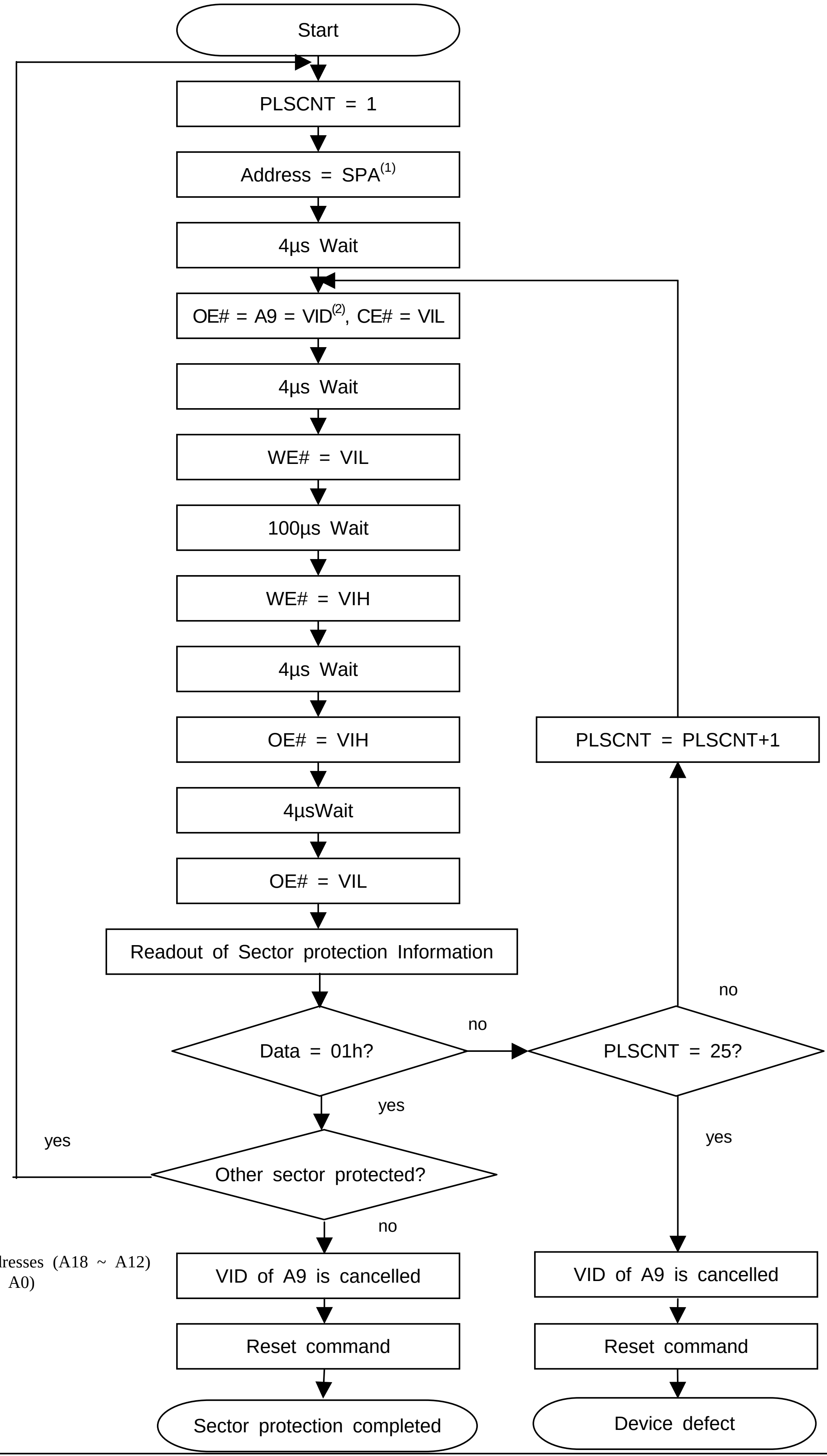
Figure 22: Toggle Bit Algorithm



(1) VA:
Programming time: the address that executes programming
Chip Erase time: a discretionary address
Sector Erase time: a sector address that executes erasing
Small Sector Erase time: a small sector address that executes erasing

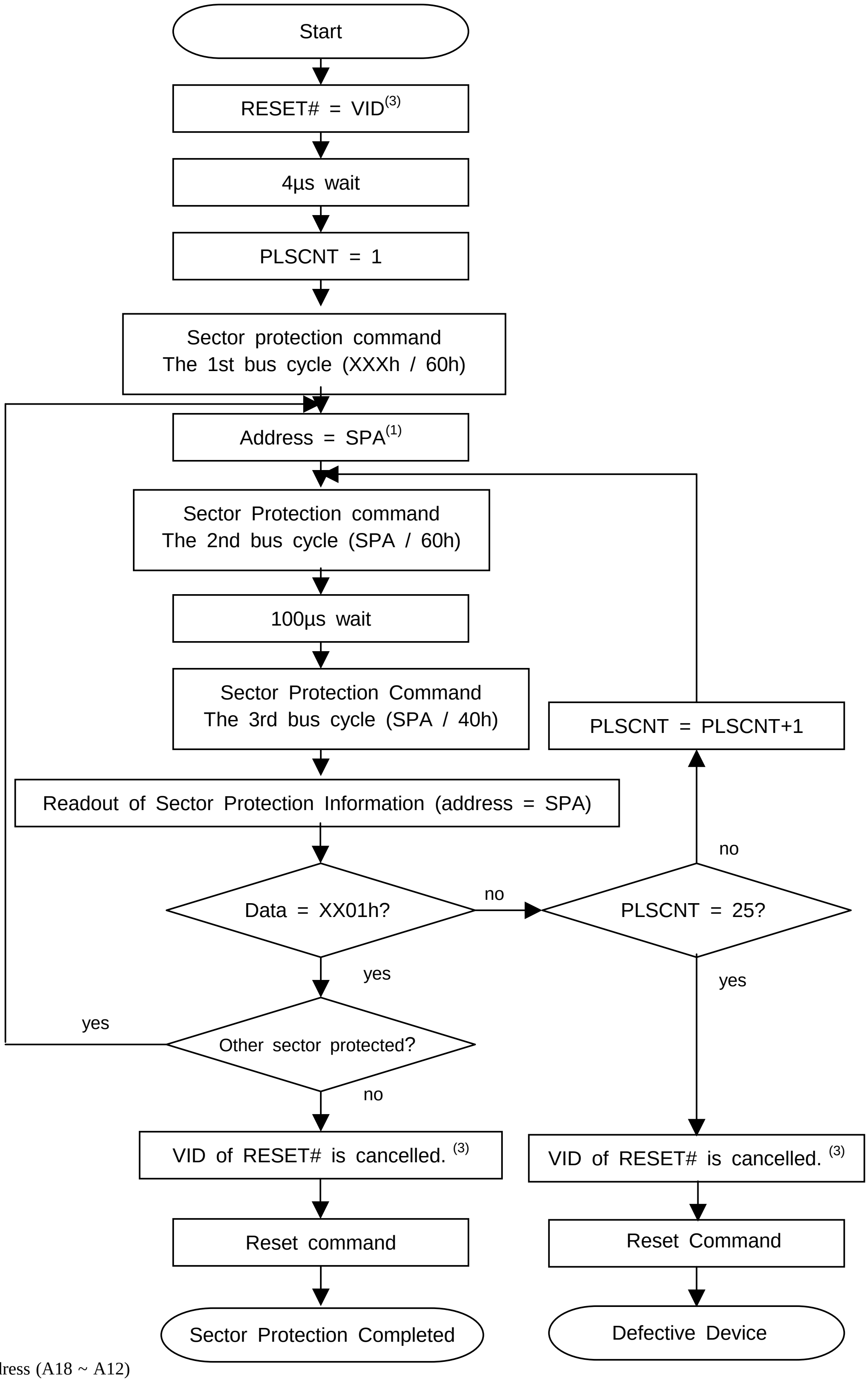
(2) The reason why DQ5 outputs 1 might be either the timing limit is exceeded or the erased data is read. When DQ5 outputs 1, check DQ6 again to see if it's completed abortively.

Figure 23: Sector Protection 1 Algorithm



(1) SPA: Protection Sector addresses (A18 ~ A12) and, Read address (A6, A1, A0)
(2) VID: High Voltage

Figure 24: Sector Protection 2 Algorithm



(1) SPA: Protection sector address (A18 ~ A12) and Read address (A6, A1, A0)
(2) VID: High Voltage
(3) Not necessary when a sector in the Security Sector range is protected.

Table 10-a: CFI Cuery Identification String

Address		Data	Description
Byte Mode	Word Mode		
20h 22h 24h	10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
26h 28h	13h 14h	0002h 0000h	Primary vendor command set and control interface ID code
2Ah 2Ch	15h 16h	0040h 0000h	Address for Primary Extended Table
2Eh 30h	17h 18h	0000h 0000h	Alternate OEM command set (00h = none exists)
32h 34h	19h 1Ah	0000h 0000h	Address for secondary algorithm extended query table (00h = none exists)

Table 10-b: System Interface Information

Address		Data	Description
Byte Mode	Word Mode		
36h	1Bh	0027h	VDD Min (2.7V)
38h	1Ch	0036h	VDD Min (3.6V)
3Ah	1Dh	0000h	VPP Min (0000h = no VPP Pin)
3Ch	1Eh	0000h	VPP Max (0000h = no VPP Pin)
3Eh	1Fh	0005h	Typical timeout for Word-Program 2^N µs (2^5 = 32µs)
40h	20h	0000h	Typical timeout for min. size buffer Program 2^N µs (00h = not supported)
42h	21h	0005h	Typical timeout for individual Sector/Block-Erase 2^N ms (2^5 = 32ms)
44h	22h	000Ah	Typical timeout for Chip-Erase 2^N ms (2^9 = 512ms)
46h	23h	0002h	Maximum timeout for Word-Program 2^N times typical ($2^2 \times 2^5$ = 128µs)
48h	24h	0000h	Maximum timeout for buffer Program 2^N times typical (00h = not supported)
4Ah	25h	0007h	Maximum timeout for individual Sector/Block-Erase 2^N times typical ($2^7 \times 2^5$ = 4048ms)
4Ch	26h	0007h	Maximum timeout for Chip-Erase 2^N times typical ($2^7 \times 2^9$ = 64sec)

Table 10-c: Device Geometry Information

Address		Data	Description
Byte Mode	Word Mode		
4Eh	27h	0014h	Device size = 2^N Bytes (14h = 20; 2^{20} = 1MByte)
50h 52h	28h 29h	0002h 0000h	Flash Device Interface description; 0002h = ×8/×16 asynchronous interface.
54h 56h	2Ah 2Bh	0000h 0000h	Maximum number of byte in multi-byte write = 2^N (00h = not supported)
58h	2Ch	0004h	Number of Erase Sector/Block sizes supported by device
5Ah 5Ch	2Dh 2Eh	0000h 0000h	Region 1 Information (y + 1 = Number of sectors) 0000h+1 = 1
5Eh 60h	2Fh 30h	0040h 0000h	Region 1 Information (z × 256 Byte = sector size) 64 × 256 Byte = 16K Byte (40h = 64)
62h 64h	31h 32h	0001h 0000h	Region 2 Information (y + 1 = Number of sectors) 0001h+1 = 2
66h 68h	33h 34h	0020h 0000h	Region 2 Information (z × 256 Byte = sector size) 32 × 256 Byte = 8K Byte (20h = 32)
6Ah 6Ch	35h 36h	0000h 0000h	Region 3 Information (y + 1 = Number of sectors) 0000h+1 = 1
6Eh 70h	37h 38h	0080h 0000h	Region 3 Information (z× 256 Byte = sector size) 128 × 256 Byte = 32K Byte (80h = 128)
72h 74h	39h 3Ah	000Eh 0000h	Region 4 Information (y + 1 = Number of sectors) 14+1 = 15 (0Eh = 14)
76h 78h	3Bh 3Ch	0000h 0001h	Region 4 Information (z × 256 Byte = sector size) 256 × 256 Byte = 64K Byte (100h = 256)

Table 10-d: Primary Vendor-Specific Extended Query

Address		Data	Description
Byte Mode	Word Mode		
80h 82h 84h	40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
86h	43h	0031h	Major version number, ASCII
88h	44h	0030h	Minor version number, ASCII
8Ah	45h	0000h	Address sensitive unlock (00h = required, 01h = not required)
8Ch	46h	0002h	Erase Suspend (00h = not supported, 01h = Read only, 2 = Read and Write)
8Eh	47h	0001h	Sector Protect (00h = not supported, n = number of sectors in per group)
90h	48h	0001h	Temporary Sector Unprotect (00h = not supported, 01h = supported)
92h	49h	0004h	Sector Protect/Unprotect scheme
94h	4Ah	0000h	Simultaneous R/W Operation (00h = not supported)
96h	4Bh	0000h	Burst Mode (00h = not supported, 01h = supported)
98h	4Ch	0000h	Page Mode (00h = not supported, 01h = supported)