Preliminary

SANYO

05.02.18 Ver2.23

LV24020LP Development Specifications

Ultra-compact FM tuner IC for mobile set

Overview

The LV24020LP is FM tuner IC's that requires absolutely no external components.

They incorporates not only the FM tuner functions as well in a compact VQLP package with dimensions of only 5 x 5 x 0.8mm.

These IC's are simply ideal for incorporating FM tuner functions into mobile phones and other small mobile set where space is always at a premium.

Functions

LV24020LP

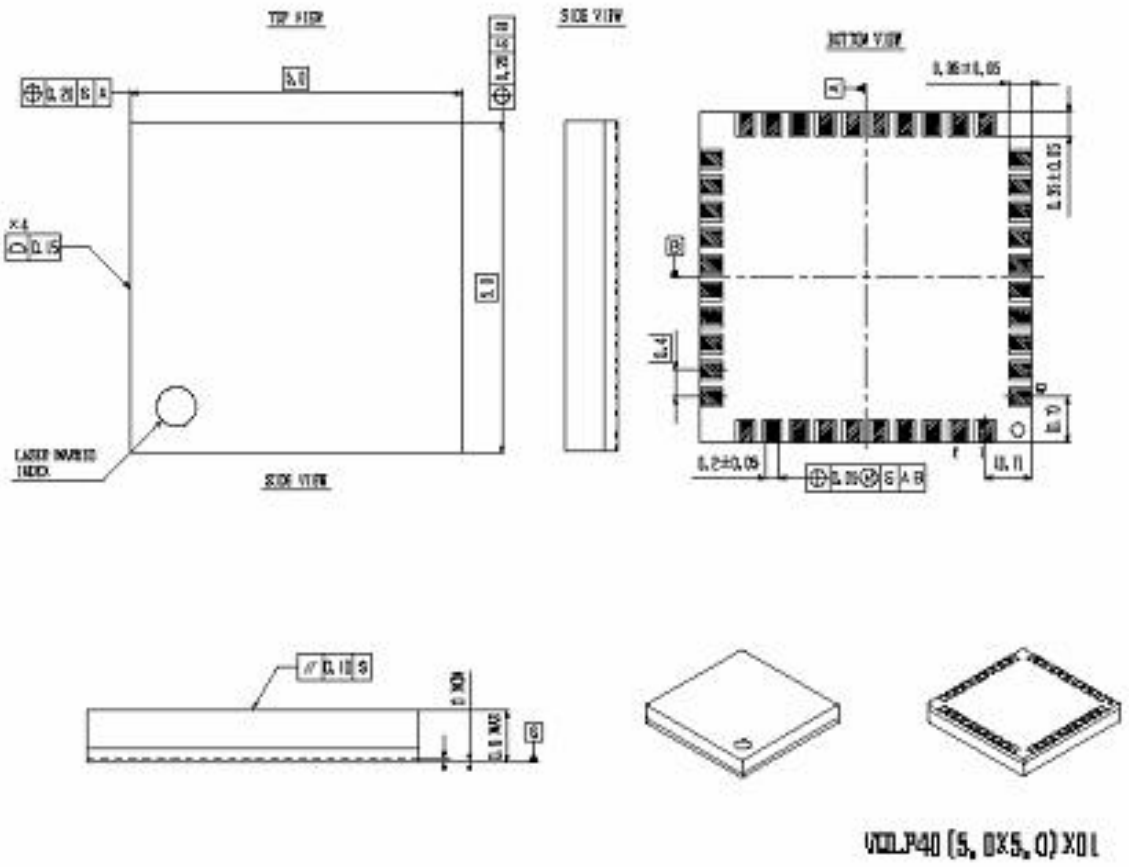
FM FE / FM IF / MPX Stereo Decoder / Tuning / Muting /Standby

Features

- No external components
- No alignments necessary
- Fully integrated low IF selectivity and demodulation
- Built in adjacent channel interference total reduction (no 114kHz, no 190kHz)
- Due to new tuning concept, the tuning is independent of the channel spacing
- Very high sensitivity due to integrated low noise RF input amplifier
- Very low power Standby mode. No power switch circuitry required
- MPX output for RDS application
- 3-wire bus interface (Date, Clock, NR-W)
- Digital AFC - Tuner locks to frequency after tuning sequence
- 8 level programmable Soft Mute
- 8 level programmable Stereo Blend
- In combination with the host, fast, low power operation of preset mode, manual search, automatic search and automatic preset store are possible
- Covers all Japanese, European and US bands

Package dimension

LV24020LP　VQLP40　　(5 x 5 x 0.8 mm)



Specifications

Maximum Ratings at Ta =25°C

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Maximum Supply Voltage	VCC max	Analog Supply Voltage	6.0	V
	VDD max	Digital Supply Voltage	5.0	V
Digital Input Voltage	Vin1 max	Clock,Data,NR_W	Vdd+0.3	mA
	Vin2 max	External_clk_in	Vdd+0.3	V
Allowable Power Dissipation	Pd max		140	mW
Storage Temperature	Tstg		-40 ～ +125	C
Operating Temperature	Topr		-20 ～ +70	C

Operating Conditions at Ta = 25°C $V_{CC} = V_{DD}$

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Recommended Supply Voltage	VCC	Analog Block	3.0	V
	VDD	Digital Block	3.0	V
Operating Supply Voltage Range	VCC op		2.7 ～ 5.0	V
	VDD op		2.5 ～ 4.0	V
	VIO op	Interface Supply Voltage	1.8 ～ 4.0	V

Note:Power supply voltage VIO eqaual VDD,or Vio < Vdd (Vio□Vdd)

Interface Conditions at Ta = from -20°C to +70 °C,Vss=0V

PARAMETER	SYMBOL	CONDITIONS	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	--	4.0	V
Digital part input	VIH	High level input voltage range	0.7VDD	--	VDD	V
	VIL	Low level input voltage range	0	--	0.6	V
Digital part Output	I OL	Low level output current	2.0	--	--	mA
	VOL	Low level output voltage IOL=2mA	--	--	0.6	V
Clock input Frequency	fclk	3wire_bus (29pin)Clock Frequency	--	--	0.7	MHz
External clock Frequency	f_{clk_ext}	CLK_IN (31Pin)Frequency	32K	--	14M	Hz

Note: CLK_IN (31pin)can input sign wave.*Extternl clock deviation is need 250ppm.

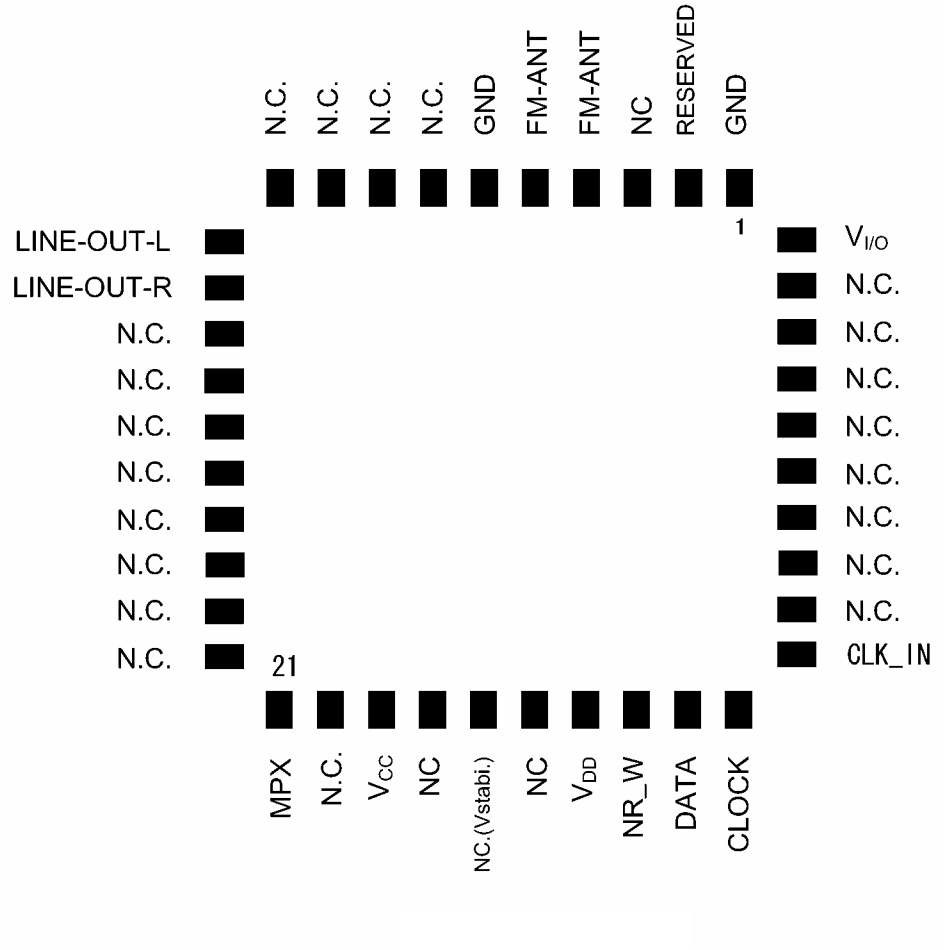
Operating Characteristics at Ta = 25°C, Vcc=3.0V , Vdd=3.0V , Vol=14, Soft Mute / Stereo=off

Vol=14 –Block2 register09h Volume_Bit 3-0 = 0010B

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operational Supply Current	ICCA	Analog Block at 60dBu input The 23pin is measured *except LV24002 HP AMP current LV24000 LV24002	--	14	17	mA
	ICCD	Digital Block at 60dBu input The 27,40 pin are measured.	0.2	0.4	0.8	
Standby supply Current	ICCA	Analog standby mode The 23 pin is measured.	--	3	30	uA
	ICCD	Digital standby mode The 27,40 pins are measured.	--	3	30	
FM Coverd frq	F_range	See Appendix	76	--	108	MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
[FM Receiving characteristics ;MONO] :fc=80MHz,fm=1kHz,22.5kHzdev. soft_stereo,soft_mute,Buss,Treble are all OFF.						
Input limiting voltage	-3dB LS	Vin=60dBμ standard for a -3dB input	--	13	19	dBμV EMF
Practical sensitivity	QS1	for 30dB signal to noise ratio input Deemphasis is 75 μsec SG open	--	10	16	dBμV EMF
Practical sensitivity	QS2	for 26dB signal to noise ratio input Deemphasis is 75 μsec SG close	--	1.25	--	μV
Demodulator Output level	Vo	Vin=60dBu, 11pin output level	60	100	140	mV
Channel balance	CB	Vin=60dBu, ratio of 11pin to 12pin output level	-2	0	2	dB
Signal to noise ratio	S/N	Vin=60dBu, 11pin output level	48	58	--	dB
Total harmonic distortion 1(MONO)	THD1	Vin=60dBu, 22.5KHzdev,11pin output	--	0.4	1.5	%
Total harmonic distortion 2(MONO)	THD2	Vin=60dBu, 75KHzdev,11pin output	--	1.3	3.0	%
Field strength level	FS	Input lever for FS1 to FS2	8	18	27	dBu
Muting attenation	Mute-Att	Vin=60dBu, 11pin output level	60	70	--	dB
[FM Receiving characteristics ;STEREO] :fc=80MHz,fm=1kHz,Vin=60dBμV,L+R=30%(22.5KHzdev),Pilot=10%(7.5Khzdev)						
Separation	SEP	L-mod,11pin→12pin output level	20	35	--	dB
Total harmonic distortion (STEREO)	THD-ST	Main-mod(L+R), 11pin/12pin output,IHF_BPF	--	0.6	1.8	%

LV24020LP pin layout



LV24020LP

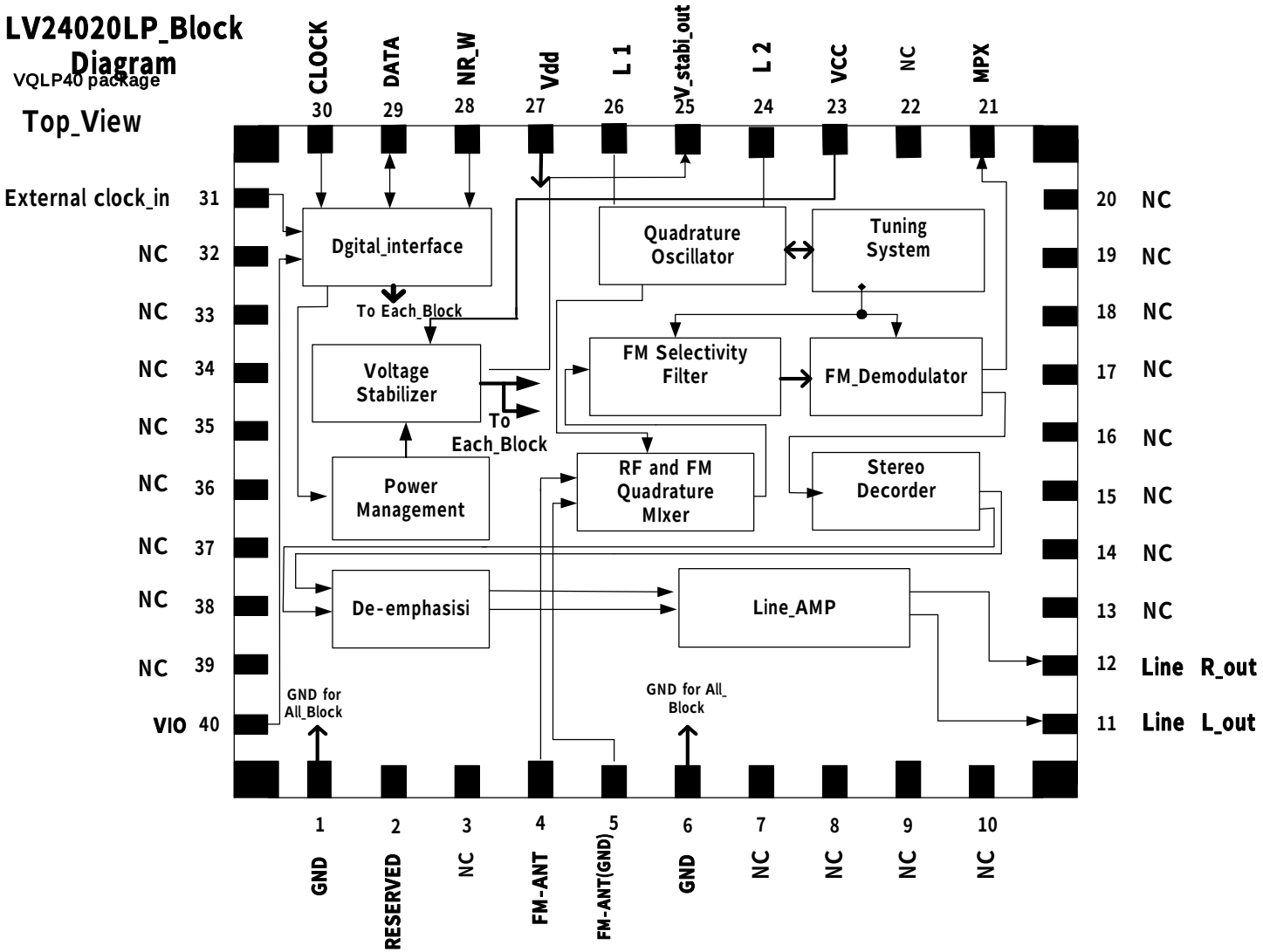
VQLP40 package Pin Description

Pin	LV24020LP	Description	Remark	DC_bias
1	GND	GND(Analog and Digital GND)		
2	RESERVED		Do not connect	
3	NC			
4	FM-ANT1	Antenna input		
5	FM-ANT2	Antenna GND	Connect to GND	
6	GND	GND（Analog and Digital GND)		
7	NC	Headphone Rch output		1.2V
8	NC	Headphone common	Not DC GND	1.2V
9	NC	Headphone Lch output		1.2V
10	NC	Headphone supply voltage		
11	LINE-OUT-L	Radio Lch Line-output		1.2V
12	LINE-OUT-R	Radio Rch Line-output		1.2V
13	NC			
14	NC			
15	NC			
16	NC			
17	NC			
18	NC			
19	NC	Rch Line-input		1.4V
20	NC	Lch Line-input		1.4V
21	MPX	MPX-signal output		Vcc-0.3V
22	NC			
23	VCC	Analog supply voltage		
24	NC (L2)	Internal coil2	Do not connect	2.7V
25	Vstabi.	Stabilizer voltage		2.7V
26	NC (L1)	Internal coil1	Do not connect	2.7V
27	VDD	Digital supply voltage		
28	NR_W	Digital interface Read/Write		
29	DATA	Digital interface DATA		
30	CLOCK	Digital interface Clock		
31	CLK_IN	Reference clock-source input for measurement	Connect to GND if not used	
32	NC			
33	NC			
34	NC			
35	NC			
36	NC			
37	NC			
38	NC			
39	NC			
40	VI/O	Digital interface supply voltage		

LV24020LP_Block Diagram

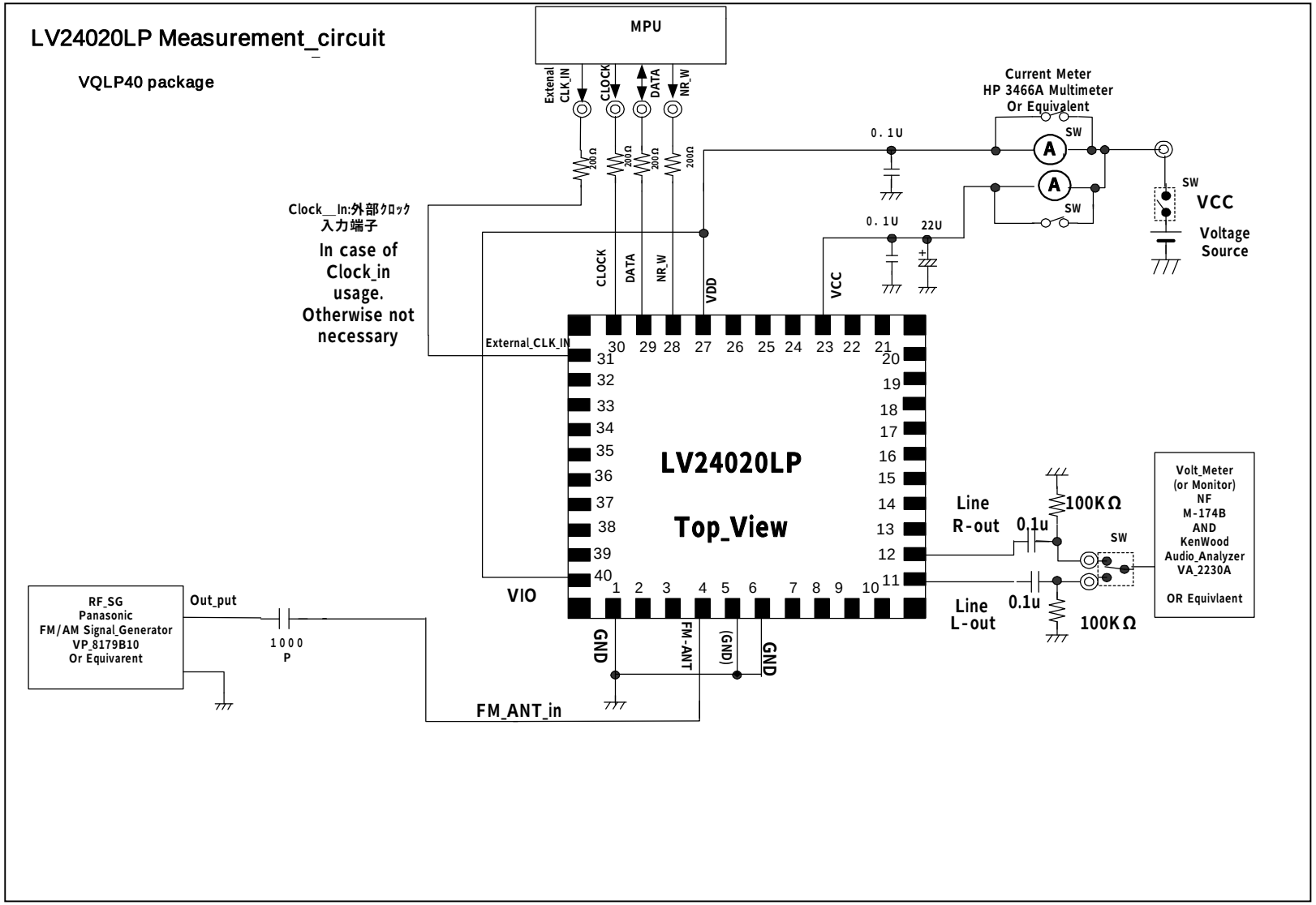
VQLP40 package

Top_View



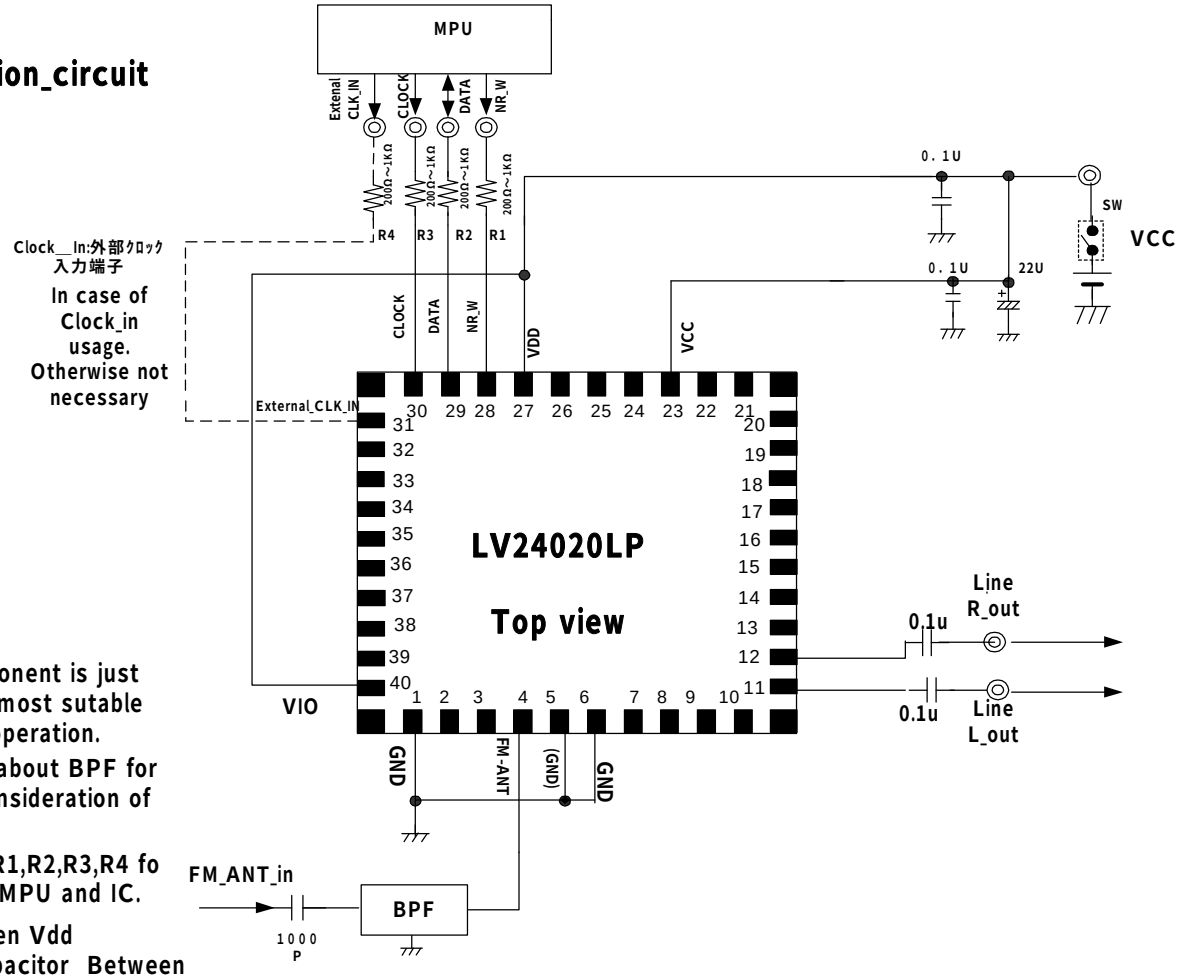
LV24020LP Measurement_circuit

VQLP40 package



LV24020LP application_circuit

VQLP40 package



Note1: Vale of Extenal Component is just reference. Please set most sutable value under Acutual_ operation.

Note2: In case of necessary about BPF for FM_in, Please take Consideration of most suitable_value.

Note3: We recomend to put R1,R2,R3,R4 fo for interface between MPU and IC.

Note4: put Capacitor Between Vdd and GND also, put Capacitor Between Vcc and GND in case of supply voltage not Staible, as shown on application.