

# SLIC-E/-E2

Subscriber Line Interface Circuit  
Enhanced Feature Set

PEB 4265, Version 1.2

PEB 4265-2, Version 1.2

Wired  
Communications



Never stop thinking.

---

## Preliminary Data Sheet

**Revision History:**           **2003-01-24**

DS1

---

Previous Version:           none

---

Page	Subjects (major changes since last revision)

---

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at <http://www.infineon.com>.

ABM<sup>®</sup>, ACE<sup>®</sup>, AOP<sup>®</sup>, ARCOFI<sup>®</sup>, ASM<sup>®</sup>, ASP<sup>®</sup>, DigiTape<sup>®</sup>, DuSLIC<sup>®</sup>, EPIC<sup>®</sup>, ELIC<sup>®</sup>, FALC<sup>®</sup>, GEMINAX<sup>®</sup>, IDEC<sup>®</sup>, INCA<sup>®</sup>, IOM<sup>®</sup>, IPAT<sup>®</sup>-2, ISAC<sup>®</sup>, ITAC<sup>®</sup>, IWE<sup>®</sup>, IWORX<sup>®</sup>, MUSAC<sup>®</sup>, MuSLIC<sup>®</sup>, OCTAT<sup>®</sup>, OptiPort<sup>®</sup>, POTSWIRE<sup>®</sup>, QUAT<sup>®</sup>, QuadFALC<sup>®</sup>, SCOUT<sup>®</sup>, SICAT<sup>®</sup>, SICOFI<sup>®</sup>, SIDEC<sup>®</sup>, SLICOFI<sup>®</sup>, SMINT<sup>®</sup>, SOCRATES<sup>®</sup>, VINETIC<sup>®</sup>, 10BaseV<sup>®</sup>, 10BaseVX<sup>®</sup> are registered trademarks of Infineon Technologies AG. 10BaseS<sup>™</sup>, EasyPort<sup>™</sup>, VDSLite<sup>™</sup> are trademarks of Infineon Technologies AG. Microsoft<sup>®</sup> is a registered trademark of Microsoft Corporation. Linux<sup>®</sup> is a registered trademark of Linus Torvalds.

The information in this document is subject to change without notice.

**Edition 2003-01-24**

**Published by Infineon Technologies AG,  
St.-Martin-Strasse 53,  
81669 München, Germany**

**© Infineon Technologies AG 2003.  
All Rights Reserved.**

### **Attention please!**

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

### **Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

<b>Table of Contents</b>		<b>Page</b>
<b>1</b>	<b>Overview</b> .....	7
1.1	Features .....	8
1.2	Logic Symbol .....	9
1.3	Pin Configuration .....	10
1.4	Pin Definitions and Functions .....	12
1.5	Functional Block Diagram .....	14
<b>2</b>	<b>Functional Description</b> .....	15
2.1	Operating Modes .....	17
2.2	Current Limitation/Overtemperature .....	18
<b>3</b>	<b>Typical Application Circuit for DuSLIC and VINETIC</b> .....	19
<b>4</b>	<b>Electrical Characteristics</b> .....	23
4.1	Absolute Maximum Ratings .....	23
4.2	Foreign Line Voltages .....	24
4.3	Power Up Sequence of Supply Voltages .....	24
4.4	Operating Range .....	25
4.5	Thermal Resistances .....	25
4.6	Electrical Parameters .....	26
4.6.1	Supply Currents and Power Dissipation .....	26
4.6.2	DC Characteristics .....	29
4.6.3	AC Characteristics .....	32
<b>5</b>	<b>Test Figures</b> .....	36
<b>6</b>	<b>Package Outlines</b> .....	40
6.1	Recommended PCB Foot Print Pattern for the P-VQFN-48-4 .....	42

<b>List of Figures</b>		<b>Page</b>
Figure 1	Logic Symbol . . . . .	9
Figure 2	Pin Configuration P-DSO-20-5 Package (top view) . . . . .	10
Figure 3	Pin Configuration P-VQFN-48-4 Package (top view) . . . . .	11
Figure 4	Block Diagram . . . . .	14
Figure 5	Definition of Output Current Directions . . . . .	16
Figure 6	Application Circuit DuSLIC . . . . .	21
Figure 7	Application Circuit VINETIC . . . . .	22
Figure 8	Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR . . . . .	31
Figure 9	Typical Frequency Dependence of PSRR VBATL/VTR . . . . .	34
Figure 10	Typical Frequency Dependence of PSRR VBATH/VTR . . . . .	34
Figure 11	Typical Frequency Dependence of PSRR VDD/VTR . . . . .	35
Figure 12	Output Current Limit. . . . .	36
Figure 13	Output Resistance PDRH, PDRHL . . . . .	36
Figure 14	Current Outputs IT, IL . . . . .	37
Figure 15	Transmission Characteristics. . . . .	37
Figure 16	Longitudinal to Transversal Rejection . . . . .	38
Figure 17	Longitudinal to Transversal Rejection Loop. . . . .	38
Figure 18	Transversal to Longitudinal Rejection . . . . .	39
Figure 19	Ring Amplitude. . . . .	39
Figure 20	Package Outline for P-DSO-20-5. . . . .	40
Figure 21	Package Outline for P-VQFN-48-4 . . . . .	41
Figure 22	Foot Print for P-VQFN-48-4 . . . . .	42

<b>List of Tables</b>		<b>Page</b>
Table 1	Pin Definitions and Functions SLIC-E/-E2 . . . . .	12
Table 2	SLIC-E/-E2 Interface Code . . . . .	17
Table 3	SLIC-E/-E2 Modes . . . . .	17
Table 4	External Components DuSLIC / VINETIC for 2 Channels . . . . .	19
Table 5	Absolute Maximum Ratings . . . . .	23
Table 6	Voltage Limits on Output Pins . . . . .	24
Table 7	Current Limits on Output Pins . . . . .	24
Table 8	Operating Range . . . . .	25
Table 9	Thermal Resistances . . . . .	25
Table 10	Supply Currents, Power Dissipation ( $I_R = I_T = 0$ A; $V_{RT} = 0$ V) . . . . .	26
Table 11	Voltage Dependence of Supply Currents . . . . .	28
Table 12	Output Stage Power Dissipation . . . . .	28
Table 13	DC Characteristics . . . . .	29
Table 14	AC Characteristics . . . . .	32

## Preface

This document describes the High Voltage Subscriber Line Interface Circuit Enhanced Feature Set SLIC-E/-E2 (PEB 4265) which is part of the DuSLIC and VINETIC chip set family. For more DuSLIC related documents please see our webpage at <http://www.infineon.com/duslic>.

### Organization of this Document

This Preliminary Data Sheet is divided into six chapters. It is organized as follows:

- **Chapter 1, Overview**  
A general description of the product, its key features, and pin configuration.
- **Chapter 2, Functional Description**  
The main functions and operating modes are presented.
- **Chapter 3, Typical Application Circuit for DuSLIC and VINETIC**  
Application circuit including bill of material and protection.
- **Chapter 4, Electrical Characteristics**  
Parameters, symbols and limit values.
- **Chapter 5, Test Figures**  
Test figures including external components.
- **Chapter 6, Package Outlines**  
Illustrations and dimensions of the package outlines.

## **1 Overview**

The High Voltage Subscriber Line Interface Circuit SLIC-E/-E2 (PEB 4265) is a reliable interface between the telephone line and the codec devices of the DuSLIC or VINETIC chip sets. It is fabricated using Infineon Technologies' well-proven Smart Power Technology SPT 170.

The SLIC-E/-E2 provides battery feeding between  $-15\text{ V}$  and  $-85\text{ V}$  and internal balanced ringing up to  $85\text{ V}_{\text{rms}}$ . In order to achieve this, an auxiliary positive battery voltage is used during ringing to enhance the useable voltage range to  $150\text{ V}$ .

The SLIC is designed for a voltage-feeding/current-sensing line interface concept and senses the transversal and longitudinal current.

To minimize system power dissipation, a power-down mode can be used; the PEB 4265 is switched off and the line outputs go to a high-impedance mode. Off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

For saving power in active mode an integrated switch enables the use of a lower battery voltage in short loop applications.

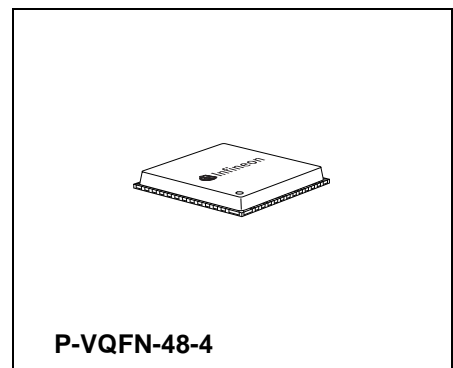
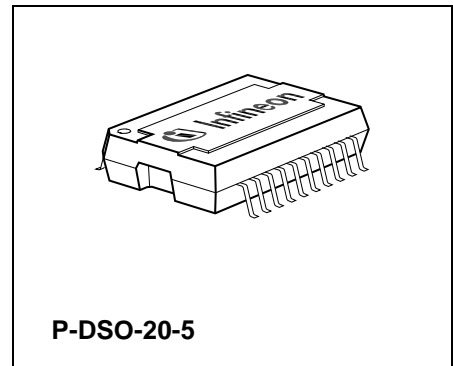
**SLIC-E/-E2**  
**Subscriber Line Interface Circuit**  
**Enhanced Feature Set**

**PEB 4265**  
**PEB 4265-2**

**Version 1.2**

**1.1 Features**

- High-voltage line feeding
- Two Battery voltages (–15 V ... –85 V)
- Total supply voltage up to 150 V
- Long loop driving capability
- Integrated balanced ringing up to 85 Vrms
- Power-saving active mode (ACTL) with reduced battery voltage
- Sensing of transversal and longitudinal line currents
- Integrated test mode (ACTH-R)
- Package options:
  - P-DSO-20-5
  - P-VQFN-48-4
- High longitudinal balance performance with PEB 4265-2
- Reliable Smart Power Technology (SPT170)
- Enables high packing densities on board



Type	Package
PEB 4265 / PEB 4265-2	P-DSO-20-5 or P-VQFN-48-4

## 1.2 Logic Symbol

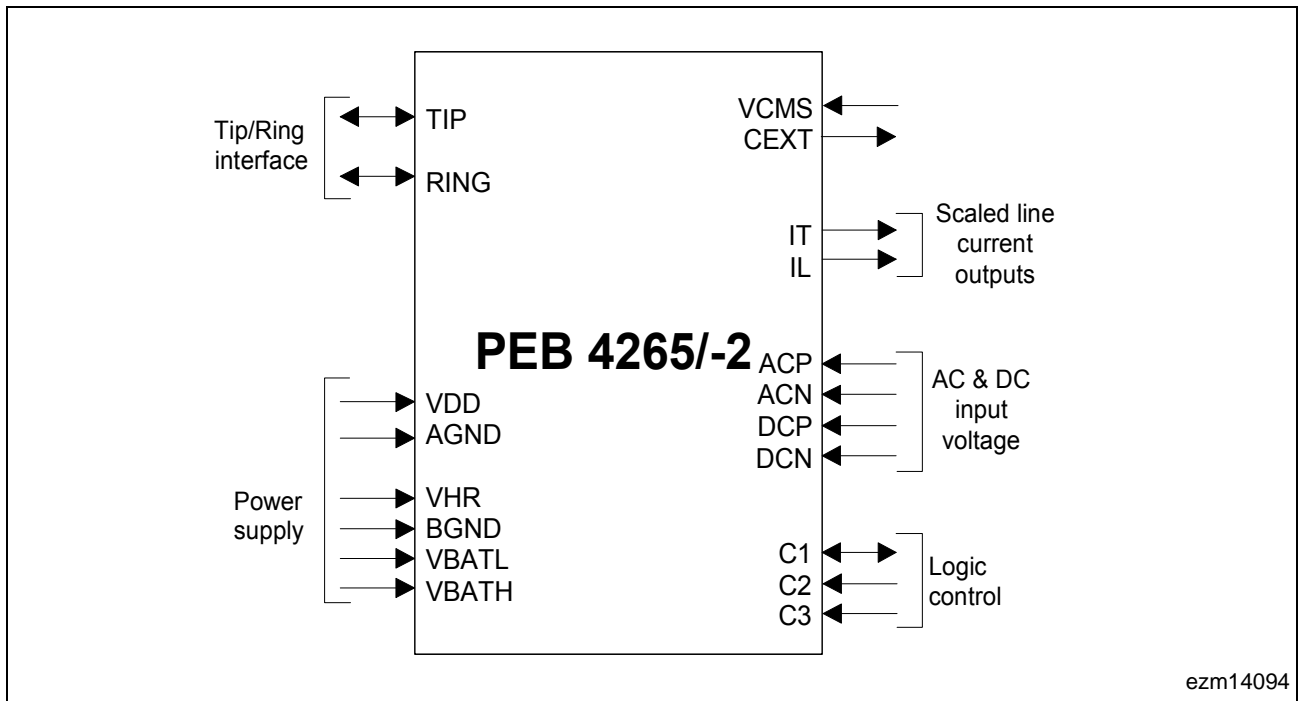
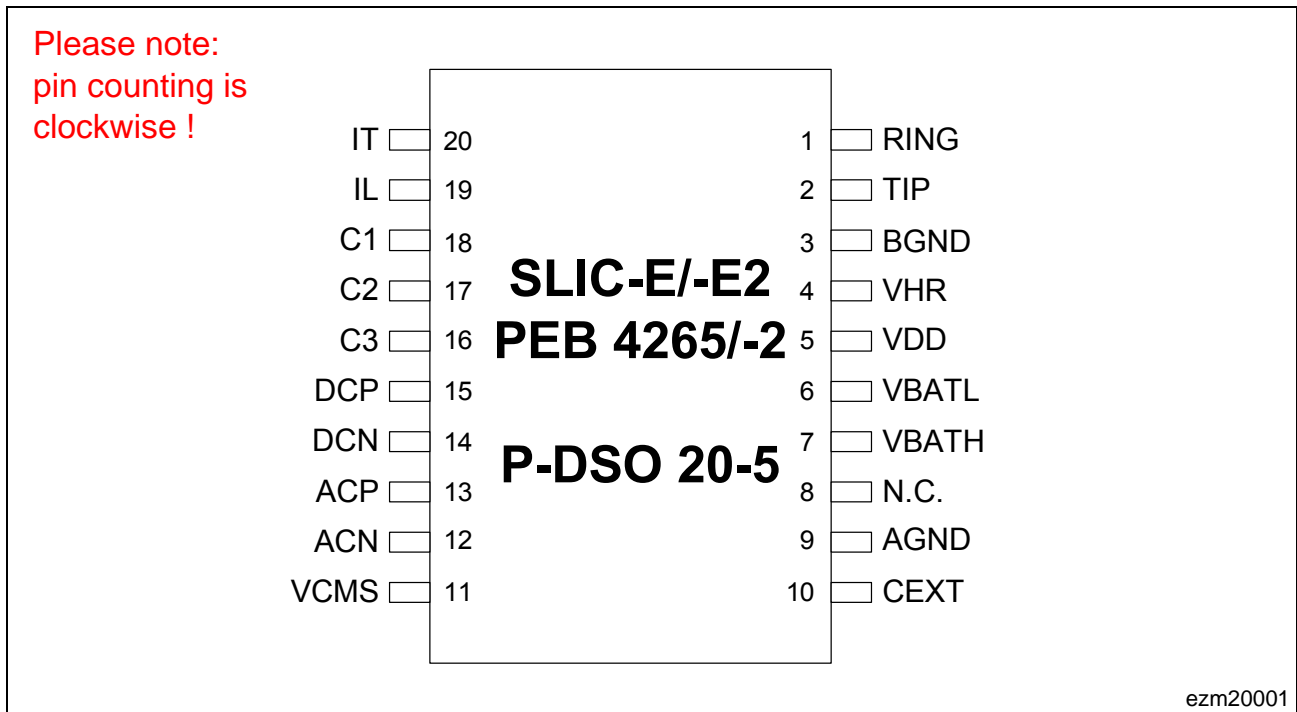


Figure 1 Logic Symbol

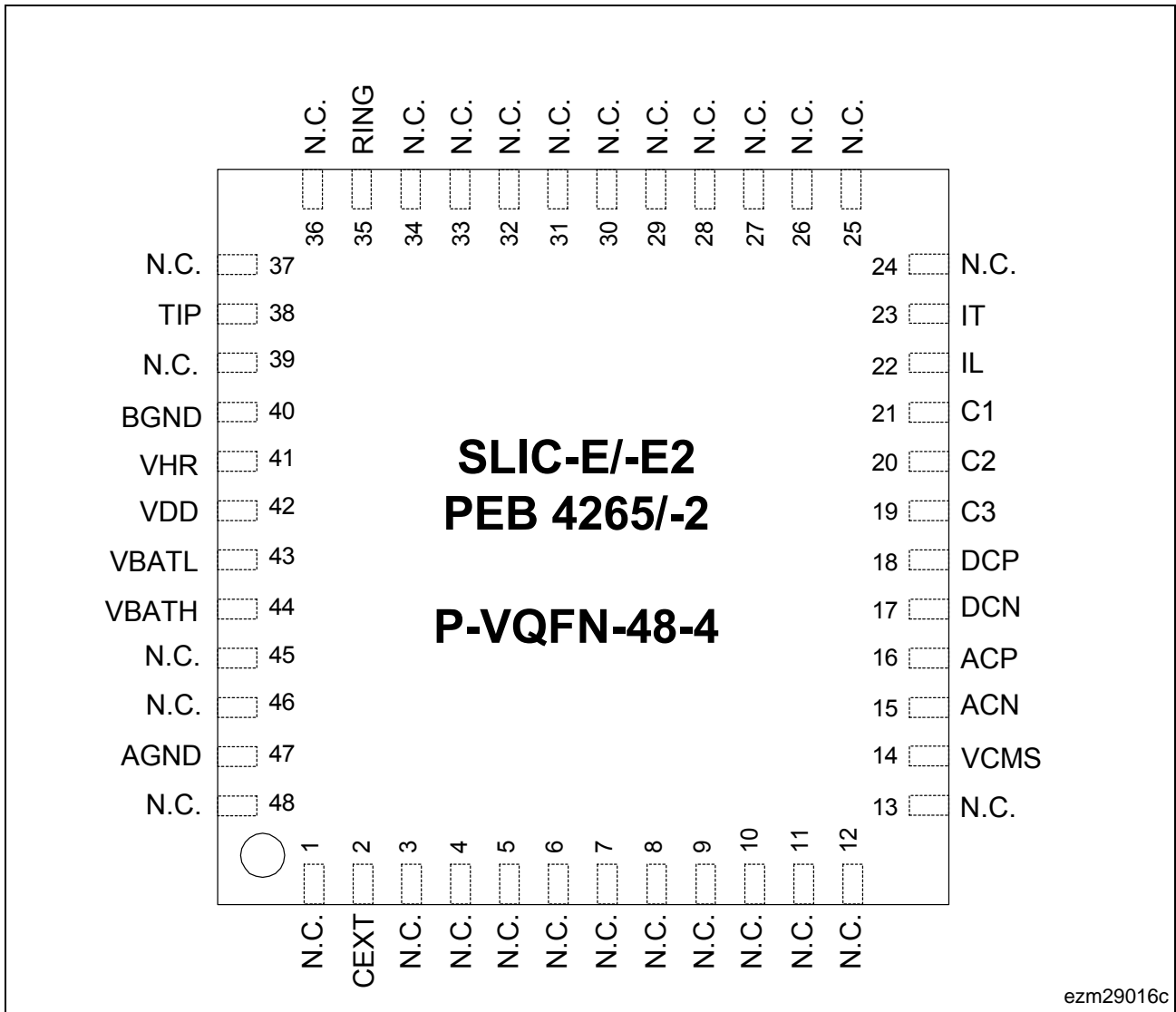
### 1.3 Pin Configuration



**Figure 2** Pin Configuration P-DSO-20-5 Package (top view)

*Note: The P-DSO-20-5 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).*

**Attention: The heatsink (see [Figure 20](#)) is connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.**



ezm29016c

**Figure 3 Pin Configuration P-VQFN-48-4 Package (top view)**

**Attention:** The exposed die pad and die pad edges are connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the die pad or any attached conducting part can be hazardous.

## 1.4 Pin Definitions and Functions

**Table 1 Pin Definitions and Functions SLIC-E/-E2**

Pin No.		Symbol	Input (I) Output (O)	Function
P-DSO-20-5	P-VQFN-48-4			
1	35	RING	I/O	Subscriber loop connection RING.
2	38	TIP	I/O	Subscriber loop connection TIP.
3	40	BGND	Power	Battery ground: TIP, RING, $V_{BATH}$ , $V_{BATL}$ and $V_{HR}$ refer to this pin.
4	41	VHR	Power	Auxiliary positive battery supply voltage ( $5\text{ V} \leq V_{HR} \leq 85\text{ V}$ ) used in ringing mode.
5	42	VDD	Power	Positive supply voltage (+5 V), referred to AGND.
6	43	VBATL	Power	Negative battery supply voltage ( $-15\text{ V} \geq V_{BATL} \geq V_{BATH}$ )
7	44	VBATH	Power	Negative battery supply voltage ( $-20\text{ V} \geq V_{BATH} \geq -85\text{ V}$ )
9	47	AGND	Power	Analog ground: $V_{DD}$ , and all signal and control pins with the exception of TIP and RING refer to AGND.
10	2	CEXT	O	Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance 50 k $\Omega$ ).
11	14	VCMS	I	Reference voltage for differential two wire interface of typically 1.5 V.
12, 13	15, 16	ACN, ACP	I	Differential two-wire AC input voltage; multiplied by $-6$ and related to $(V_{HI} + V_{BI})/2^1$ , ACN appears at the TIP and ACP at the RING output, respectively.
14, 15	17, 18	DCN, DCP	I	Differential two-wire DC input voltage; multiplied by $-30$ (ACTH and ACTL mode) or $-60$ (ACTR mode) and related to $(V_{HI} + V_{BI})/2$ , DCN appears at the TIP and DCP at the RING output, respectively.

**Table 1 Pin Definitions and Functions SLIC-E/-E2 (cont'd)**

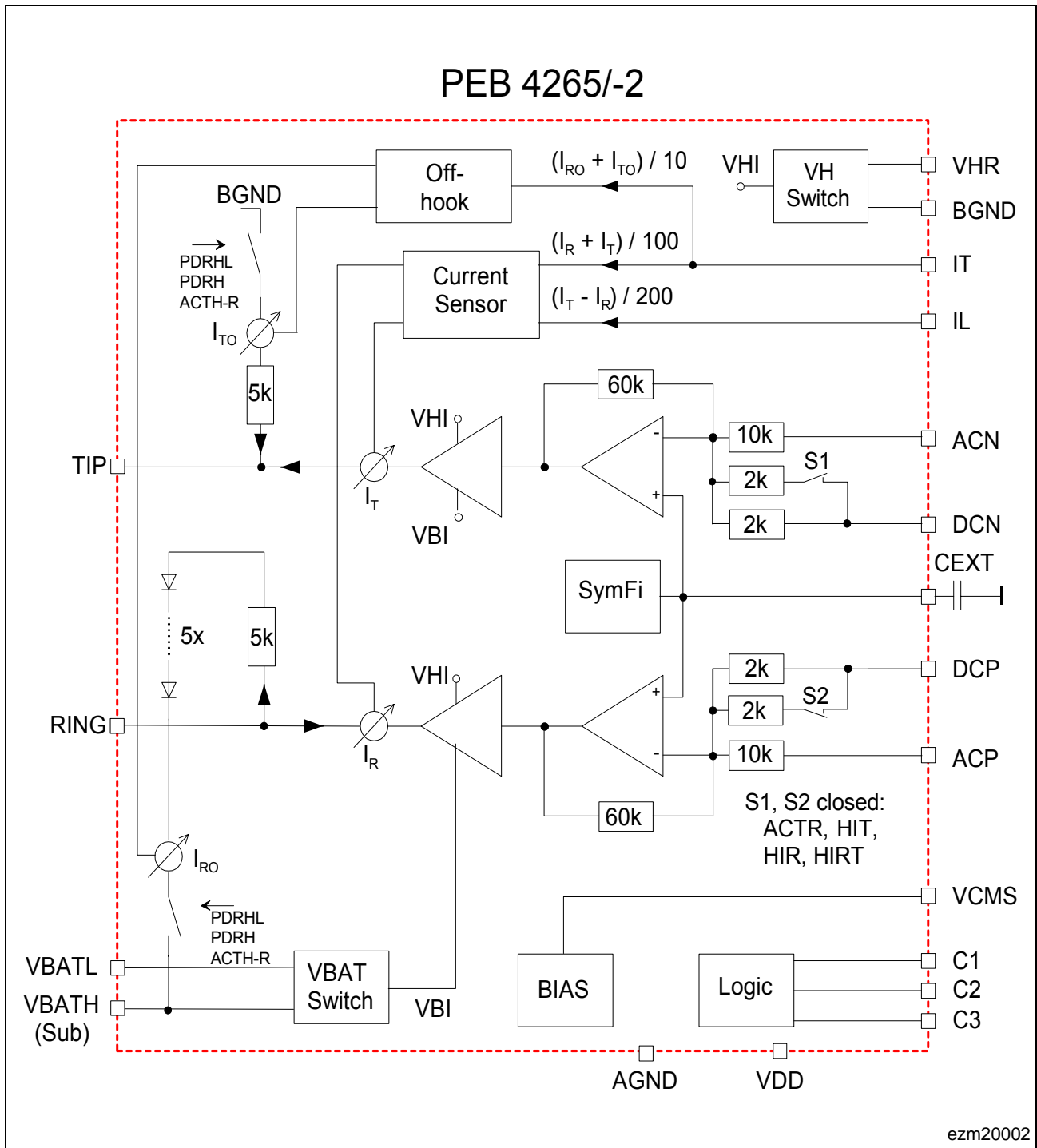
Pin No.		Symbol	Input (I) Output (O)	Function
P-DSO-20-5	P-VQFN-48-4			
16	19	C3	I	Ternary logic input, controlling the operation mode. Internal pull-down (C3 = L, if not connected)
17	20	C2	I	Ternary logic input, controlling the operation mode.
18	21	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C) this pin sinks a current of typically 150 $\mu$ A.
19	22	IL	O	Current output: Longitudinal line current scaled down by a factor of 100
20	23	IT	O	Current output: Transversal line current scaled down by a factor of 50
8	2)	N.C.		Not connected.

<sup>1)</sup>  $V_{HI}$  is the output voltage of the positive battery switch,

$V_{BI}$  is the output voltage of the negative battery switch (see [Figure 4](#)).

<sup>2)</sup> For the P-VQFN-48-4 the following pins are not connected: 1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 36, 37, 39, 45, 46, 48

### 1.5 Functional Block Diagram



**Figure 4** Block Diagram

## 2 Functional Description

The SLIC-E/-E2 supports AC and DC control loops based on feeding a voltage  $V_{TR}$  to the line and sensing the transversal line current  $I_{Trans}$  and the longitudinal current  $I_{Long}$  (**Figure 5**).

In receive direction DC and AC voltages are handled separately with different gains on the PEB 4265. Both are applied differentially via pins DCP and DCN or ACP and ACN, respectively.

The line voltages  $V_R$  and  $V_T$  are the amplified input voltages, related to the mean supply voltage  $V_M = (V_{HI} + V_{BI})/2$ . Depending on the operation mode,  $V_{HI}$  is switched either to  $V_{HR}$  or to BGND via the VH switch and  $V_{BI}$  is switched either to  $V_{BATL}$  or to  $V_{BATH}$  via the VBAT switch (see **Figure 4**).

In the active modes ACTH with  $V_M = V_{BATH}/2$  and ACTL with  $V_M = V_{BATL}/2$ , the line voltages are given by

$$V_T = V_{TIP} = V_M - 30 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$

$$V_R = V_{RING} = V_M - 30 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS}),$$

while in ringing mode ACTR with  $V_M = [V_{HR} + V_{BATH}]/2$ ,

$$V_T = V_{TIP} = V_M - 60 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$

$$V_R = V_{RING} = V_M - 60 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS})$$

The transversal line voltage  $V_{TR} = V_T - V_R$  is simply related to the input voltages:

$$V_{TR} = V_{TIP} - V_{RING} = V_{ab} =$$

$= 30 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$	for modes ACTH, ACTL
$= 60 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$	for mode ACTR

A reversed polarity of  $V_{TR}$  is easily obtained by changing the sign of  $(V_{DCP} - V_{DCN})$ .

Functional Description

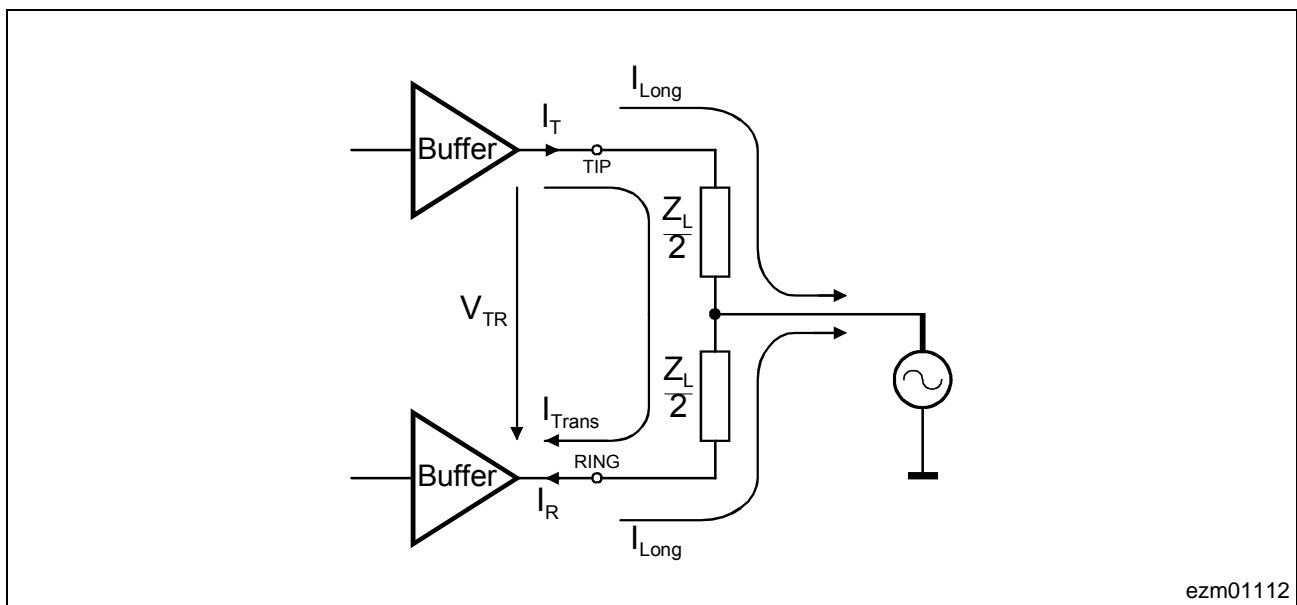
In transmit direction the transversal and longitudinal currents are measured and scaled images are provided at the IT and IL pin, respectively:

$I_{IT} = (I_T + I_R)/100 = I_{Trans}/50$	$I_{IL} = (I_T - I_R)/200 = I_{Long}/100$
$I_{Trans} = (I_T + I_R)/2$	$I_{Long} = (I_T - I_R)/2$

For off-hook detection, in PDRH mode 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH, respectively.

The currents through these resistors,  $I_{T0}$  and  $I_{R0}$  are sensed, scaled and provided at the IT pin (see [Figure 4](#))

$$I_{IT0} = (I_{T0} + I_{R0})/10 = I_{TRANS0}/5$$



ezm01112

Figure 5 Definition of Output Current Directions

## 2.1 Operating Modes

The PEB 4265/-2 (SLIC-E/-E2) operates in the following modes controlled by ternary logic signals at C1, C2 and a binary signal at C3:

**Table 2 SLIC-E/-E2 Interface Code**

		C2				
		L	M	H		
C1	L <sup>1)</sup>	PDH	PDRHL	PDRH	L or N.C.	C3
		HIRT			H	
	M	ACTL	ACTH	ACTR	L or N.C.	
		H	H			
	H	HIRT	HIT	HIR	L or N.C.	
		ACTH-R			H	

<sup>1)</sup> No 'Overtemp' signaling possible via pin C1 if C1 is low.

**Table 3 SLIC-E/-E2 Modes**

SLIC-E/-E2 Mode	Mode Description	Internal Supply Voltages $V_{BI}$ , $V_{HI}$
PDH	Power Down High Impedance	supply switches open
PDRH	Power Down Resistive High	supply switches open
PDRHL	Power Down Resistive High Load	supply switches open
ACTL	Active Low	$V_{BATL}$ , BGND
ACTH	Active High	$V_{BATH}$ , BGND
ACTH-R	Active High Resistive	$V_{BATH}$ , BGND
ACTR	Active Ring	$V_{BATH}$ , $V_{HR}$
HIRT	High Impedance on RING and TIP	$V_{BATH}$ , $V_{HR}$
HIT	High Impedance on TIP	$V_{BATH}$ , $V_{HR}$
HIR	High Impedance on RING	$V_{BATH}$ , $V_{HR}$

### Power Down High Impedance (PDH)

PDH offers high impedance at TIP and RING; it can be used for testing purposes or when an error condition occurs. In PDH mode all functions are switched off. Off-hook detection is not available.

### Power Down Resistive High (PDRH)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, PDRH provides a connection of 5 k $\Omega$  each from TIP to BGND and RING to VBATH, respectively, while the output buffers show high impedance (see [Figure 4](#)). The current through these resistors is sensed and transferred to the IT pin for off-hook supervision.

### Power Down Resistive High Load (PDRHL)

PDRHL is used as a transition state at a mode change from PDRH or PDH to ACTH mode (automatically initiated by the codec device at a mode change). It causes fast preloading of  $C_{EXT}$  in order to suppress line voltage transients.

### Active Low (ACTL), Active High (ACTH)

These are the regular transmission modes for voiceband. The line-driving section is operated between  $V_{BATL}$  or  $V_{BATH}$  and BGND.

### Active High Resistive (ACTH-R)

The SLIC is operated in Active High state together with the 5 k $\Omega$  resistors from TIP to BGND and from RING to VBATH. This mode is intended to be used for line testing.

### Active Ring (ACTR)

Utilizing an additional positive battery voltage  $V_{HR}$ , this mode allows balanced ringing of up to 85 V<sub>rms</sub> or feeding of very long telephone lines.

### High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer can still be measured by IT or IL. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

## 2.2 Current Limitation/Overtemperature

In any operating mode (except Power Down) the total current delivered by the output drivers is limited to approximately 100 mA.

If, however, the junction temperature exceeds 165 °C, the current limit is further reduced to keep the junction temperature constant.

Simultaneously, pin C1 sinks a signalling current  $I_{therm}$ .

**Typical Application Circuit for DuSLIC and VINETIC**

### 3 Typical Application Circuit for DuSLIC and VINETIC

**Figure 6 (Figure 7)** shows one channel of an application circuit including a SLIC-E/-E2 and a SLICOFI-2/-2S or VINETIC-4VIP/-4M/-8M chip (for latest information please refer to the DuSLIC or VINETIC Data Sheet).

**Table 4** shows the external passive components needed for a dual-channel solution as shown in **Figure 6** and **Figure 7**.

**Table 4 External Components DuSLIC / VINETIC for 2 Channels**

No.	Symbol	Value	Unit	Relat. Tol.	Rating	DuSLIC Systems	VINETIC Systems
2	$R_{IT1}$	470	$\Omega$	1 %		x	
2	$R_{IT1}$	510	$\Omega$	1 %			x
2	$R_{IT2}$	680	$\Omega$	1 %		x	x
2	$R_{IL}$	1.6	k $\Omega$	1 %		x	x
4	$R_{STAB}$	30	$\Omega$	1 % <sup>1)</sup>		x	x
4	$R_{PROT}$ <sup>2)</sup>	20 ... 50	$\Omega$	1 % <sup>1)</sup>		x	x
4	$C_{STAB}$	15 (typ.)	nF	10 %	100 V	x	x
2	$C_{DC}$	120	nF	10 %	10 V	x	
2	$C_{DC}$	220	nF	10 %	10 V		x
2	$C_{ITAC}$	680	nF	10 %	10 V	x	
2	$C_{ITAC}$	1	$\mu$ F	10 %	10 V		x
1	$C_{PRE}$ <sup>3)</sup>	18	nF	5 %	10 V		x
2	$C_{VCMIT}$	680	nF	10 %	10 V	x	
1	$C_{REF}$	68	nF	20 %	10 V	x	x
2	$C_{EXT}$	470	nF	20 %	10 V	x	x
7	$C_1$	typ. 100	nF	10 %	10 V	x	
13	$C_1$	typ. 100	nF	10 %	10 V		x
6	$C_2$	typ. 100	nF	10 %	100 V	x	x
1	$C_3$	4.7	$\mu$ F	20 %	10 V, Tantal	x	
2	$D_1$	BAS 21	–	–	–	x	x
4	$D_2$	BAS 21	–	–	–	x	x

Typical Application Circuit for DuSLIC and VINETIC

**Table 4 External Components DuSLIC / VINETIC for 2 Channels (cont'd)**

No.	Symbol	Value	Unit	Relat. Tol.	Rating	DuSLIC Systems	VINETIC Systems
2	$U_1^{2)}$	Overvoltage Protection Element	—	—	—	x	x

<sup>1)</sup> Matching tolerance dependent on longitudinal balance requirements (for details see the Application Note *External Components*).

<sup>2)</sup> See Application Note *Protection of DuSLIC / VINETIC Linecard Chip Sets against Overvoltages and Overcurrents*.

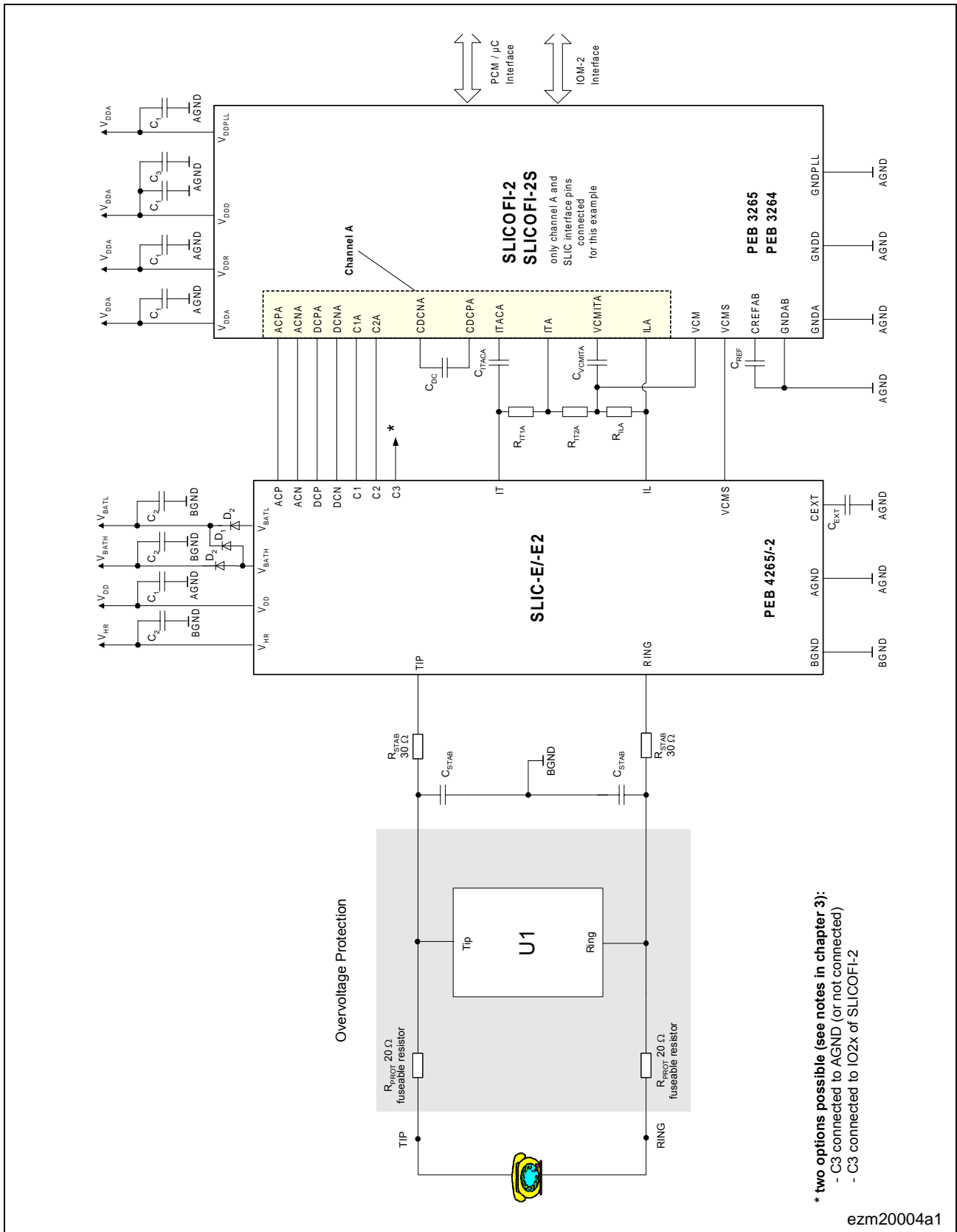
<sup>3)</sup>  $C_{PRE}$  is only necessary when TTX (12 or 16 kHz metering) is used.

The C3 pin of SLIC-E/-E2 can be either

- not connected (or connected to AGND) to be compatible with SLIC-E/-E2 Version 1.1 or
- connected to IO0x (IO2x) of VINETIC<sup>1)</sup> (SLICOFI-2/-2S) to offer an additional test mode ACTH-R.

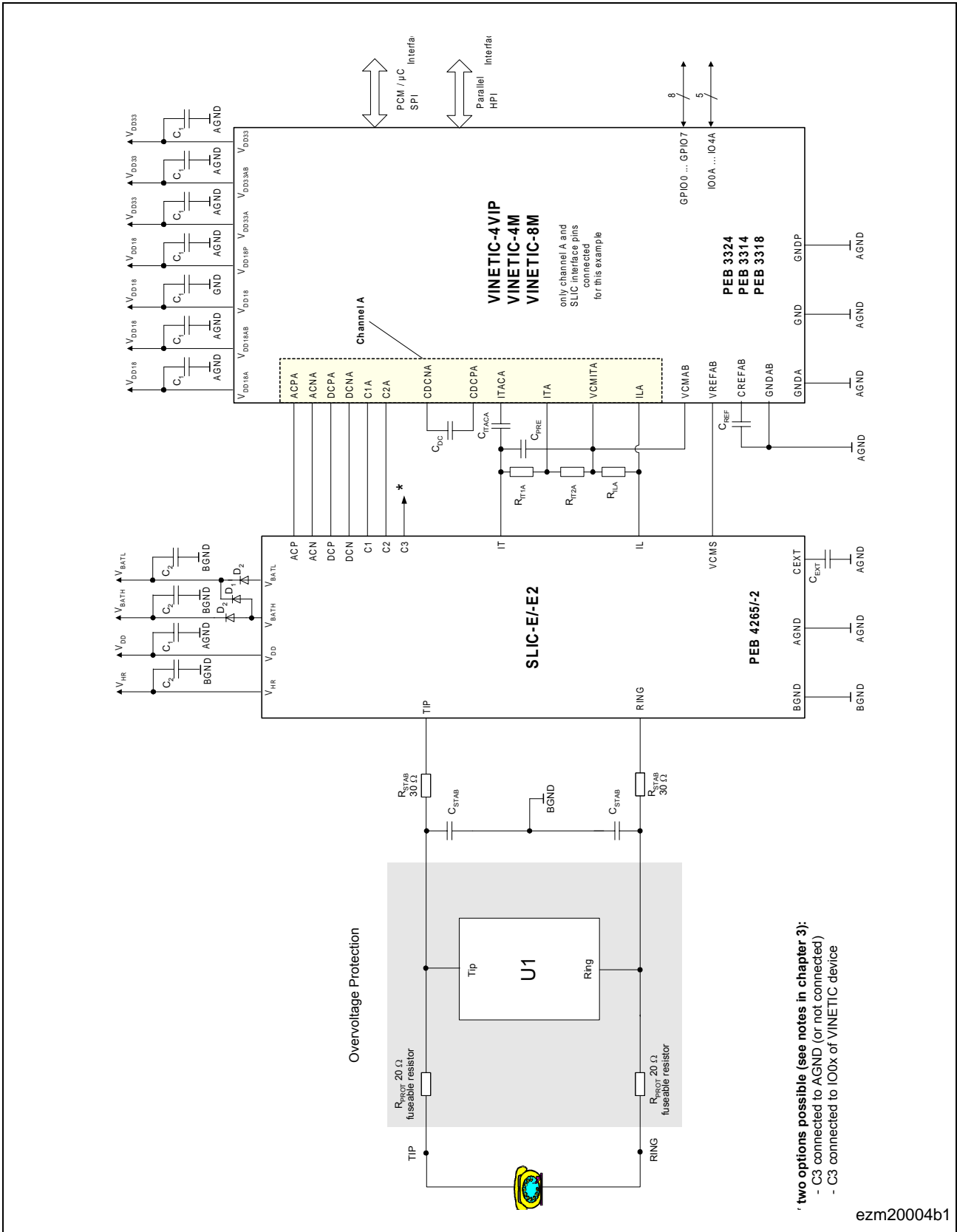
<sup>1)</sup> Please refer to the latest VINETIC documentation which IO pin has to be used.

**Typical Application Circuit for DuSLIC and VINETIC**



**Figure 6 Application Circuit DuSLIC**

**Typical Application Circuit for DuSLIC and VINETIC**



**Figure 7 Application Circuit VINETIC**

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

**Table 5 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Battery voltage low	$V_{\text{BATL}}$	-85	0.4	V	Referred to BGND
Battery voltage high	$V_{\text{BATH}}$	-90	0.4	V	Referred to BGND
Battery voltage difference	$V_{\text{BATL}} - V_{\text{BATH}}$	-0.4	-	V	-
Auxiliary supply voltage	$V_{\text{HR}}$	-0.4	90	V	Referred to BGND
Total battery supply voltage, continuous	$V_{\text{HR}} - V_{\text{BATH}}$	-	160	V	-
$V_{\text{DD}}$ supply voltage	$V_{\text{DD}}$	-0.4	7	V	Referred to AGND
Ground voltage difference BGND, AGND	-	-0.4	0.4	V	-
Input voltages	$V_{\text{DCP}}, V_{\text{DCN}}, V_{\text{ACP}}, V_{\text{ACN}}, V_{\text{C1}}, V_{\text{C2}}, V_{\text{CMS}}$	-0.4	$V_{\text{DD}} + 0.4$	V	Referred to AGND
Voltages on current outputs	$V_{\text{IT}}, V_{\text{IL}}$	-0.4	$V_{\text{DD}} + 0.4$	V	Referred to AGND
Junction temperature	$T_{\text{j}}$	-	150	°C	
ESD voltage, all pins	-	-	1	kV	SDM (Socketed Device Model) <sup>1)</sup>

<sup>1)</sup> EOS/ESD Assn. Standard DS5.3-1993.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.*

## 4.2 Foreign Line Voltages

External voltages applied at the line outputs cause a current flow in the SLIC-E/-E2. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, because overtemperature protection cannot react fast enough at high local power density. The value of allowed power dissipation strongly depends on its duration. It can be expressed in terms of voltage and current limits directly at the TIP/RING outputs.

**Table 6 Voltage Limits on Output Pins**

Duration of Voltage	Pins	Min. Voltage [V]	Max. Voltage [V]
Continuous	TIP, RING	$V_{BATH} - 0.4$	$V_{HR} + 5$
< 10 ms	TIP, RING	$V_{BATH} - 5$	$V_{HR} + 10$
< 100 $\mu$ s	TIP, RING	$V_{BATH} - 10$	$V_{HR} + 20$
< 1 $\mu$ s	TIP, RING	$V_{BATH} - 15$	$V_{HR} + 40$

**Table 7 Current Limits on Output Pins**

Duration of Current	Pins	Min. current [A]	Max. current[A]
Continuous	TIP, RING	- 0.1	0.1
< 10 ms	TIP, RING	- 0.5	0.5
< 100 $\mu$ s	TIP, RING	- 1	1.0
< 1 $\mu$ s	TIP, RING	- 1.5	1.5

The above limitations ([Table 6](#) and [Table 7](#)) have to be regarded as typical. They are valid simultaneously. Together with external circuitry they determine protection requirements (see Application Note of the DuSLIC/VINETIC chip set on overvoltages and overcurrents).

## 4.3 Power Up Sequence of Supply Voltages

It is recommended to apply the SLIC-E/-E2 supply voltages in the following order to the respective pins:

- 1) AGND, BGND
- 2)  $V_{DD}$
- 3)  $V_{BATH}$
- 4)  $V_{HR}$
- 5)  $V_{BATL}$

When powering down the SLIC-E/-E2, the supply voltages have to be removed in reverse order.

With the use of the diodes  $D_1$  and  $D_2$  (see application circuits [Figure 6](#) and [Figure 7](#)) it is not necessary to keep the recommended power up sequence.

## 4.4 Operating Range

**Table 8 Operating Range**

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Battery voltage L <sup>1)</sup>	$V_{BATL}$	-80	-15	V	Referred to BGND
Battery voltage H <sup>1)</sup>	$V_{BATH}$	-85	-20	V	Referred to BGND
Auxiliary supply voltage	$V_{HR}$	5	85	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	-	150	V	-
$V_{DD}$ supply voltage	$V_{DD}$	4.75	5.25	V	Referred to AGND
Ground voltage difference BGND, AGND	-	-0.4	0.4	V	-
Voltage at pins IT, IL	$V_{IT}, V_{IL}$	-0.4	3.5	V	Referred to AGND
Input range $V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}$	$V_{ACDC}$	0	3.3	V	Referred to AGND
Ambient temperature	$T_{amb}$	-40	85	°C	-
Junction temperature	$T_J$	-	125 <sup>2)</sup>	°C	-

<sup>1)</sup> If the battery switch is not used, pins  $V_{BATL}$  and  $V_{BATH}$  should be connected externally. In this case the full voltage range of -15 V to -85 V can be used.

<sup>2)</sup> Operation up to  $T_J = 150$  °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

## 4.5 Thermal Resistances

**Table 9 Thermal Resistances**

Parameter	Symbol	Typical Value	Unit	Condition
Junction to case	$R_{th, jC}$	2	K/W	P-DSO-20-5, P-VQFN-48-4
Junction to ambient	$R_{th, jA}$	50	K/W	P-DSO-20-5, without additional heatsink
		20	K/W	P-DSO-20-5, with heatsink
Junction to ambient	$R_{th, jA}$	25	K/W	P-VQFN-48-4, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see <a href="#">Chapter 6.1</a> )

## 4.6 Electrical Parameters

Minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at  $V_{BATH} = -48\text{ V}$ ,  $V_{BATL} = -24\text{ V}$ ,  $V_{HR} = +32\text{ V}$  and  $V_{DD} = +5\text{ V}$ .

Functionality and performance is guaranteed for  $T_A = 0\text{ to }70\text{ °C}$  by production testing. Extended temperature range operation at  $-40\text{ °C} < T_A < 85\text{ °C}$  is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

### 4.6.1 Supply Currents and Power Dissipation

**Table 10** Supply Currents, Power Dissipation ( $I_R = I_T = 0\text{ A}$ ;  $V_{RT} = 0\text{ V}$ )

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	

#### Power Down High Impedance, Power Down Resistive High

1.	$V_{DD}$ current	$I_{DD}$	PDx	–	120	200	$\mu\text{A}$
2.	$V_{BATH}$ current	$I_{BATH}$	PDx	–	80	120	$\mu\text{A}$
3.	$V_{BATL}$ current	$I_{BATL}$	PDx	–	0	10	$\mu\text{A}$
4.	$V_{HR}$ current	$I_{HR}$	PDx	–	0	10	$\mu\text{A}$

#### Active Low

5.	$V_{DD}$ current	$I_{DD}$	ACTL	–	0.9	1.2	$\text{mA}$
6.	$V_{BATH}$ current	$I_{BATH}$	ACTL	–	20	40	$\mu\text{A}$
7.	$V_{BATL}$ current <sup>1)</sup>	$I_{BATL}$	ACTL	–	2.5	3.3	$\text{mA}$
8.	$V_{HR}$ current	$I_{HR}$	ACTL	–	0	10	$\mu\text{A}$

#### Active High

9.	$V_{DD}$ current	$I_{DD}$	ACTH	–	1	1.3	$\text{mA}$
10.	$V_{BATH}$ current <sup>1)</sup>	$I_{BATH}$	ACTH	–	3	4	$\text{mA}$
11.	$V_{BATL}$ current	$I_{BATL}$	ACTH	–	0	10	$\mu\text{A}$
12.	$V_{HR}$ current	$I_{HR}$	ACTH	–	0	10	$\mu\text{A}$

**Electrical Characteristics**
**Table 10 Supply Currents, Power Dissipation ( $I_R = I_T = 0$  A;  $V_{RT} = 0$  V) (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	

**Active Ring**

13.	$V_{DD}$ current	$I_{DD}$	ACTR	–	0.5	0.7	mA
14.	$V_{BATH}$ current <sup>1)</sup>	$I_{BATH}$	ACTR	–	2.8	3.7	mA
15.	$V_{BATL}$ current	$I_{BATL}$	ACTR	–	0	10	$\mu$ A
16.	$V_{HR}$ current <sup>1)</sup>	$I_{HR}$	ACTR	–	2.1	2.8	mA

**High Impedance on RING, High Impedance on TIP**

17.	$V_{DD}$ current	$I_{DD}$	HIR, HIT	–	0.5	0.7	mA
18.	$V_{BATH}$ current <sup>1)</sup>	$I_{BATH}$	HIR, HIT	–	1.9	2.5	mA
19.	$V_{BATL}$ current	$I_{BATL}$	HIR, HIT	–	0	10	$\mu$ A
20.	$V_{HR}$ current <sup>1)</sup>	$I_{HR}$	HIR, HIT	–	1.3	1.8	mA

**High Impedance on RING and TIP**

21.	$V_{DD}$ current	$I_{DD}$	HIRT	–	0.5	0.7	mA
22.	$V_{BATH}$ current <sup>1)</sup>	$I_{BATH}$	HIRT	–	1	1.4	mA
23.	$V_{BATL}$ current	$I_{BATL}$	HIRT	–	0	10	$\mu$ A
24.	$V_{HR}$ current <sup>1)</sup>	$I_{HR}$	HIRT	–	0.5	0.8	mA

<sup>1)</sup> Current depending on supply voltage (see [Table 11](#))

The total power dissipated in the SLIC consists of the quiescent power  $P_Q$  due to the supply currents and the output stage power  $P_O$  caused by any line current  $I_{TRANS}$  (see [Table 12](#)).

$$P_{tot} = P_Q + P_O$$

$$\text{with } P_Q = V_{DD} \times I_{DD} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL} + V_{HR} \times I_{HR}$$

The supply currents  $I_{BATL}$ ,  $I_{BATH}$  and  $I_{HR}$  are dependent on the respective supply voltages. They can be calculated from the specified values  $I_{BATL}$  (-24 V),  $I_{BATH}$  (-48 V) and  $I_{HR}$  (32 V) by the formulas in [Table 11](#).

**Table 11 Voltage Dependence of Supply Currents**

Operating Mode	Equation for $I$ Calculation
ACTL	$I_{\text{BATL}}(V_{\text{BATL}}) = I_{\text{BATL}}(-24\text{V}) + ( V_{\text{BATL}}  - 24)/50 \text{ k}\Omega$
ACTH	$I_{\text{BATH}}(V_{\text{BATH}}) = I_{\text{BATH}}(-48\text{V}) + ( V_{\text{BATH}}  - 48)/50 \text{ k}\Omega$
ACTR <sup>1)</sup>	$I_{\text{BATH}}(V_{\text{BATH}}) = I_{\text{BATH}}(-48\text{V}) + ( V_{\text{BATH}}  - 48)/50 \text{ k}\Omega$ $I_{\text{HR}}(V_{\text{HR}}) = I_{\text{HR}}(32\text{V}) + (V_{\text{HR}} - 32)/200 \text{ k}\Omega$

<sup>1)</sup> valid for  $|V_{\text{BATH}}| > V_{\text{HR}}$

**Table 12 Output Stage Power Dissipation**

Operating Mode	Equation for $P_{\text{O}}$ Calculation
ACTL	$P_{\text{O}} = (1.05 \times  V_{\text{BATL}}  - V_{\text{TR}}) \times I_{\text{Trans}}$
ACTH	$P_{\text{O}} = (1.05 \times  V_{\text{BATH}}  - V_{\text{TR}}) \times I_{\text{Trans}}$
ACTR	$P_{\text{O}} = (1.02 \times V_{\text{HR}} + 1.05 \times  V_{\text{BATH}}  - V_{\text{TR}}) \times I_{\text{Trans}}$ (ohmic load) $P_{\text{O}} = [4 \times (V_{\text{H}} +  V_{\text{BATH}} ) - \pi \times V_{\text{P}} \times \cos \varphi] \times V_{\text{P}} / (2 \times \pi \times Z_{\text{L}})$ (complex load $Z = Z_{\text{L}}e^{i\varphi}$ , $V_{\text{P}}$ ... peak ring voltage)

**4.6.2 DC Characteristics**
**Table 13 DC Characteristics**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
25.	DC line voltage	$V_{TR, DC}$	ACTL, ACTH, ACTR	-0.4	0	0.4	V	$V_{DCP} = V_{DCN} = V_{ACP} =$ $V_{ACN} = 1.5 V$
26.		$V_{TIP, DC}$	ACTL	-13	-12	-11	V	
27.			ACTH	-25	-24	-23	V	
28.			ACTR	-10.5	-9.5	-8.5	V	
29.		$V_{TR, DC}$	ACTH	23.5	24	24.5	V	$V_{DCP} - V_{DCN} = 0.8 V,$ $V_{ACP} = V_{ACN} = 1.5 V$
30.				-24.5	-24	-23.5	V	$V_{DCP} - V_{DCN} = -0.8 V,$ $V_{ACP} = V_{ACN} = 1.5 V$
31.	DC line voltage drop (see <a href="#">Figure 8</a> )	$-V_{BATH}$ $-V_{TR, max}$	ACTH	-	2	3	V	$I_{Trans, DC} = 20 mA,$ $V_{DCP} - V_{DCN} = 2.5 V,$ $V_{ACP} = V_{ACN} = 1.5 V$
32.	Output current limit (see <a href="#">Figure 12</a> )	$ I_{R, max} ,$ $ I_{T, max} $	ACTL, ACTH, ACTR, HIR HIT	80		130	mA	
33.	Open loop resistance TIP to $V_{BGND}$ (see <a href="#">Figure 13</a> )	$R_{TG}$	PDRH	4.25	5.0	5.75	k $\Omega$	$I_T = 2 mA,$ Temp = 25 °C <sup>1)</sup>
34.	Open loop resistance RING to $V_{BATH}$ (see <a href="#">Figure 13</a> )	$R_{RB}$	PDRH	4.25	5.0	5.75	k $\Omega$	$I_R = 2 mA,$ Temp = 25 °C <sup>1)</sup>
35.	Open loop line voltage	$V_{TR}$	PDRH		45		V	
36.	Power down	$I_{Leak, R}$	PDH	-30		30	$\mu A$	$V_{BATH} < V_R < V_{HR}$
37.	output leakage current	$I_{Leak, T}$		-30		30	$\mu A$	$V_{BATH} < V_T < V_{HR}$

**Electrical Characteristics**
**Table 13 DC Characteristics (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
38.	High impedance	$I_{Leak,R}$	HIR, HIRT	-30		30	$\mu A$	$V_{BATH} < V_R < V_{HR} - 3$
39.	output leakage current	$I_{Leak,T}$	HIT, HIRT	-30		30	$\mu A$	$V_{BATH} < V_T < V_{HR} - 3$

**Inputs DCP, DCN, ACP, ACN, Output C<sub>EXT</sub>**

40.	Input resistance DCP, DCN	$R_{DC}$	ACTR, HIR, HIT	-	1	-	$k\Omega$	
41.			ACTL, ACTH	-	2	-	$k\Omega$	
42.	Input resistance ACP, ACN	$R_{AC}$	all	-	10	-	$k\Omega$	
43.	Output resistance on C <sub>EXT</sub>		all	-	50	-	$k\Omega$	

**Current Outputs I<sub>T</sub>, I<sub>L</sub>**

44.	IT output current (see <a href="#">Figure 14</a> )	$I_{IT}$	ACTx	-15	0	15	$\mu A$	$I_R = I_T = 0 \text{ mA}$
45.				380	400	420	$\mu A$	$I_R = I_T = 20 \text{ mA}$
46.				-420	-400	-380	$\mu A$	$I_R = I_T = -20 \text{ mA}$
47.	Transversal current ratio (guaranteed by design, see <a href="#">Figure 14</a> )	$I/G_{IT,DC}^{2)}$	ACTx	49.5	50	50.5	-	$I_R = I_T = 20 \text{ mA}$ , $I_R = I_T = -20 \text{ mA}$
48.	Off-hook output current on IT		PDRH	750	900	1050	$\mu A$	TIP/RING shorted Temp = 25 °C <sup>3)</sup>
49.	IL output current (see <a href="#">Figure 14</a> )	$I_{IL}$	ACTx	-20	0	20	$\mu A$	$I_R = I_T = 20 \text{ mA}$
50.				30	50	70	$\mu A$	$I_R = 15 \text{ mA}$ , $I_T = 25 \text{ mA}$
51.				-160	-125	-90	$\mu A$	$I_R = 62.5 \text{ mA}$ , $I_T = 37.5 \text{ mA}$

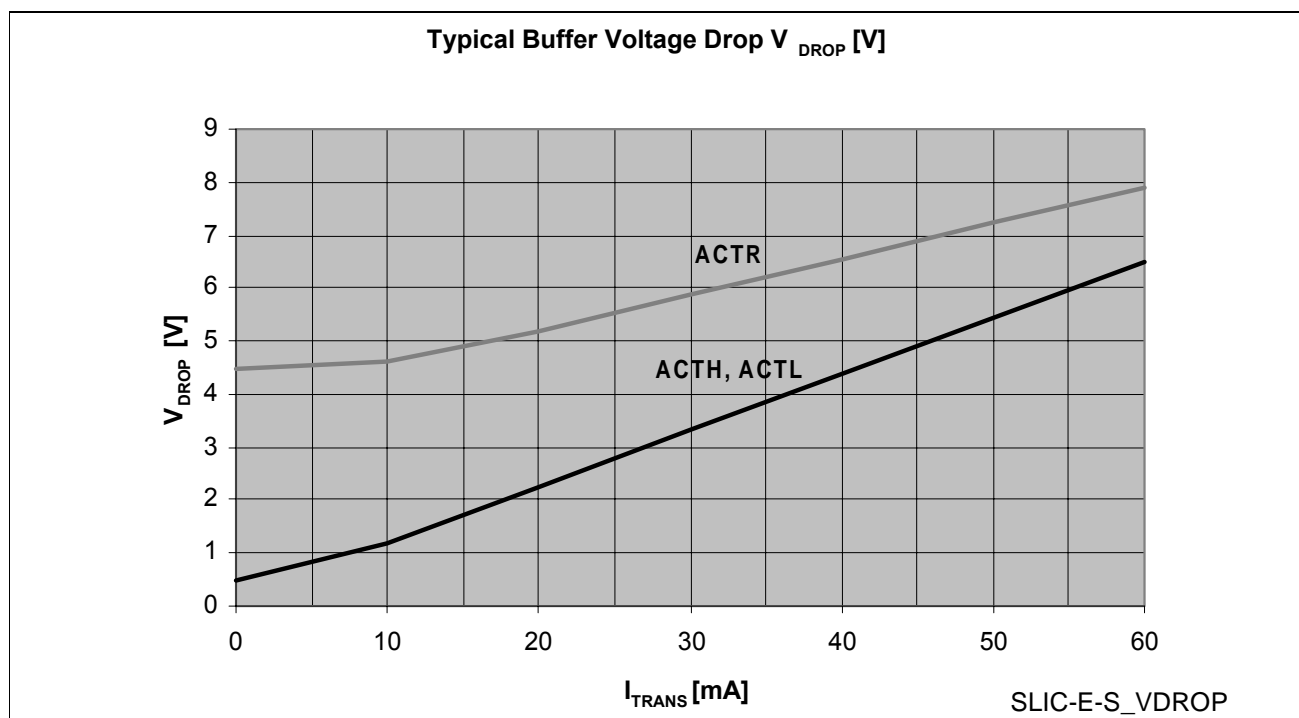
**Table 13 DC Characteristics (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		

**Control Inputs C1, C2, C3**

52.	H-input voltage	$V_{IH}$	–	2.7		$V_{DD} + 0.3$	V	–
53.	M-input voltage	$V_{IM}$	–	1.2		2.1	V	only C1, C2
54.	L-input voltage	$V_{IL}$	–	–0.3		0.6	V	–
55. 56.	Input leakage current	$I_{Leak}$	–	–5 0	0 5	5 10	$\mu A$	C1, C2 C3
57.	Thermal overload current C1	$I_{therm}$	ACTx, Hlx	120	150	250	$\mu A$	$V_{C1} = 1.20 V$
58.	Max. junction temperature <sup>4)</sup>	$T_{jLIM}$	ACTx, Hlx	–	165	–	$^{\circ}C$	–

- 1) The systematic temperature dependency of this resistance is  $+0.1 \%/^{\circ}C$ .
- 2) The offset ( $I_R = I_T = 0 mA$ ) has to be taken into account.
- 3) The systematic temperature dependency of this current is  $-0.1 \%/^{\circ}C$ .
- 4) Overtemperature protection (guaranteed by design)



**Figure 8 Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR**

### 4.6.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

**Table 14 AC Characteristics**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		

#### Line Termination TIP, RING

59.	Receive gain (see <a href="#">Figure 15</a> )	$G_r$		5.925	6.0	6.075	–	$V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$
60.	Total harmonic distortion $V_{TR}$ (see <a href="#">Figure 15</a> )	$THD$		–	0.03	0.3	%	$V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$
61.	Teletax distortion	$THD_{TTX}$		–	0.1	1	%	$V_{TR,AC} = 5 \text{ Vrms}$ $f = 16 \text{ kHz}, R_L = 200 \Omega$
62.				–	1	3	%	$V_{TR,AC} = 5 \text{ Vrms}$ $f = 16 \text{ kHz}, R_L = 200 \Omega,$ $I_{Trans,DC} = 0 \text{ mA}$
63.	Psophometric noise (see <a href="#">Figure 15</a> )	$N_{pVTR}$		–	–80	–76	dBmp	
64.	Longitudinal to transversal rejection ratio $V_{long}/V_{TR}$ (see <a href="#">Figure 16</a> )	$LTRR$		60	70	–	dB	$V_{long} = 3 \text{ Vrms}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$
65.	Longitudinal to transversal rejection ratio $V_{long}/V_{TR}$ (loop) (see <a href="#">Figure 16</a> )	$LTRR-1$ $loop^1$		54	58	–	dB	$V_{long} = 3 \text{ Vrms}$ $300 \text{ Hz} < f < 1 \text{ kHz}$
66.				52	56	–	dB	3.4 kHz
67.		$LTRR-2$ $loop^2$		61	65	–	dB	$300 \text{ Hz} < f < 1 \text{ kHz}$
68.				56	60	–	dB	3.4 kHz
69.	Transversal to longitudinal rejection ratio $V_{TR}/V_{long}$ (see <a href="#">Figure 18</a> )	$TLRR$		48	58	–	dB	$V_{ACP} - V_{ACN} = 1920 \text{ mVrms}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$

**Electrical Characteristics**
**Table 14 AC Characteristics (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
70.	Power supply rejection ratio $V_{BATL}/V_{TR}$	$PSRR$		40	60		dB	$V_{SupplyAC} = 100 \text{ mVp}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$  modes ACTL, ACTH
71.	$V_{BATH}/V_{TR}$			40	60			
72.	$V_{HR}/V_{TR}$			33	50			
73.	$V_{DD}/V_{TR}$ (see <a href="#">Figure 9</a> , <a href="#">10</a> , <a href="#">11</a> )			33	50			
74.	Ringing amplitude TIP/RING	$V_{RNG0}$	ACTR		85		Vrms	$V_{DCP} - V_{DCN} = 0.15 \text{ V}$ (DC) + 1.42 Vrms (sine wave),
75.	Ringing distortion (see <a href="#">Figure 19</a> )	$RD$		–	0.1	2	%	$R_R = 450 \Omega$ , $C_R = 3.4 \mu\text{F}$ , $f = 20 \text{ Hz}$

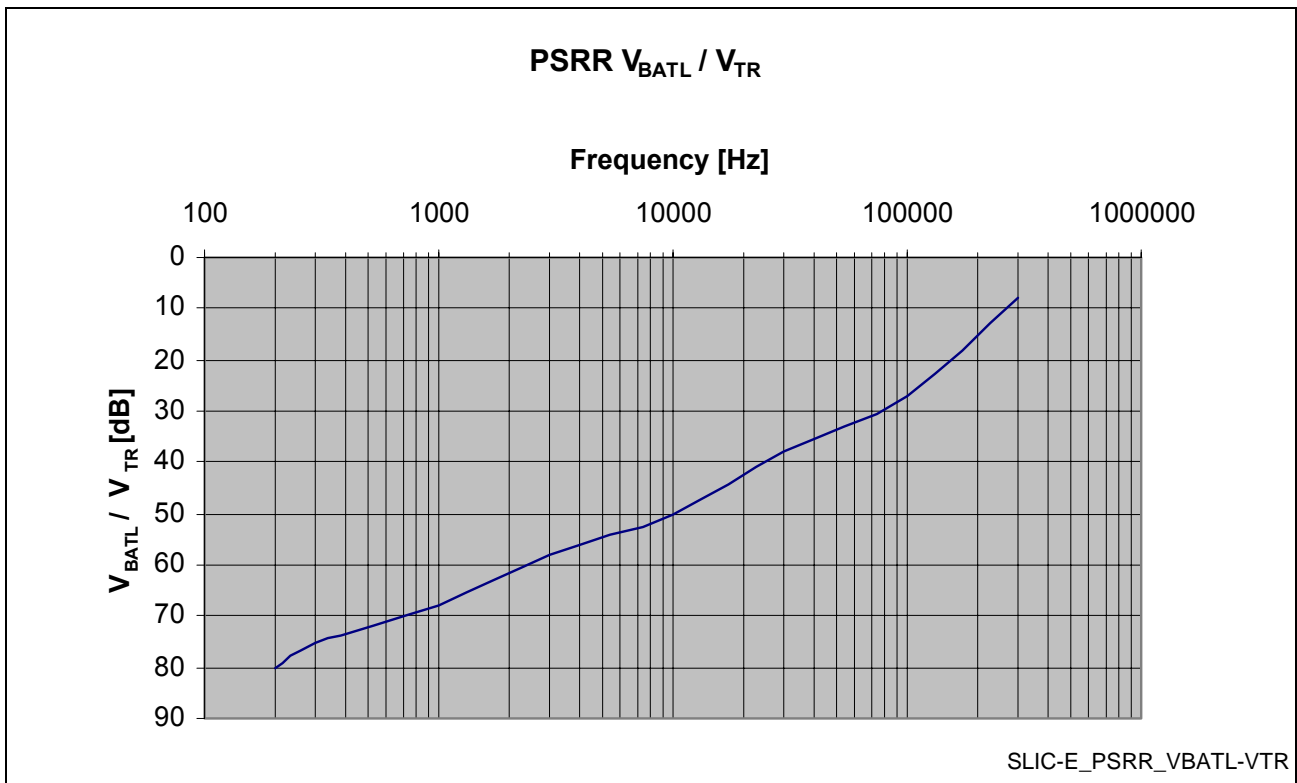
**Transversal Current  $I_T$** 

76.	Transversal current ratio (see <a href="#">Figure 15</a> )	$I/G_{it}$		49.5	50	50.5	–	$V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$ $I_{Trans,DC} = 25 \text{ mA}$ $I_{Trans,DC} = -25 \text{ mA}$	
77.				49	50	51			
78.	Total harmonic distortion $V_{IT}$	$THD_{IT}$		–	0.02	0.3	%	$I_{Trans,DC} = 25 \text{ mA}$ $V_{ACP} - V_{ACN} = 640 \text{ mVrms}$ $f = 1015 \text{ Hz}$	
79.	Psophometric noise (see <a href="#">Figure 15</a> )	$N_{pVIT}$		–	–110	–105	dBmp		
80.	Longitudinal to transversal current output rejection ratio $V_{long}/V_{IT}$ (see <a href="#">Figure 16</a> )	$LITRR$		78			dB	$V_{long} = 3 \text{ Vrms}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$	
81.	Power supply rejection ratio	$PSRR$		50	70	–	dB	$V_{SupplyAC} = 100 \text{ mVp}$ $300 \text{ Hz} < f < 3.4 \text{ kHz}$	
82.				$V_{BATL}/V_{IT}$	50	70			–
83.				$V_{BATH}/V_{IT}$	50	70			–
84.				$V_{HR}/V_{IT}$	50	70			–

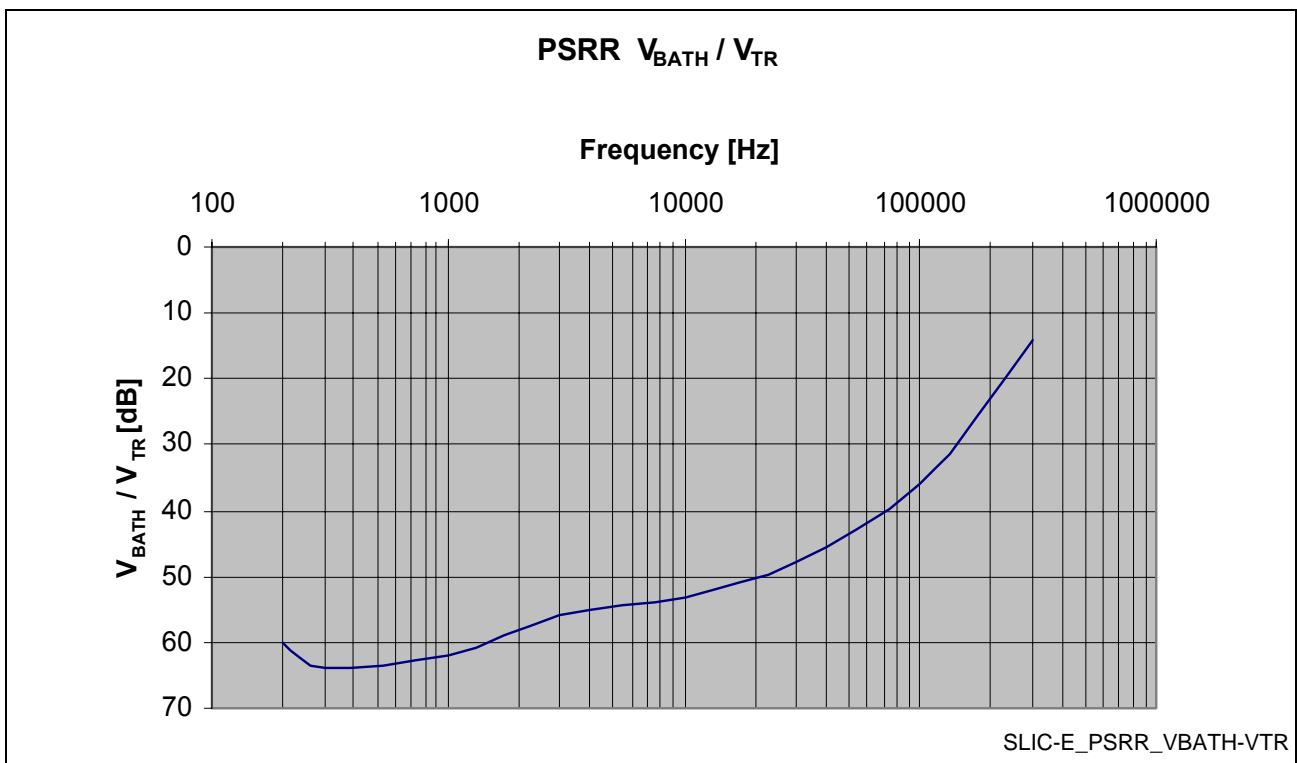
<sup>1)</sup> Longitudinal to transversal rejection ratio for PEB 4265

<sup>2)</sup> Longitudinal to transversal rejection ratio for PEB 4265-2

Electrical Characteristics



**Figure 9** Typical Frequency Dependence of PSRR VBATL/VTR



**Figure 10** Typical Frequency Dependence of PSRR VBATH/VTR

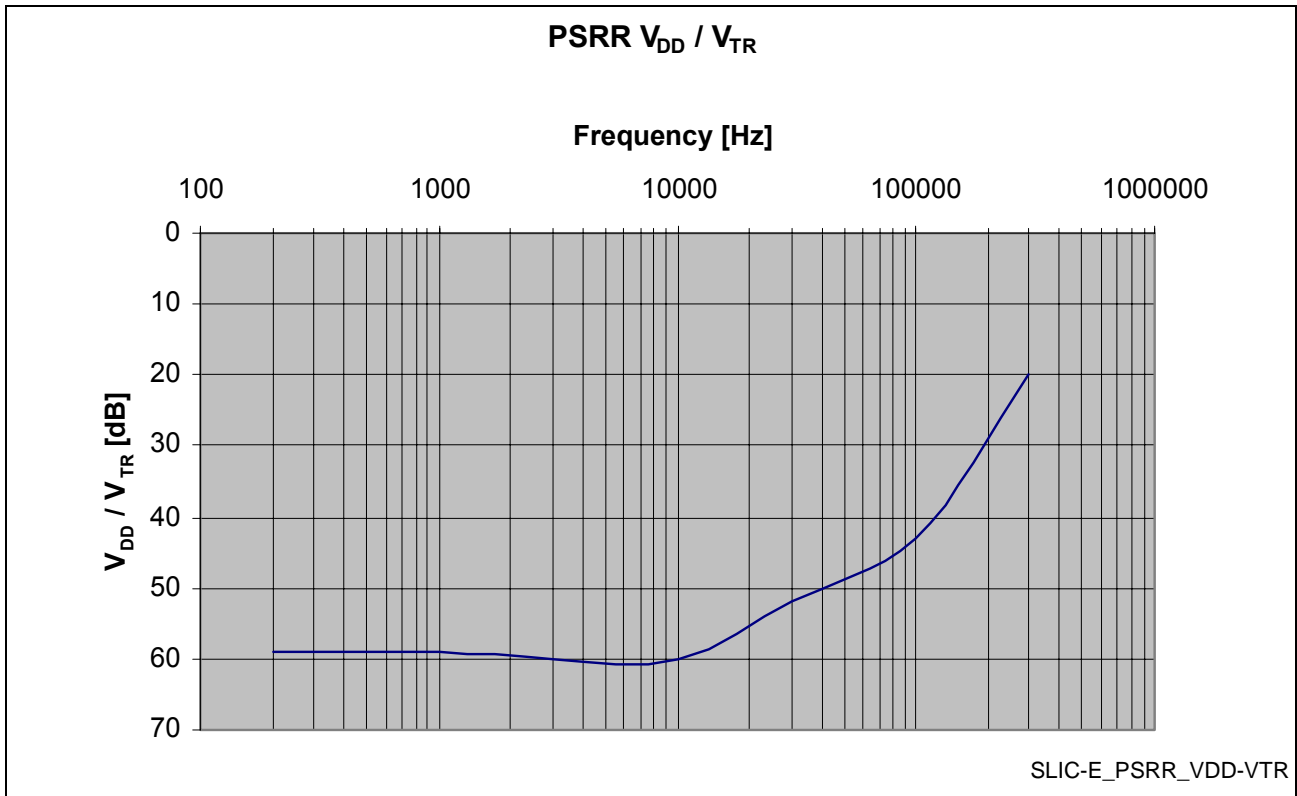


Figure 11 Typical Frequency Dependence of PSRR VDD/VTR

## 5 Test Figures

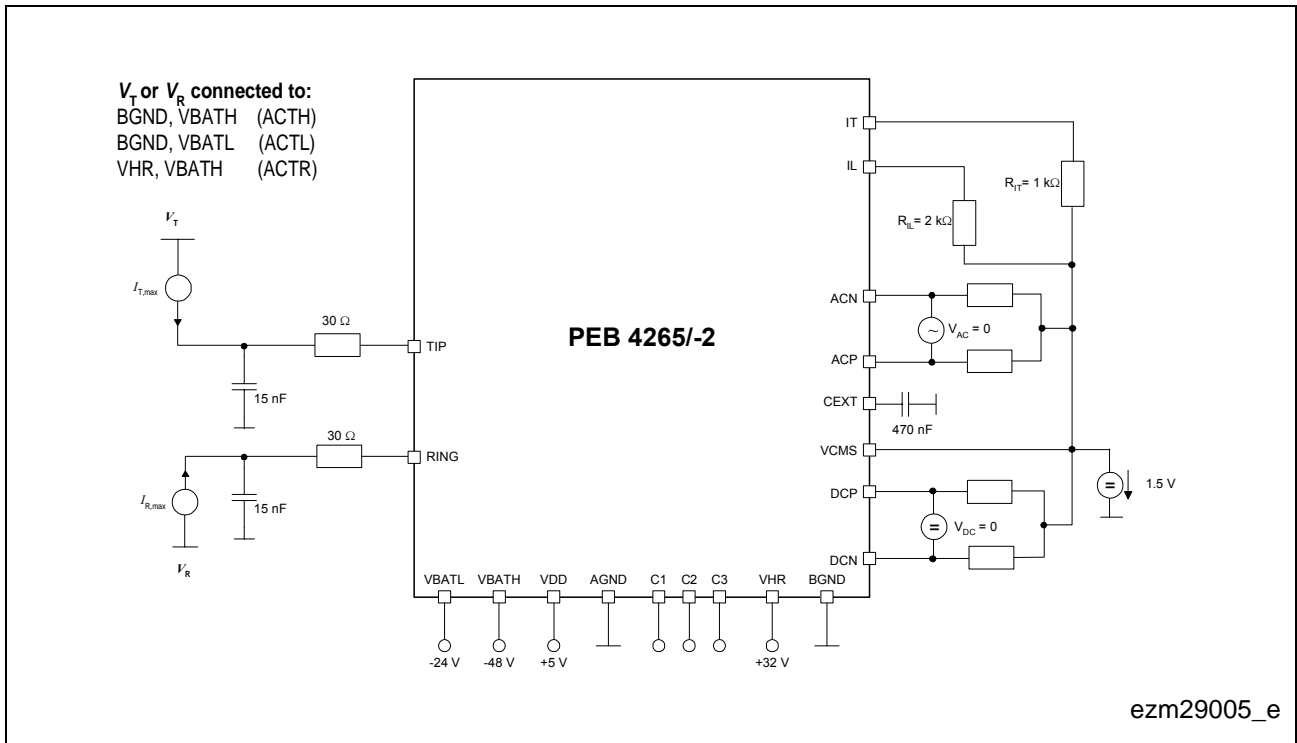


Figure 12 Output Current Limit

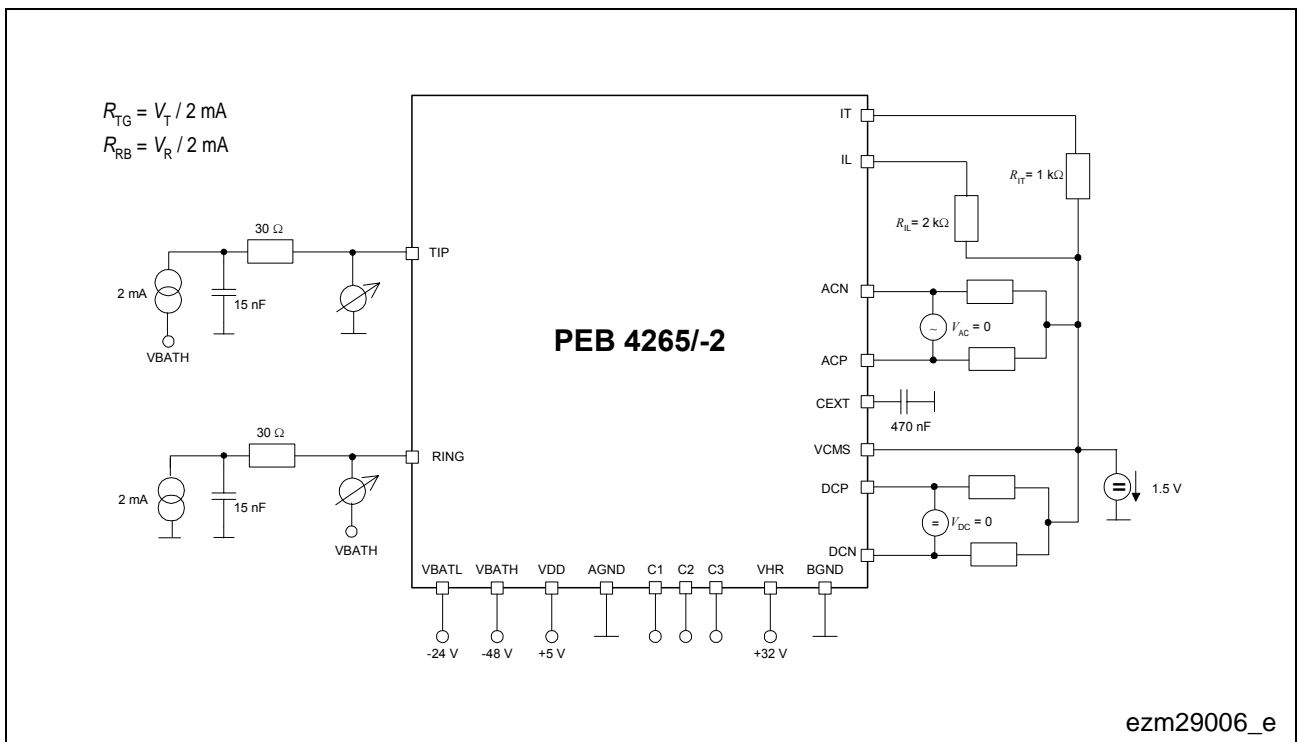
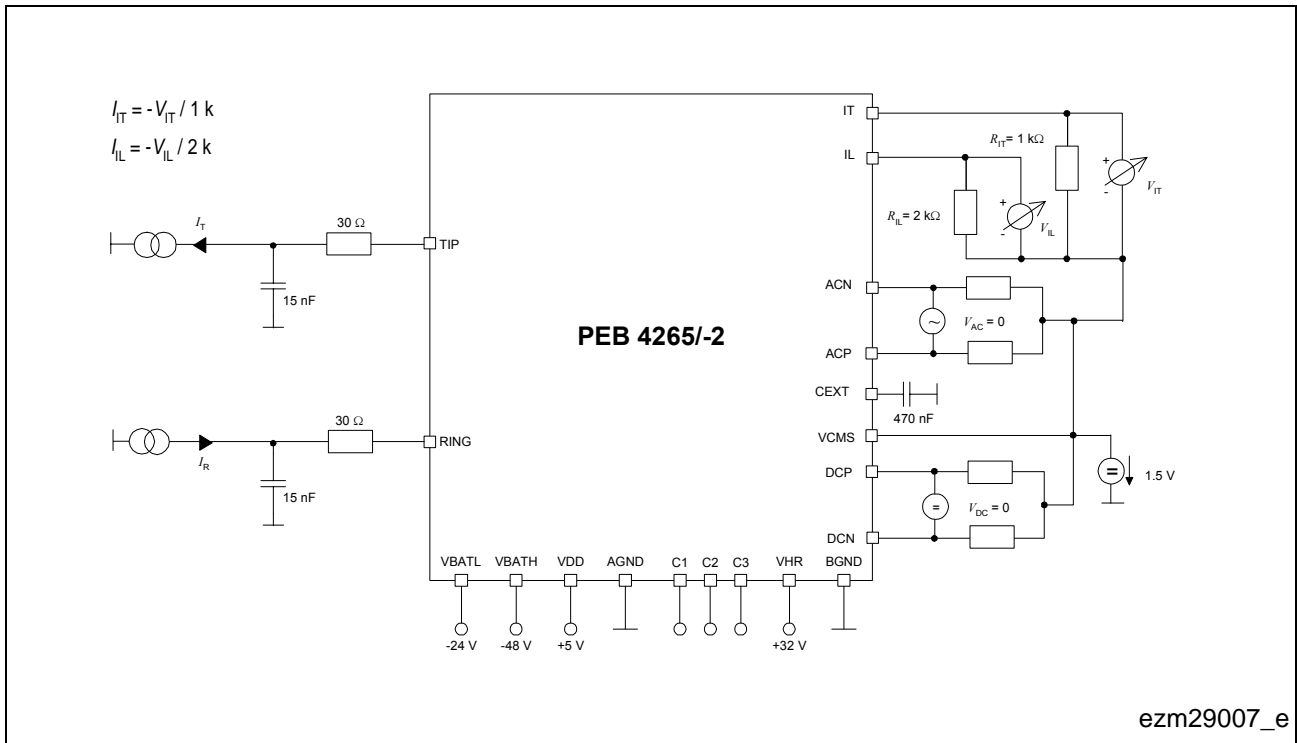
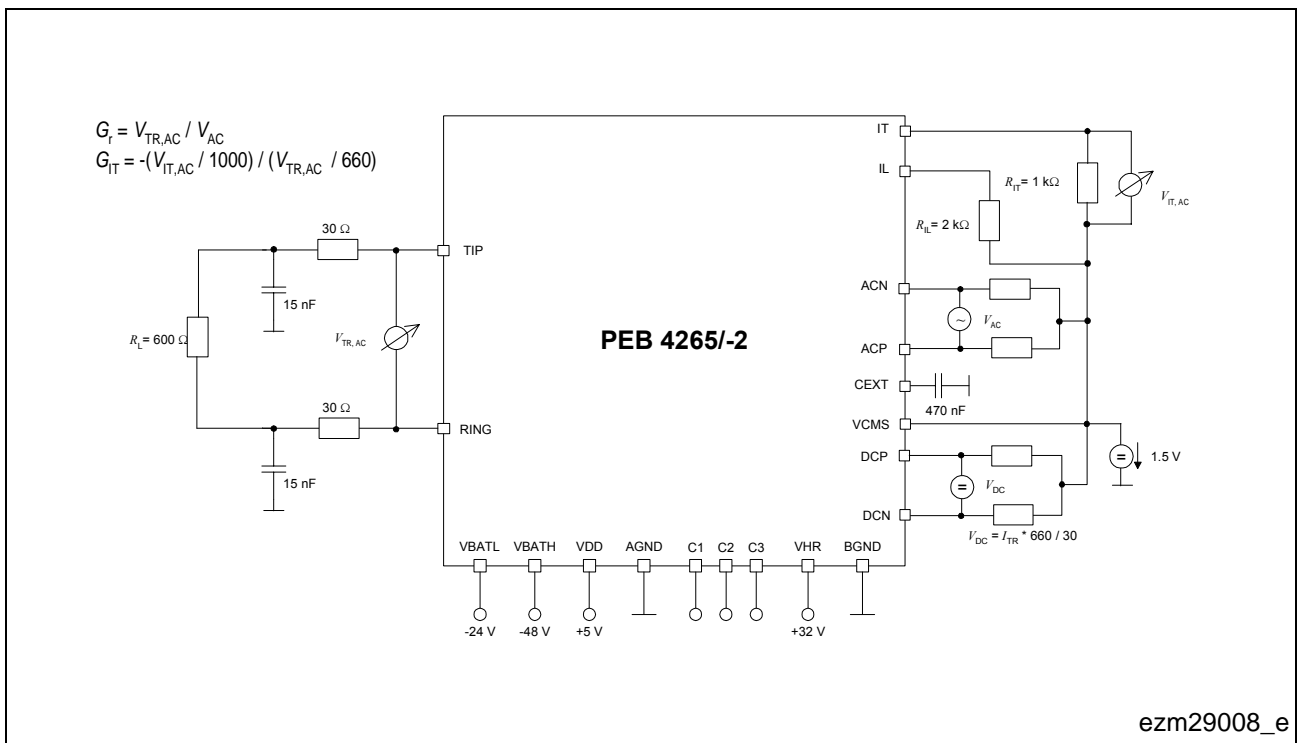


Figure 13 Output Resistance PDRH, PDRHL



**Figure 14** Current Outputs  $I_T$ ,  $I_L$



**Figure 15** Transmission Characteristics

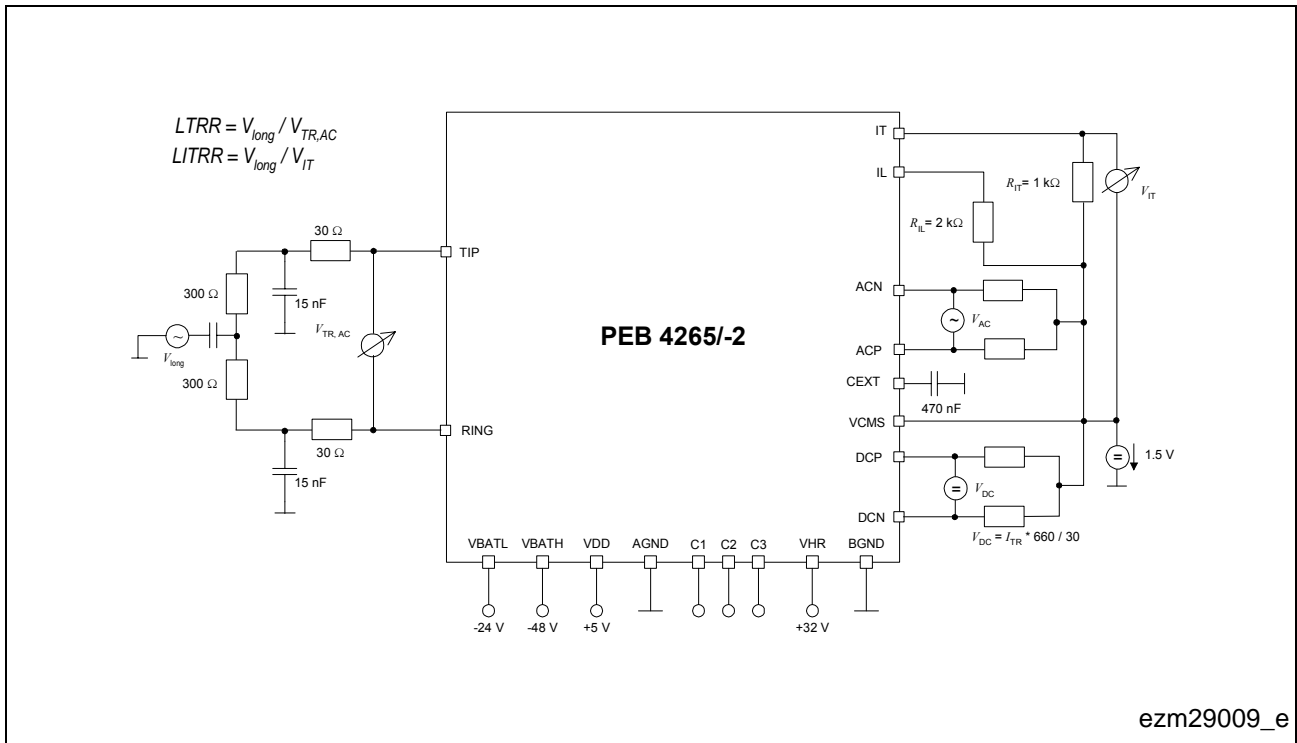


Figure 16 Longitudinal to Transversal Rejection

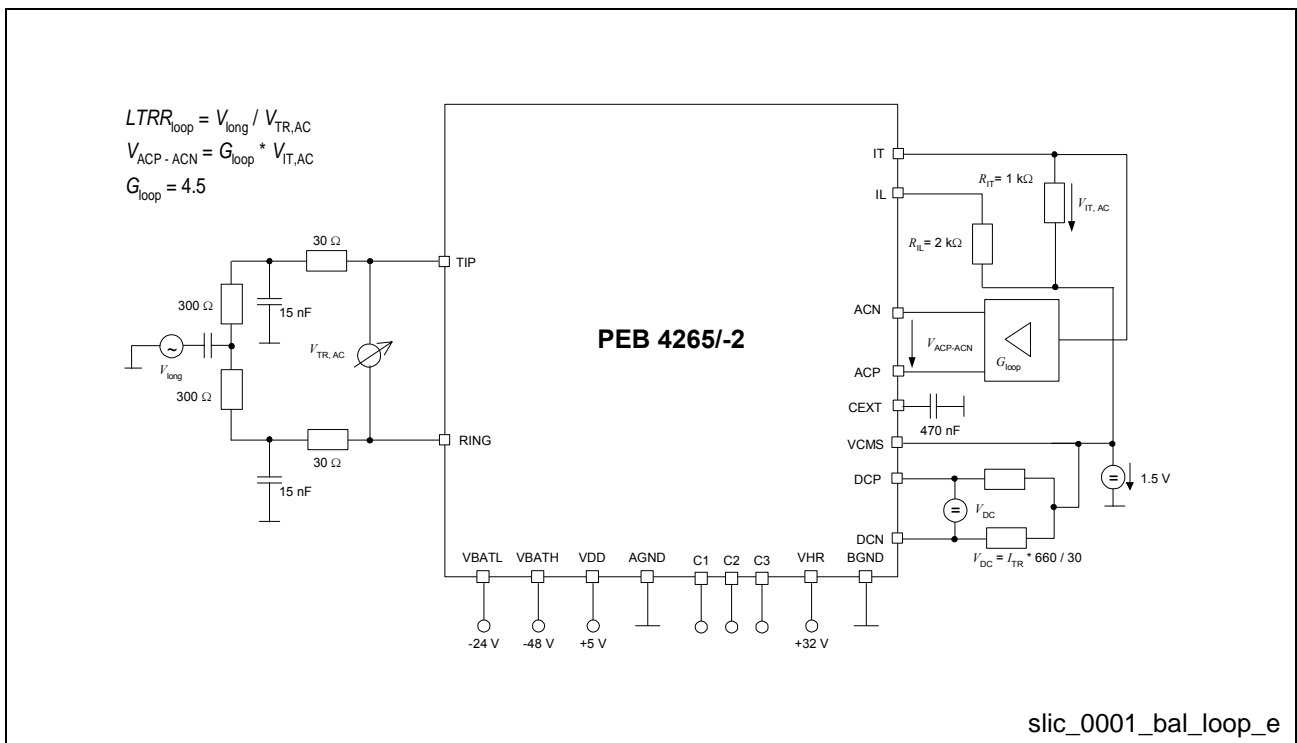


Figure 17 Longitudinal to Transversal Rejection Loop

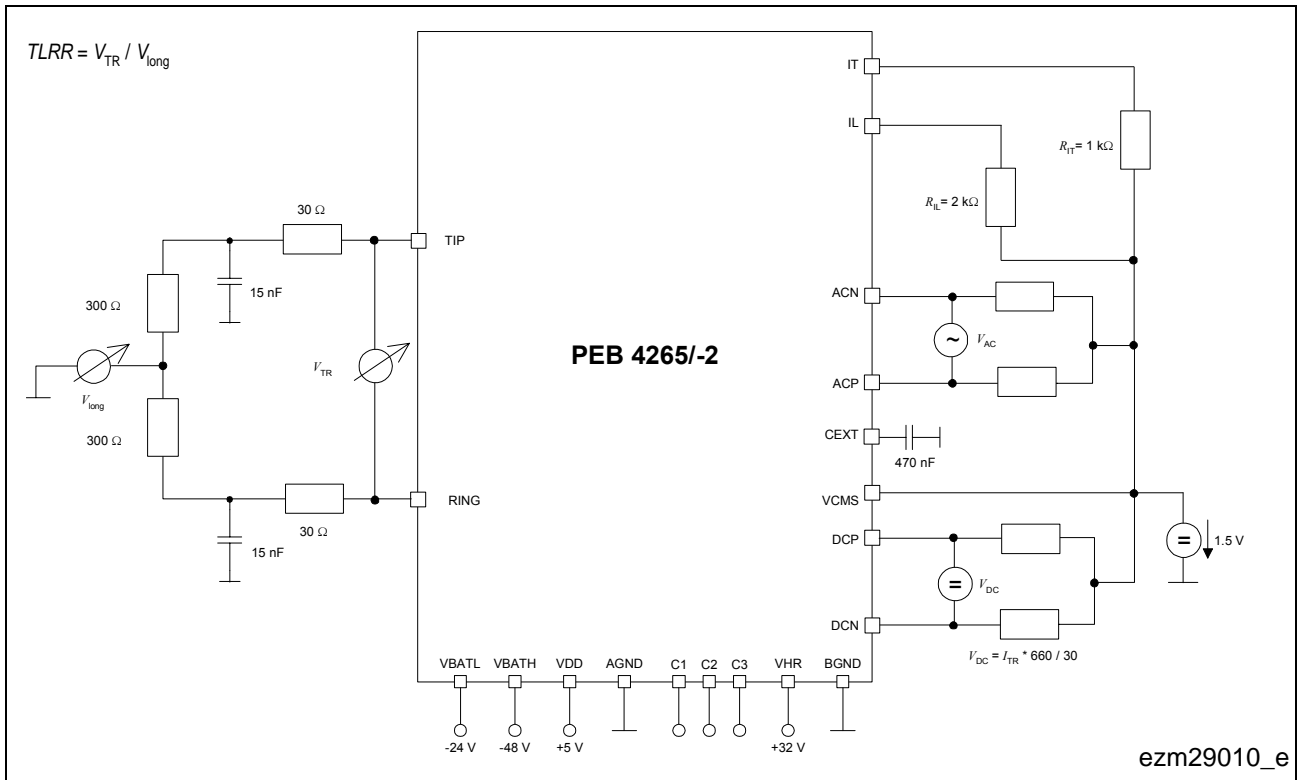


Figure 18 Transversal to Longitudinal Rejection

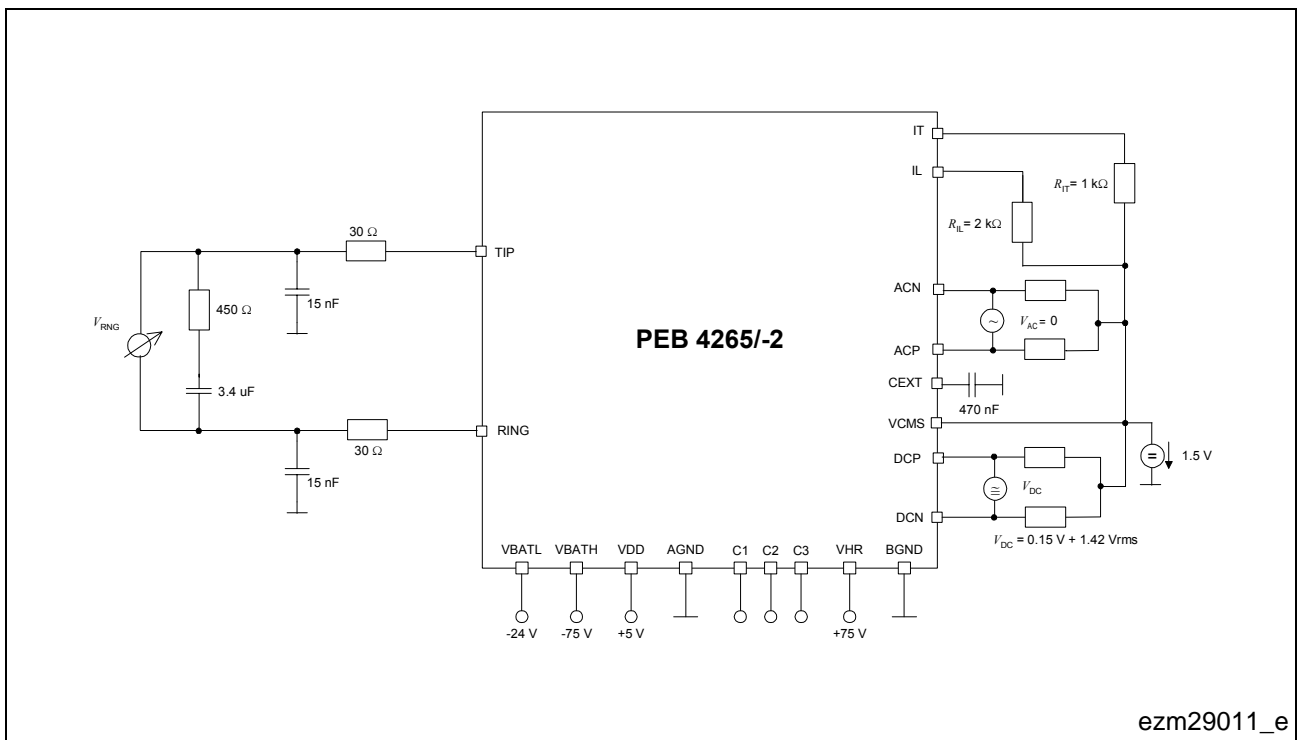
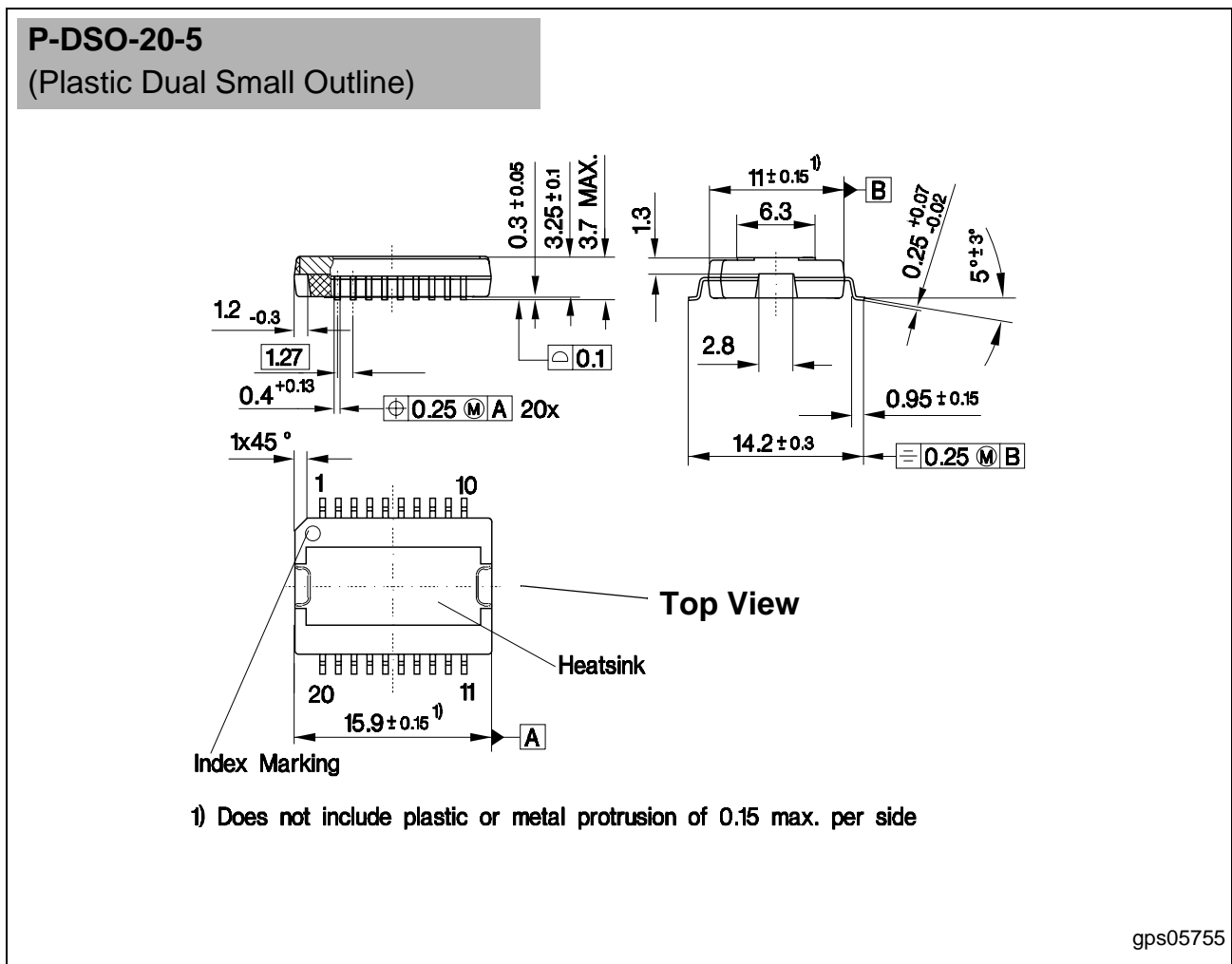


Figure 19 Ring Amplitude

## 6 Package Outlines



**Figure 20 Package Outline for P-DSO-20-5**

*Note: The P-DSO-20-5 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).*

**Attention: The heatsink (see Figure 20) is connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.**

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm



### 6.1 Recommended PCB Foot Print Pattern for the P-VQFN-48-4

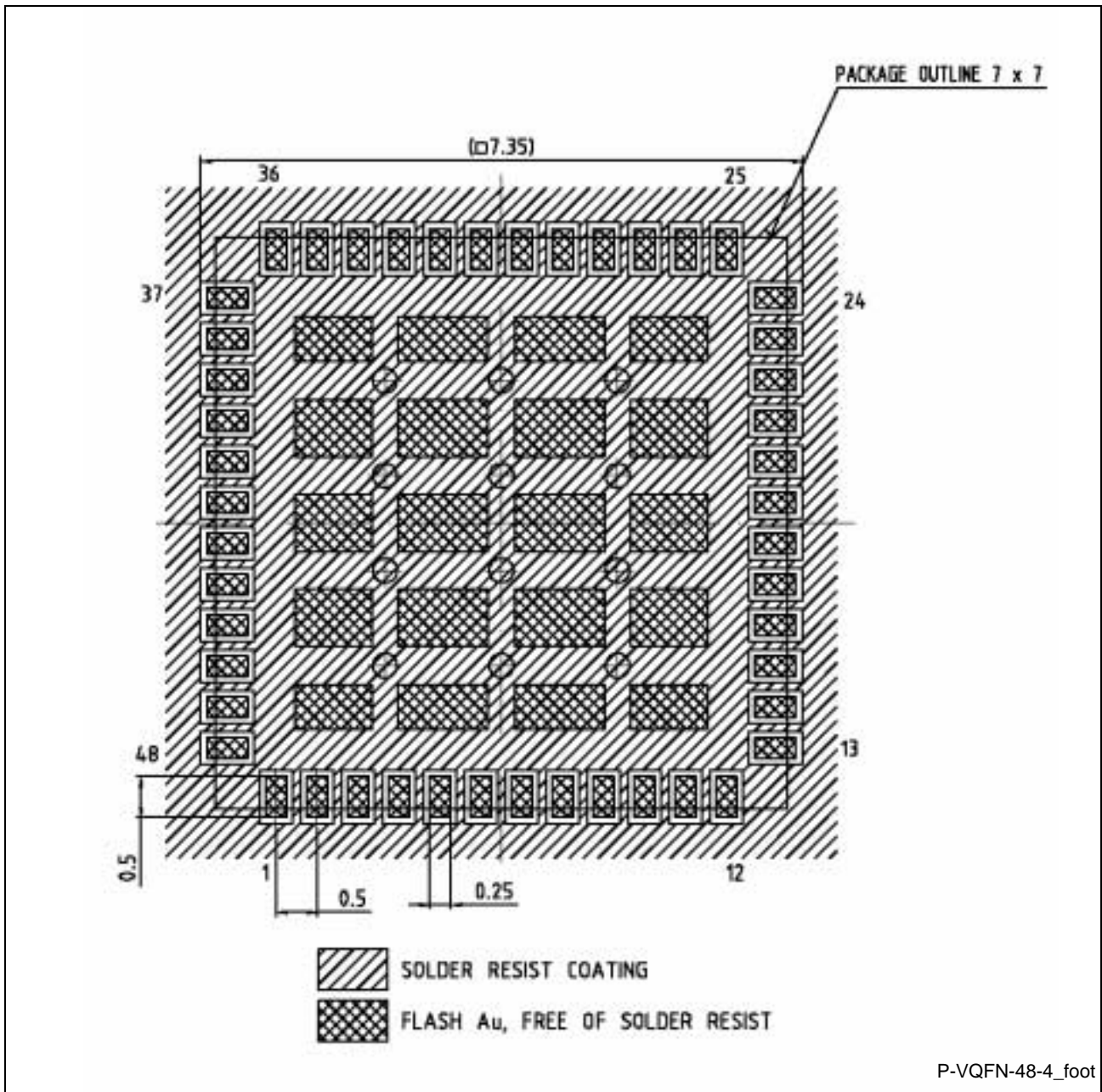


Figure 22 Foot Print for P-VQFN-48-4

<http://www.infineon.com>

Published by Infineon Technologies AG