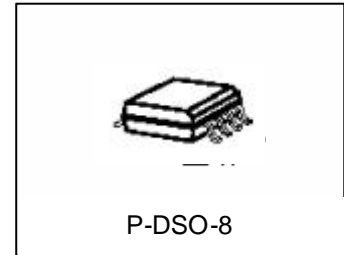


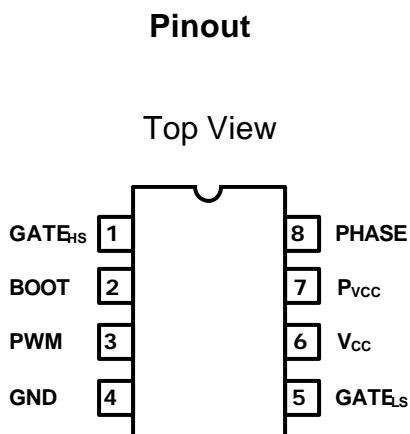
High speed Driver with bootstrapping for dual Power MOSFETs



Features

- Fast rise and fall times for frequencies up to 2 MHz
- Capable of sinking more than 4 A peak current for lowest switching losses
- Charges High Side MOSFET gate drive voltage to 6 ... 12V according to PVCC setting; Low Side MOSFET to 12 V.
- Adjustable High Side MOSFET gate drive voltage via PVCC pin for optimizing ON losses and gate drive losses.
- Integrates the bootstrap diode for reducing the part count
- Prevents from cross-conducting by adaptive gate drive control
- High voltage rating on Phase node
- Supports shut-down mode for very low quiescent current through three-state input
- Compatible to standard PWM controller ICs (Intersil, Analog Devices)
- Floating High Side MOSFET drive
- Footprint compatible to TDA21101G and HIP6601B
- Ideal for multi-phase Desktop CPU supplies on motherboards and VRM's

Type	Package	Marking	Ordering Code
TDA21106	P-DSO-8	21106	Q67042-S4223



Number	Name	Description
1	GATE _{HS}	Gate drive output for the N-Channel High side MOSFET
2	BOOT	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the high side N-Channel MOSFET
3	PWM	Input for the PWM controller signal
4	GND	Ground
5	GATE _{LS}	Gate drive output for the N-Channel Low Side MOSFET
6	VCC	Supply voltage
7	PVCC	Input to adjust the High Side gate drive
8	PHASE	To be connected to the junction of the High Side and the Low Side MOSFET

General Description

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from input to output, short rise and fall times and the same pin configuration to be compatible to TDA21101G and HIP6601B. In addition it provides several protection features as well as a shut down mode for efficiency reasons. The high breakdown voltage makes it suitable for mobile applications.

Target application

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver's capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM's but also in motor drive and class-D amplifier type applications.

Absolute Maximum Ratings

At $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value		Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin; DC	V_{VCC}	-0.3	25	V
Voltage supplied to 'PVCC' pin; DC	V_{PVCC}	-0.3	25	
Voltage supplied to 'PWM' pin	V_{PWM}	-0.3	5.5	
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	$V_{BOOT} - V_{PHASE}$	-0.3	25	
Voltage rating at 'PHASE' pin, DC	V_{PHASE}	-1	25	
Voltage rating at 'PHASE' pin, $t_{pulse_max} = 500\text{ns}$ Max Duty Cycle = 2%		-20	30	
Junction temperature	T_J	-25	150	$^\circ\text{C}$
Storage temperature	T_S	-55	150	
ESD Rating; Human Body Model			3	KV
IEC climatic category; DIN EN 60068-1			55/150/56	-

Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-soldering point			95		K/W
Thermal resistance, junction-ambient			125		

Electrical Characteristic

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply Characteristic						
Quiescent current	$I_{PVCCQ}+I_{VCCQ}$	$1.8\text{ V} \leq V_{PWM} \leq 3.0\text{ V}$		1.3	3	mA
VCC supply current	I_{VCC}	f = 1 MHz, $V_{PVCC} = V_{VCC} = 12\text{ V}$ No load		4.8		
PVCC supply current	I_{PVCC}	f = 1 MHz, $V_{PVCC} = V_{VCC} = 12\text{ V}$ No load		4.8		
Under-voltage lockout		V_{VCC} rising threshold	9.7	10.1	10.5	V
Under-voltage lockout		V_{VCC} falling threshold	7.3	7.6	8.0	
Input Characteristic						
Current in 'PWM' pin	$I_{PWM\ L}$	$V_{PWM} = 0.4\text{ V}$	-80	-115	-150	μA
Current in 'PWM' pin	$I_{PWM\ H}$	$V_{PWM} = 4.5\text{ V}$	120	180	250	
Shut down window	$V_{IN\ SHUT}$	$t_{SHUT} > 300\text{ ns}$	1.7		3.1	V
Shut down hold-off time	t_{SHUT}	$1.6\text{ V} \leq V_{PWM} \leq 3.2\text{ V}$	100	150	300	ns
PWM pin open	$V_{PWM\ O}$		1.8	2.0	2.2	V
PWM Low level	$V_{PWM\ L}$				1.4	
PWM High level	$V_{PWM\ H}$		3.7			
Pulse width High Side	t_P	= Pulse width on PWM pin	40			ns

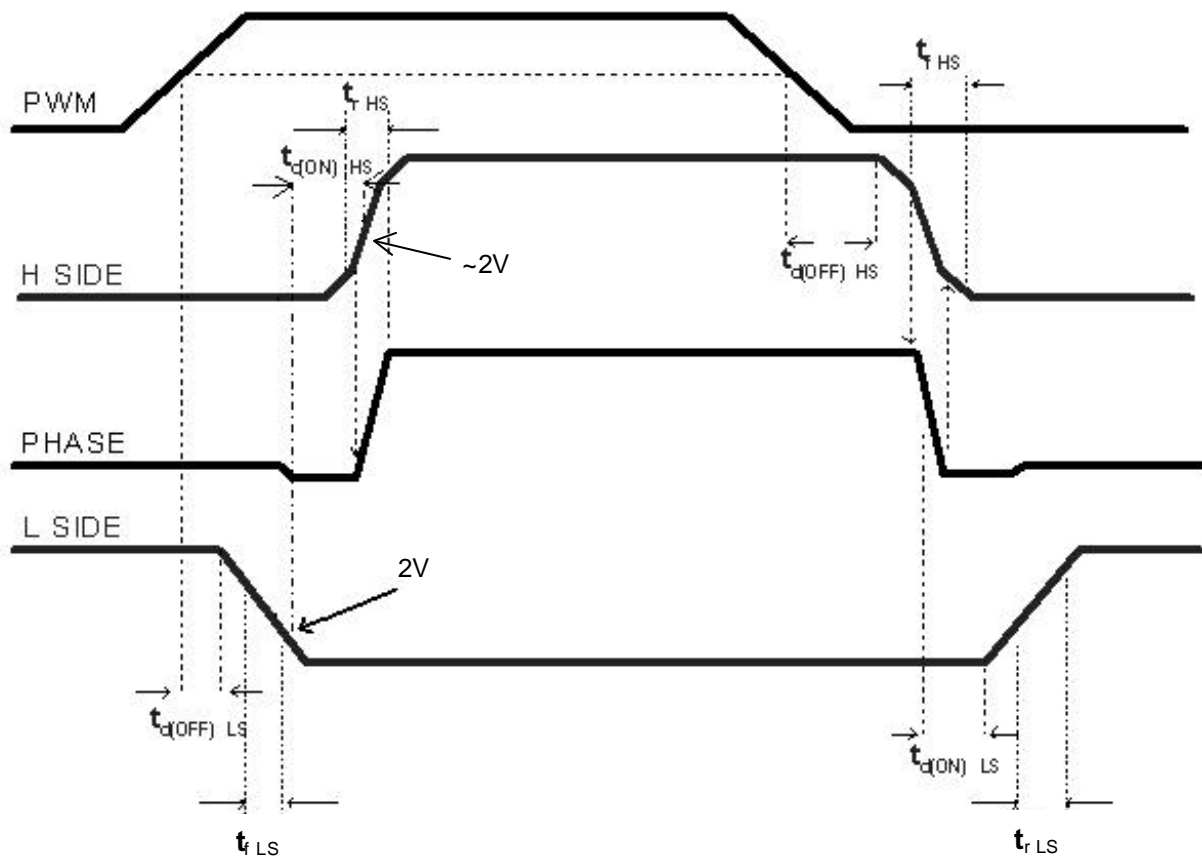
At Tj = 25 °C, unless otherwise specified

Dynamic Characteristic						
Turn-on propagation Delay High Side	$t_{d(ON)\ HS}$	$V_{PVCC} = V_{VCC} = 12\text{ V}$ $C_{ISS} = 3000\text{ pF}$		30	40	ns
Turn-off propagation delay High Side	$t_{d(OFF)\ HS}$			15	25	
Rise time High Side	$t_r\ HS$			20	33	
Fall time High Side	$t_f\ HS$			20	25	
Turn-on propagation Delay Low Side	$t_{d(ON)\ LS}$			20	30	
Turn-off propagation delay Low Side	$t_{d(OFF)\ LS}$			12	20	
Rise time Low Side	$t_r\ LS$			20	33	
Fall time Low Side	$t_f\ LS$			17	25	

At Tj = 125 °C, unless otherwise specified

Dynamic Characteristic					
Turn-on propagation Delay High Side	$t_{d(ON)_HS}$	$V_{PVCC} = V_{VCC} = 12\text{ V}$ $C_{ISS} = 3000\text{ pF}$		41	ns
Turn-off propagation delay High Side	$t_{d(OFF)_HS}$			20	
Rise time High Side	$t_r\ HS$			28	
Fall time High Side	$t_f\ HS$			22	
Turn-on propagation Delay Low Side	$t_{d(ON)_LS}$			30	
Turn-off propagation delay Low Side	$t_{d(OFF)_LS}$			18	
Rise time Low Side	$t_r\ LS$			28	
Fall time Low Side	$t_f\ LS$			20	

Timing diagram



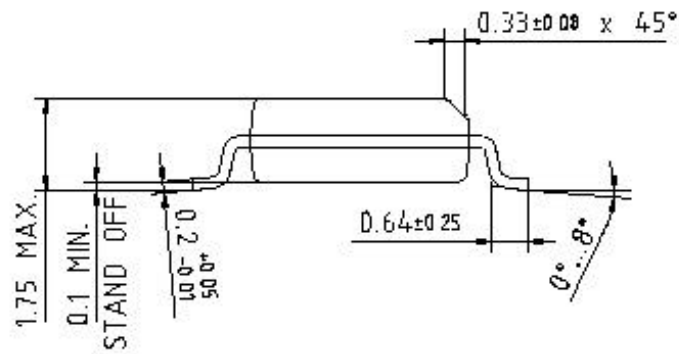
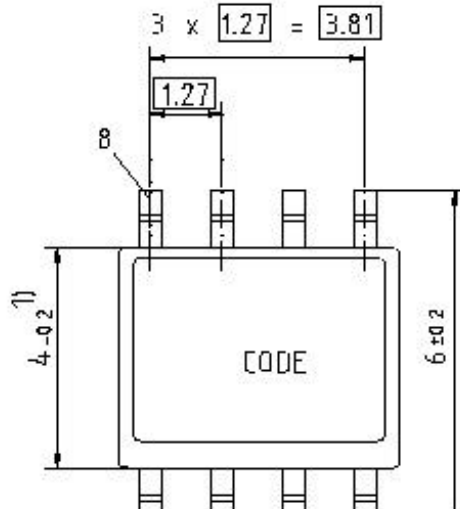
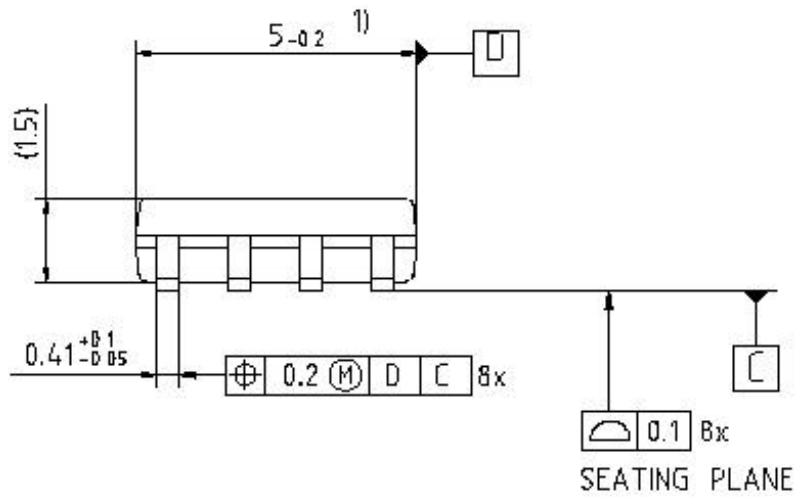
Operating ConditionsAt $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pins	V_{VCC}		10.8		13.2	V
Voltage supplied to 'PVCC' pins	V_{PVCC}		6		13.2	V
Input signal transition frequency	f		0.1		2	MHz
Power dissipation	P_{TOT}	$T_A = 25\text{ }^\circ\text{C}$, $T_J = 125\text{ }^\circ\text{C}$		0.8		W
Junction temperature	T_J		-25		150	$^\circ\text{C}$

At $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Conditions	Values			Unit	
		Min.	Typ.	Max.		
Output Characteristic High Side (HS) and Low Side (LS), ensured by design						
Output Resistance and Voltage drop resp.	HS; Source	$V_{PVCC} = V_{VCC} = 12\text{ V}$ $I_{HS_SRC} = 2\text{ A}$		1.0		Ω
	HS; Sink	$V_{PVCC} = V_{VCC} = 12\text{ V}$		1.0	1.5	
	LS; Source	$V_{PVCC} = V_{VCC} = 12\text{ V}$ $I_{HS_SRC} = 2\text{ A}$		1.4		
	LS; Sink	$V_{PVCC} = V_{VCC} = 12\text{ V}$		1	1.3	
Peak output-current	HS; Source	$V_{PVCC} = V_{VCC} = 12\text{ V}$	4			A
	HS; Sink	$t_{P_HS} / \text{Pulse} < 20\text{ ns}$	4			
	LS; Source	$t_{P_LS} / \text{Pulse} < 40\text{ ns}$	4			
	LS; Sink		4			

Package Drawing P-DSO-8



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