October 23, 2001 Objective specification
Version : 1.1

TDA8920TH

Class-D audio amplifier 2 x 80W Single chip

1. General description

The TDA8920 is a high efficiency class-D audio power amplifier. Typical output power is 2 x 80 W and it operates with high efficiency and very low dissipation. The device comes in a HSOP24 power package with a small internal heatsink. Depending on supply voltage and load conditions a very small or even no external heatsink is required. The amplifier operates over a wide supply voltage range from ±12.5 up to =±30 V and consumes a very low quiescent current.

2. Features

- High efficiency (~90%)
- Operating voltage from ±12.5 V to ± 30V
- Very low quiescent current
- Low distortion
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Fixed gain of 30 dB in Single Ended (SE) and 36 dB in Bridge-Tied-Load (BTL)
- High output power
- Good ripple rejection
- Internal switching frequency can be overruled by an external clock
- No switch-on or switch-off plop noise
- Short-circuit proof across the load
- Electrostatic discharge protection
- Thermally protected

3. Applications

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters)

4. Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General, V_p = ± 25V						
V_p	operating supply voltage		±12.5	±25	±30	V
$I_{q(tot)}$	total quiescent current	No load connected	-	55	75	mA
η	efficiency	P_o = 30 W, SE: R_L=2x8Ω f_i=1kHz	-	90	-	%
Stereo single-ended configuration						
P_o	output power	R_L=8Ω, THD = 10%, Vp= ± 25V note 1	36	39	-	W
		R_L=4Ω, THD = 10%, Vp= ± 27V note 1	74	80	-	W
Mono Bridge-Tied load configuration						
P_o	output power	R_L=4Ω, THD = 10%, Vp= ± 17V note 1	100	110	-	W
		R_L=8Ω, THD = 10%, Vp= ± 25V note 1	128	140	-	W

Notes
1. See also section 15.2.5: “ heatsink requirements” in the test and application information

5. Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8920TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-2

6. Block diagram

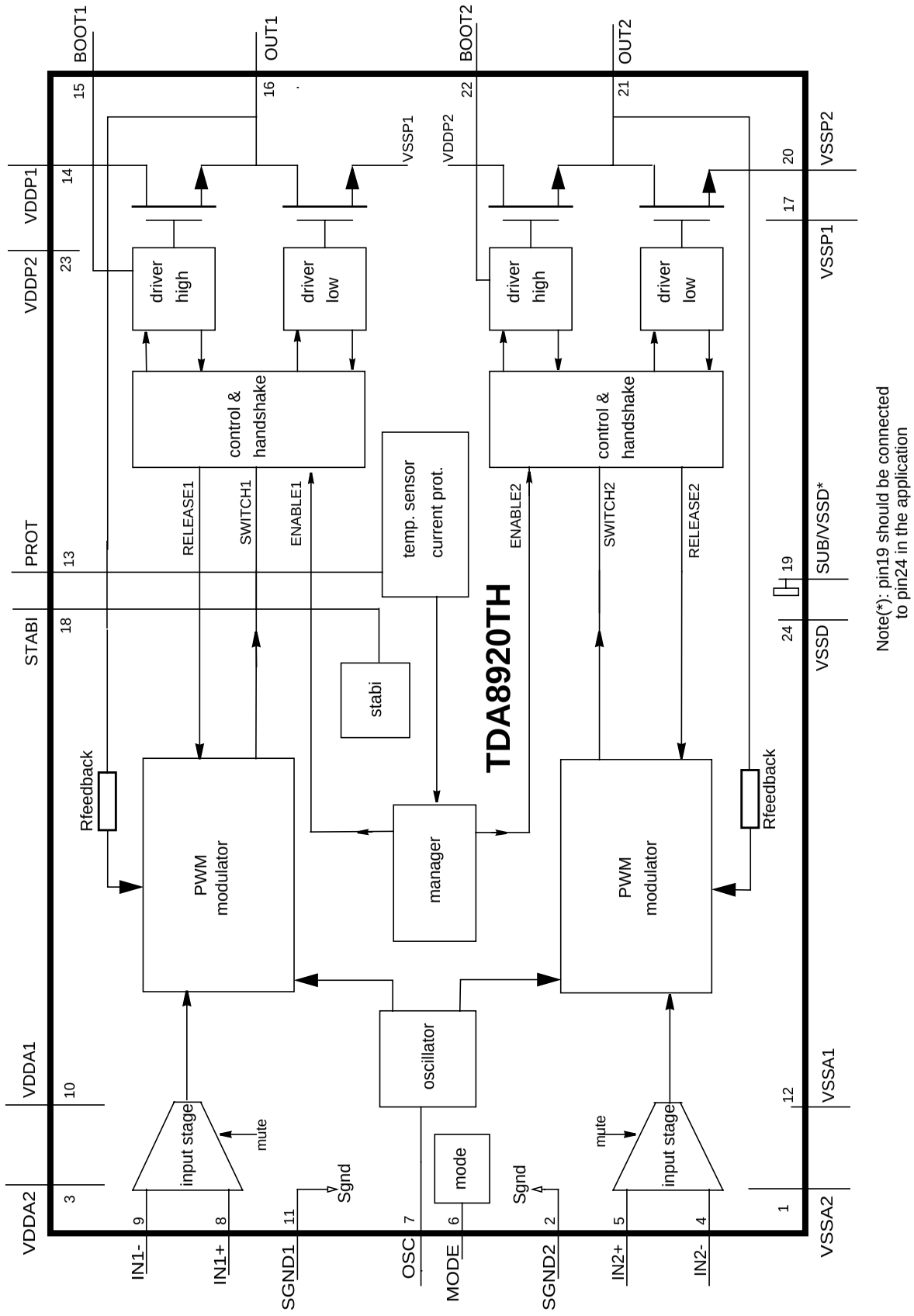
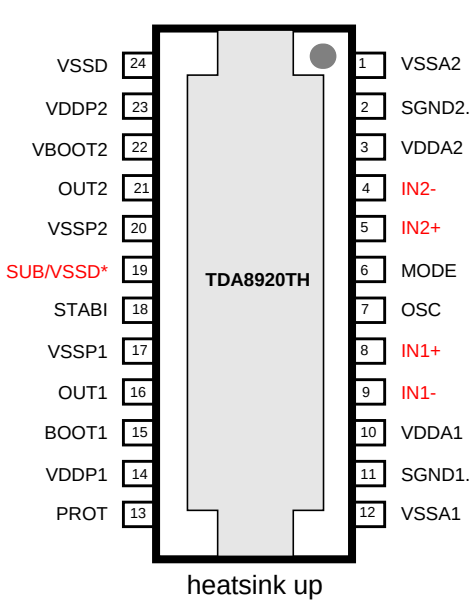


Figure 1: Block diagram of TDA8920TH

7. Pinning information

SYMBOL	PIN	DESCRIPTION
VSSA2	1	Negative analog supply channel 2
SGND2	2	Signal ground channel 2
VDDA2	3	Positive analog supply channel 2
IN2-	4	Negative audio input channel 2
IN2+	5	Positive audio input channel 2
MODE	6	Mode select input (standby/mute/operating)
OSC	7	Oscillator frequency adjustment, or tracking input
IN1+	8	Positive audio input channel 1
IN1-	9	Negative audio input channel 1
VDDA1	10	Positive analog supply channel 1
SGND1	11	Signal ground channel 1
VSSA1	12	Negative analog supply channel 1
PROT	13	Time constant capacitor for protection delay
VDDP1	14	Positive power supply channel 1
BOOT1	15	Bootstrap capacitor channel 1
OUT1	16	PWM output channel 1
VSSP1	17	Negative power supply channel 1
STABI	18	Decoupling internal stabilizer for logic supply
SUB/VSSD	19	Substrate, must be connected to negative supply VSSD (pin 24)
VSSP2	20	Negative power supply channel 2
OUT2	21	PWM output channel 2
BOOT2	22	Bootstrap capacitor channel 2
VDDP2	23	Positive power supply channel 2
VSSD	24	Negative digital supply



Note (*): pin 19 should be connected to pin 24 in the application

Figure 2 : Pin configuration of TDA8920TH

8. Functional description

8.1 General

The TDA8920TH is a two channel audio power amplifier using class-D technology. A typical application schematic is given in figure 4. In section 15.2.8 a detailled application reference design is provided. Via an analog input stage and PWM modulator the audio input signal is converted into a digital PWM signal. To drive the output power transistors this digital PWM signal is applied to a control and handshake block and driver circuits for both highside and lowside. In this way a level shift is performed from the low power digital PWM signal at logic levels to a high power PWM signal switching between the main supply lines.
A second order low pass filter converts the PWM signal to an analog audio signal across the loudspeaker.

The TDA8920TH one-chip class-D amplifier contains high power D-MOS switches, drivers, timing and handshaking between the power switches and some control logic. For protection a temperature sensor and a maximum current detector are built-in on the chip.

The two audio channels of the TDA8920TH contain two pulse width modulators (PWM), two analog feedback loops and two differential input stages. Furthermore it contains circuits common to both channels like the oscillator, all reference sources, the mode functionality and a digital timing manager.

The TDA8920TH contains two independent amplifier channels with high output power, high efficiency (90%), low distortion and a low quiescent current. The amplifier channels can be connected in the following configurations:

- Mono bridge-tied load (BTL) amplifier
- Stereo single-ended (SE) amplifiers.

The amplifier system can be switched in three operating modes with the MODE select pin:

- Standby mode, with a very low supply current.
- Mute mode, the amplifiers are operational, but the audio signal at the output is suppressed.
- Operating mode (amplifier fully operational) with output signal.

For suppressing pop noise the amplifier will remain automatically in the mute mode for approx.150ms before switching to operating (see also figure 5). In this time the coupling capacitors at the input are fully charged. See fig. 3 for an example of a switching circuit for driving the mode pin.

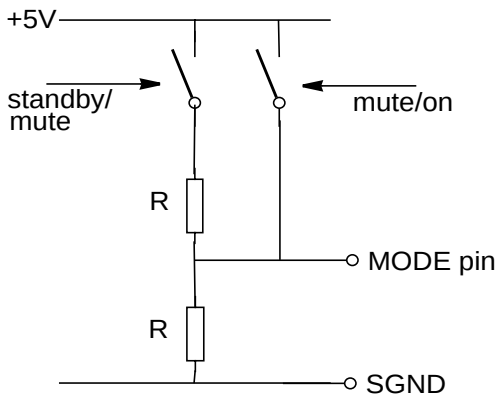


Figure 3: Example of mode select circuit

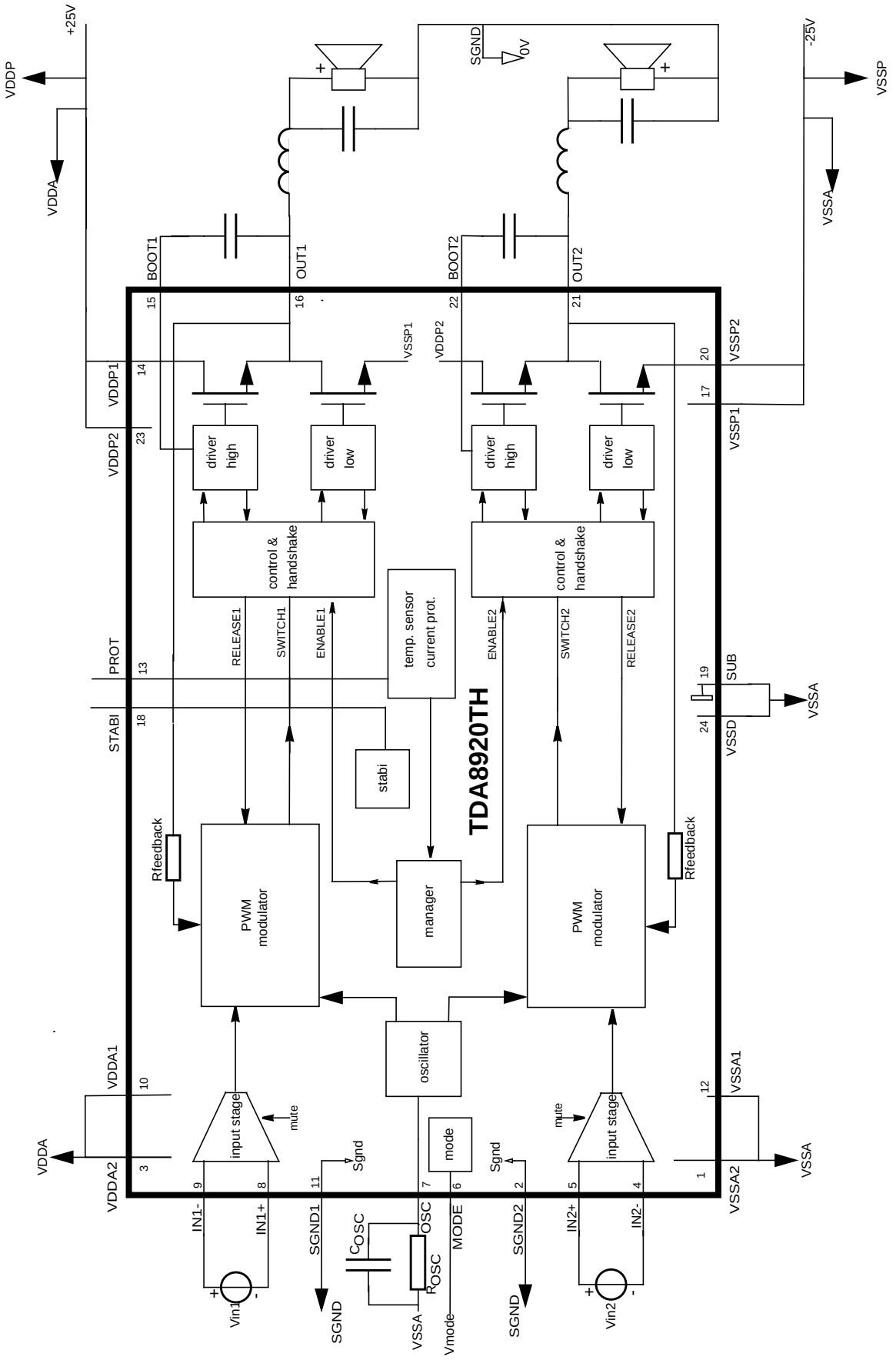
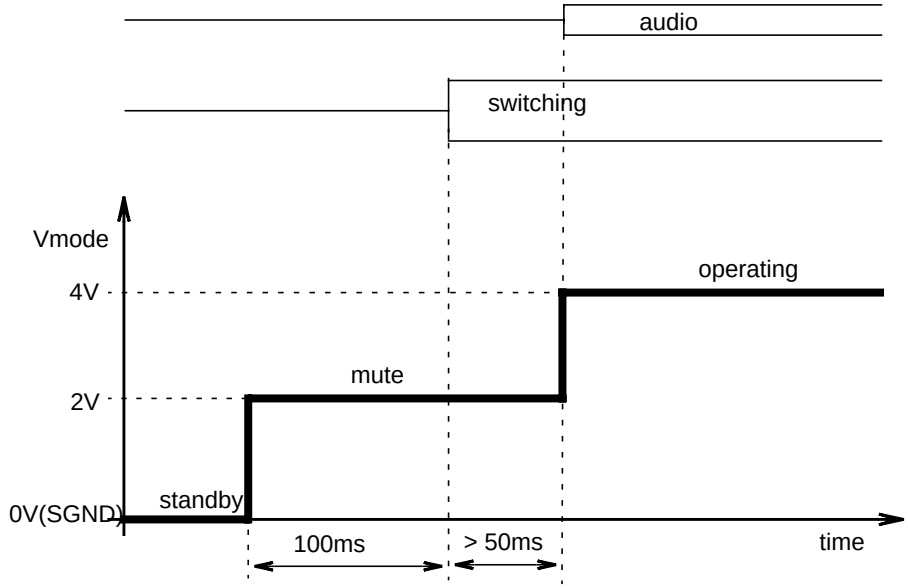
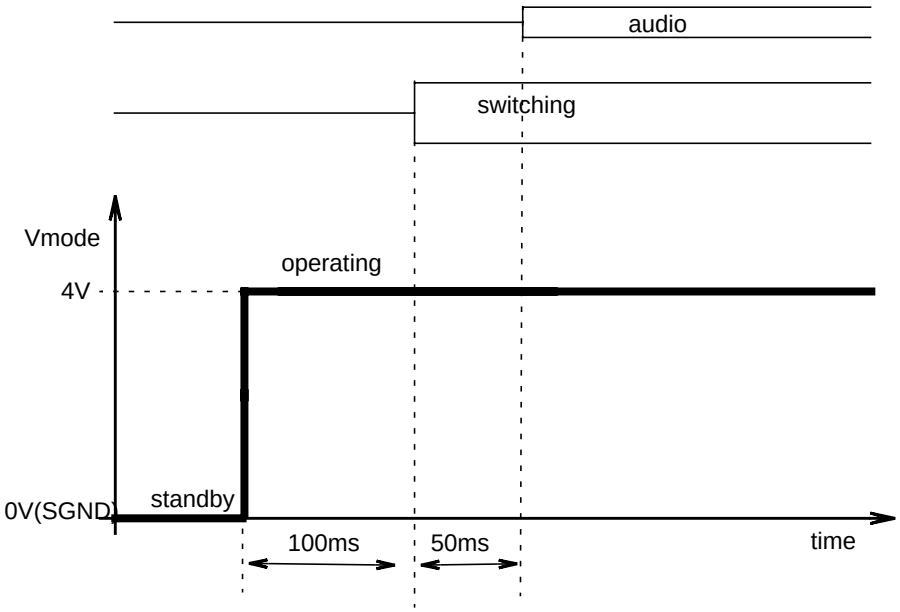


Figure 4: Typical application schematic of TDA8920TH



When switching from standby to mute there is a delay of 100ms before the output starts switching.
Audio signal is available after the mode pin has been set to operating, but not earlier than 150ms after switching to mute.



When switching from standby to operating there is a first delay of 100ms before the outputs starts switching.
After a second delay of 50ms the audio signal is available

Figure 5: Timing mode pin

8.2 Pulse Width Modulation (PWM) frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approx. 350 kHz. Using a second order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. This switching frequency is fixed by an external resistor R_{OSC} connected between pin OSC (pin 7) and VSSA1 (pin 12). With the resistor value given in the schematic of the reference design, the carrier frequency is typical 350 kHz. The carrier frequency can be calculated using:

$$f_{osc} = 9 \times 10^9 / R_{osc} \text{ [Hz]}$$

If two or more class-D amplifiers are used in the same audio application, it is advised to have all devices working at the same switching frequency. This can be realized by connecting all OSC pins together and feed them from a external central oscillator. Using an external oscillator it is necessary to force the OSC pin to a DC-level above SGND for switching form internal to external oscillator. In this case the internal oscillator is disabled and the PWM will be

switching on the external frequency.The frequency range of the external oscillator must be in the range as specified in the switching characteristics.

Application in a practical circuit:

Internal oscillator: R_{osc} connected from OSC pin to V_{SS}
External oscillator: connect oscillator signal between OSC pin and SGND pin; delete R_{osc} and C_{osc}

8.3 Protections

Temperature-, supply voltage- and short circuit protections sensors are included on the chip. In case of exceeding the maximum current or maximum temperature the system shuts down. The protection is activated in case of:

8.3.1. Over-temperature

If the junction temperature (Tj) exceeds 150°C, then the power stage shuts down immediately. The power stage starts switching again if the temperature is dropped to approx. 130°C, so there is a hysteresis of approx. 20°C.

8.3.2. Short-circuit across the loudspeaker terminals:

When the loudspeaker terminals are short-circuited this will be detected by the current protection. If the output current exceeds the maximum output current of 7.5 Amp, then the power stage shuts down within less than1µs and the high current is switched off. In this state the dissipation is very low. Every 100ms the system tries to restart again. If there is still a short across the loudspeaker load, the system is switched off again as soon as the maximum current is exceeded.The average dissipation will be low because of this low duty cycle.

8.3.3. Start-up safety test

During the start-up sequence, when the mode pin is switched from standby to mute, the condition at the output terminals of the power stage are checked. In case of a short of one of the output terminals to V_{DD} or V_{SS} the start-up procedure is interrupted and the systems waits for un-shorted outputs. Because the test is done before enabling the power stages, no large currents will flow in case of a short circuit. This system protects for shorts at both sides of the output filter to both supply lines. When there is a short from the power PWM output of the power stage to one of the supply lines - so before the demodulation filter - it will also be detected by the ‘start-up safety test. Practical use of this test feature can be found in detection of shorts on the pcb.
Remark: this test is only operational prior or during the start-up sequence, so not during normal operation.

8.3.4. Supply voltage alarm

If the supply voltage goes below the value of ± 12.5V the under voltage protection is activated and system shuts down correctly and silently without plopnoises. When the supply voltage comes above the threshold the system is restarted again after 100ms. If the supply voltage exceeds ± 32V the overvoltage protection is activated and the power stages shut down. They are enabled again as soon as the supply voltage drops down the threshold.
An additional balance protection compares the positive (Vdd) and the negative (Vss) supply voltages and triggers if the voltage difference between them exceeds a certain level. This level depends on the sum of both supply voltages. An expression for the unbalance threshold level :

$$V_{unb,\,thres} \sim 0.15 \cdot (|Vdd| + |Vss|)$$

Example: with a symmetrical supply of +30V / -30V the protection will be triggered if the unbalance exceeds approx. 9V.

See also section 15.2.7 “pumping effects” in the test and application information.

8.4 Differential audio inputs

For a high common mode rejection and a maximum of flexibility of application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels is inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier and with the same loud-speaker impedance approximately a four times higher output power can be obtained. In figure 6 the input configuration for mono BTL application is given (for more information see the application information).
Also in the stereo single ended configuration it is recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies.

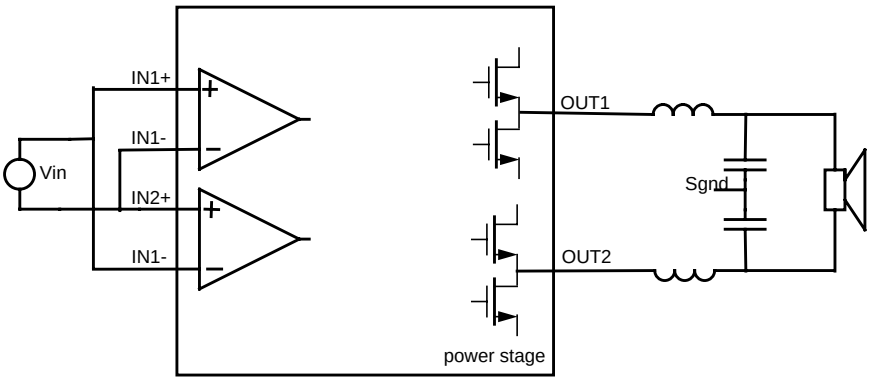


Figure 6 : Input configuration for mono BTL application

9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_p	supply voltage		–	±30	V
V_{ms}	mode select switch voltage	with respect to SGND	–	5.5	V
V_{sc}	short circuit voltage of output pins		–	±30	V
I_{ORM}	repetitive peak current in output pin	note 1	–	7.5	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

10. Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air note 2, 3	35	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	note 2, 3	2	K/W

Notes
1. See also section 15.2.6 : “output current limiting” in the test and application information
2. See also section 15.2.5 : “heatsink requirements” in the test and application information
3. Under investigation

11. Quality specification

In accordance with *“**SNW-FQ611-partD**”* if this type is used as an audio amplifier.

12. Static characteristics

V_p = ±25 V; T_{amb} = 25 °C; measured in Fig. 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_p	supply voltage range	note 1	±12.5	±25	±30	V
I_q	quiescent current	no load connected	-	55	75	mA
I_{stb}	standby current		-	100	500	µA
Mode select pin						
V_{ms}	input voltage range	note 2	0	-	5.5	V
I_{ms}	input current	V_{ms} = 5.5 V	-	-	1000	µA
$V_{standby}$	input voltage range mode select for standby mode	note 2, 3	0	-	0.8	V
V_{mute}	input voltage range mode select for mute mode	note 2, 3	2.0	-	2.8	V
V_{on}	input voltage range mode select for on mode	note 2, 3	4.2	-	5.5	V
Audio input pins						
V_{inDC}	DC input level	note 2		0		V
Amplifier outputs						
$\lvert V_{OOSE} \rvert$	output offset voltage single-ended (SE)	on and mute	-	-	150	mV
$\lvert \Delta V_{OOSE} \rvert$	delta output offset voltage single-ended (SE)	on ↔ mute	-	-	80	mV
$\lvert V_{OOBTL} \rvert$	output offset voltage bridge-tied- load (BTL)	on and mute	-	-	215	mV
$\lvert \Delta V_{OOBTL} \rvert$	delta output offset voltage bridge-tied-load (BTL)	on ↔ mute	-	-	115	mV
Stabilizer						
V_{stabi}	Stabilizer output voltage	mute and operating note 4	11	13	15	V
Temperature protection						
T_{prot}	Temperature protection activation		150	-	-	°C
T_{hys}	Hystereses on temperature protection		-	20	-	°C

Notes

1. The circuit is DC adjusted at V_p = ±12.5 to ±30 V.
2. With respect to SGND (0 V).
3. The transition regions between standby-mute-on contain hystereses (see fig. 7)
4. With respect to V_{SS}

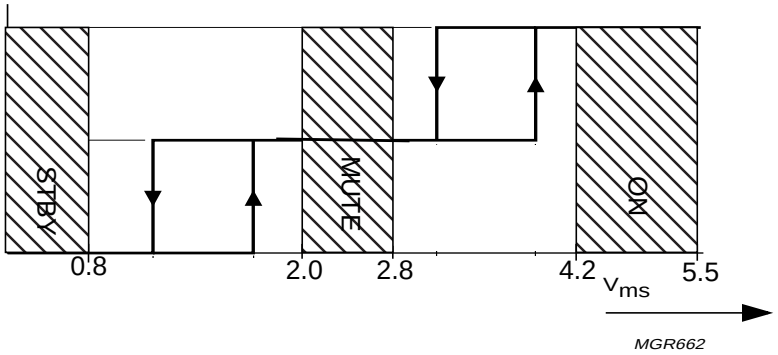


Figure 7 : mode select pin behaviour

13. Switching characteristics

V_p = ±25 V; T_{amb} = 25 °C; measured in Fig. 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching frequency						
f_{oscTYP}	typical oscillator frequency	R_{OSC} = 30.0 kohm, see reference design	309	317	329	kHz
f_{osc}	oscillator frequency range	Note 1	210		600	kHz
V_{OSC}	maximum voltage at OSC pin	frequency tracking			SGND+ 12	V
V_{OSC_trip}	Triplevel at OSC pin for tracking	frequency tracking	-	SGND+ 2.5	-	V
f_{track}	frequency range for tracking	frequency tracking	210		600	kHz
V_{OSC}^{EXT}	Amplitude at OSC pin for tracking	Note 2	-	5	-	V

Notes
1. Frequency set with Rosc, according to formula in functional description
2. For tracking the external oscillator has to switch around (SGND+2.5V) with a minimum amplitude of V_{OSC}EXT

14. Dynamic AC characteristics

Stereo/dual single ended (SE) application

V_p=±25V; R_L=8 Ω; f_i=1kHz; f_{osc}=317 kHz; R_{sL}<0.1Ω (note 11); T_{amb}=25°C;measured in Fig. 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	R_L=8Ω, V_p = ±20V; THD = 0.5% note 1	18	20	-	W
		R_L=8Ω, V_p = ±20V; THD = 10% note 1	23	25	-	W
		R_L=8Ω, V_p = ±25V; THD = 0.5% note 1	28	30	-	W
		R_L=8Ω, V_p = ±25V; THD = 10%; note 1	36	39	-	W
		R_L=4Ω, V_p = ±25V; THD = 0.5% note 1	51	55	-	W
		R_L=4Ω, V_p = ±25V; THD = 10% note 1	65	70	-	W
		R_L=4Ω, V_p = ±27V; THD = 0.5% note 1	60	65	-	W
		R_L=4Ω, V_p = ±27V; THD = 10% note 1	74	80	-	W
THD	total harmonic distortion	P_o = 1 W; note 2				
		f_i = 1 kHz	-	0.01	0.05	%
		f_i = 10 kHz	-	0.08	-	%
G_v	closed loop voltage gain		29	30	31	dB
η	efficiency	P_o = 30 W; f_i = 1 kHz; note 3	85	90	-	%
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 4	-	55	-	dB
		on; f_i = 1 kHz; note 5	40	50	-	dB
		mute; f_i = 100 Hz; note 4	-	55	-	dB
		standby; f_i=100 Hz; note 4	-	80	-	dB
$\|Z_i\|$	input impedance		45	68		kΩ
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; note 6	-	200	400	μV
		on; R_s = 10 kΩ; note 7	-	230	-	μV
		mute; note 8	-	220	-	μV
α_{cs}	channel separation	note 9	-	70	-	dB
$\|\Delta G_v\|$	channel unbalance		-	-	1	dB
$V_{o,mute}$	output signal in mute	note 10	-	-	400	μV
CMRR	common mode rejection ratio	$V_{i(CM)(rms)}$ = 1 V	-	75	-	dB

Notes

1. Output power is measured indirectly; based on R_{dson} measurement
2. Total Harmonic Distortion is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a lower order lowpass filter a significant higher value is found, due to the switching frequency outside the audio band.
3. Output power measured across the loudspeaker load.
4. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 100 Hz; R_s = 0 Ω.
5. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); f_i = 1 kHz; R_s = 0 Ω.
6. B = 22 Hz to 22 kHz; R_s = 0 Ω.
7. B = 22 Hz to 22 kHz; R_s = 10 kΩ.
8. B = 22 Hz to 22 kHz; independent of R_s.
9. P_o = 1 W; R_s = 0 Ω.
10. $V_i = V_{i(max)}$ = 1 V (RMS).
11. R_{sL} = series resistance of inductor of low-pass LC-filter in the application

Mono bridge-tied-load (BTL) application

V_p = ±25 V; R_L=8 Ω; f_i = 1 kHz; f_{osc} = 317 kHz; R_{sL} < 0.1Ω (note 10); T_{amb} = 25 °C; measured in Fig. 8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Po	output power	RL=8Ω, V_p=±25V; THD=0.5% note 1	100	110	-	W
		RL=8Ω, V_p=± 25V; THD=10% note 1	128	140	-	W
		RL=8Ω,V_p=± 21V; THD=0.5% note 1	73	79	-	W
		RL=8Ω, V_p=± 21V; THD=10% note 1	92	100	-	W
		RL=4Ω, V_p=±17V; THD=0.5% note 1	66	75	-	W
		RL=4Ω, V_p=±17V; THD=10% note 1	100	110	-	W
THD	total harmonic distortion	P_o = 1 W; note 2				
		f_i = 1 kHz	-	0.015	0.05	%
		f_i = 10 kHz	-	0.02	-	%
G_v	closed loop voltage gain		35	36	37	dB
η	efficiency	P_o = 140 W; f_i = 1 kHz; note 3	85	89	-	%
SVRR	supply voltage ripple rejection	on; f_i = 100 Hz; note 4	-	49	-	dB
		on; f_i = 1 kHz; note 5	36	44	-	dB
		mute; f_i = 100 Hz; note 4	-	49	-	dB
		standby; f_i=100 Hz; note 4	-	80	-	dB
$\|Z_i\|$	input impedance		22	34		kΩ
$V_{n(o)}$	noise output voltage	on; R_S = 0 Ω; note 6	-	280	560	μV
	output signal in mute	on; R_S = 10 kΩ; note 7	-	300	-	μV
		mute; note 8	-	280	-	μV
$V_{o,mute}$		note 9	-	-	500	μV
CMRR	common mode rejection ratio	$V_{i(CM)(rms)}$ = 1 V	-	75	-	dB

Notes

1. Output power is measured indirectly; based on R_{dson} measurement
2. Total Harmonic Distortion is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a low order lowpass filter a significant higher value will be found, due to the switching frequency outside the audio band.
3. Output power measured across the loudspeaker load.
4. V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); f_i = 100 Hz; R_S = 0 Ω.
5. V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); f_i = 1 kHz; R_S = 0 Ω.
6. B = 22 Hz to 22 kHz; R_S = 0 Ω.
7. B = 22 Hz to 22 kHz; R_S = 10 kΩ.
8. B = 22 Hz to 22 kHz; independent of R_S.
9. V_i = $V_{i(max)}$ = 1 V (RMS).
10. R_{sL} = series resistance of inductor of low-pass LC-filter in the application

15. Test and application information

15.1 Test information

To be finished

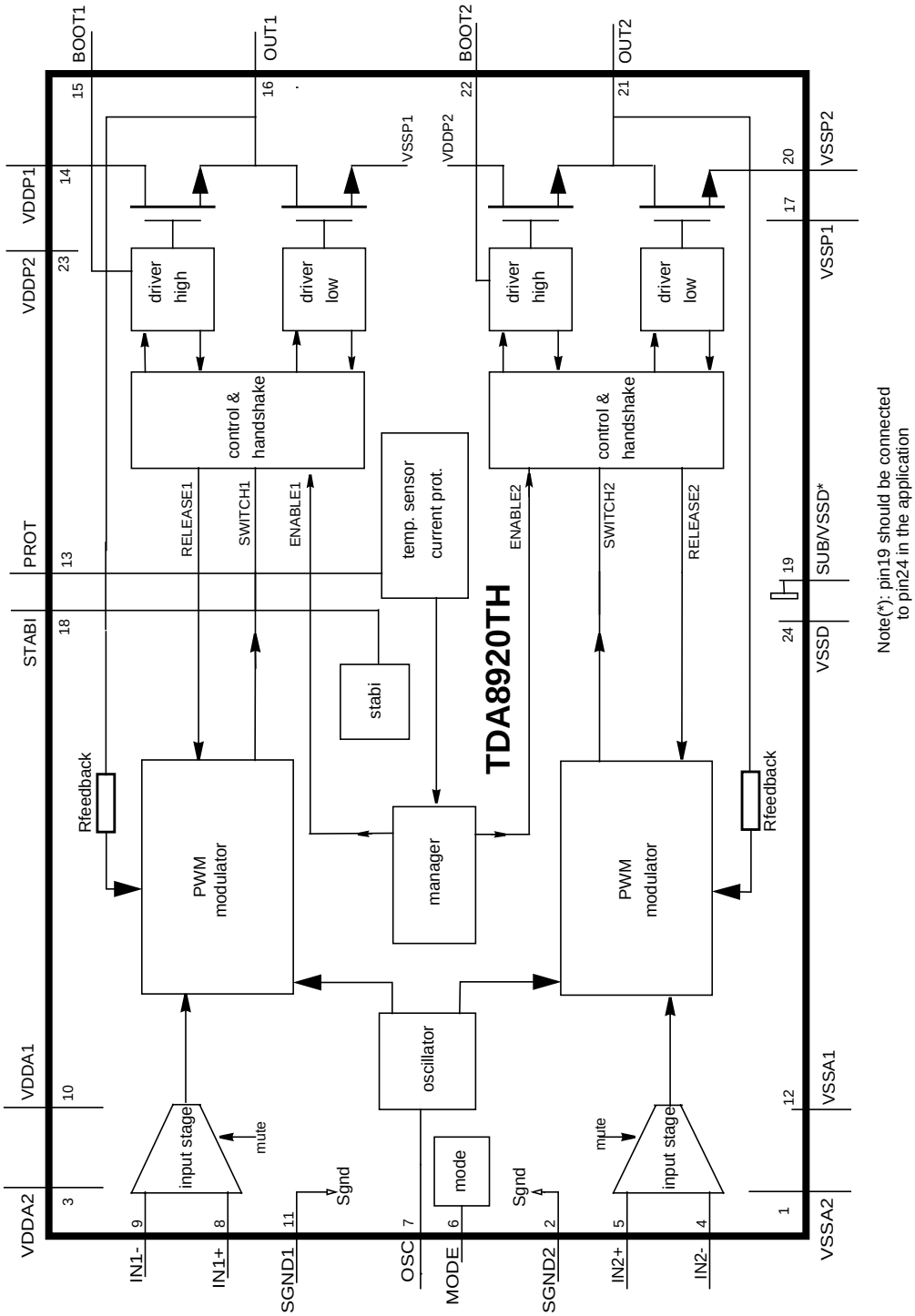


Figure 8: Test circuit

15.2 Application information

15.2.1 BTL application

For using the system in mono BTL application (for more output power), the inputs of both channels must be connected in parallel. The phase of one the inputs must be inverted (see also figure 6 in section 8.5). In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

15.2.2 MODE pin

For correct operation the switching voltage at the mode pin should be de-bounced. If the mode pin is driven by a mechanical switch an appropriate debouncing low pass filter should be used. If the mode pin is driven by an electronic circuit or micro controller then it should remain for at least 100ms at the mute voltage level before switching back to the standby voltage level.

15.2.3 Output power estimation

The output power in several applications (SE and BTL) can be estimated using the following expressions:

SE : $P_{out\_1\%} = \dfrac{\left(\dfrac{R_{Load}}{R_{Load} + 0.6} \cdot Vp\,(1 - t_{min} \cdot f_{osc})\right)^2}{2 \cdot R_{Load}}$

Maximum current : $I_{out\hat{}} = \dfrac{Vp\,(1 - t_{min} \cdot f_{osc})}{R_{Load} + 0.6}$ should not exceed 7.5 Amp

BTL : $P_{out\_1\%} = \dfrac{\left(\dfrac{R_{Load}}{R_{Load} + 1.2} \cdot 2Vp\,(1 - t_{min} \cdot f_{osc})\right)^2}{2 \cdot R_{Load}}$

Maximum current : $I_{out\hat{}} = \dfrac{2\,Vp\,(1 - t_{min} \cdot f_{osc})}{R_{LOAD} + 1.2}$ should not exceed 7.5 Amp

Legend:

R_{LOAD} = Load impedance
f_{osc} = Oscillator frequency
t_{min} = minimum pulse width (typical 190 ns)
Vp = single sided supply voltage (so if supply +/-30V symmetrical -> Vp =30V)
Pout_1% =Output power just at clipping
Pout_10% = Output power at THD = 10%
Pout_10% =1.25 x Pout_1%

15.2.4 External clock

In figure 9 a possible solution for an external clock oscillator circuit is given:

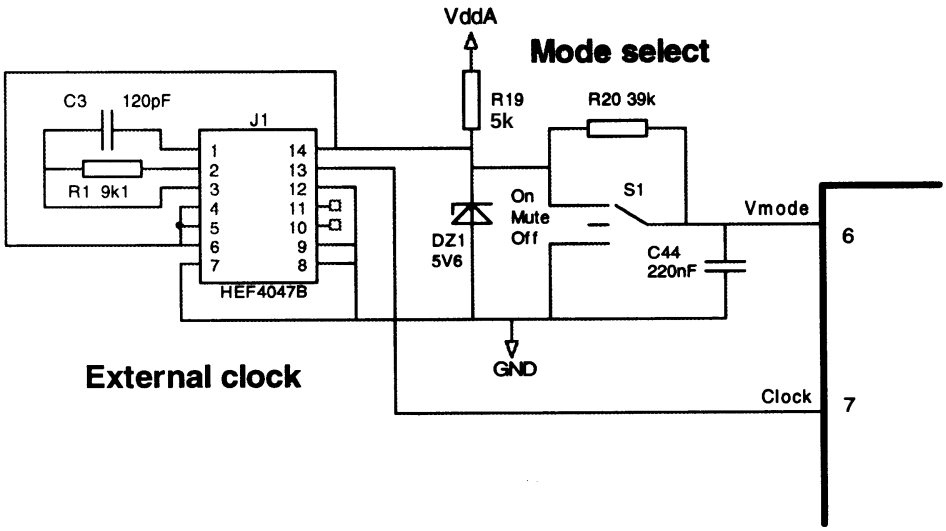


Figure 9 : External oscillator circuit

15.2.5 Heatsink requirements

In some applications it may be necessary to connect an external heatsink to the TDA8920TH. The determining factor is the 150 degr. maximum junction temperature, T_{jmax} which cannot be exceeded.The expression below shows the relation between the maximum allowable power dissipation and the total thermal resistance from junction to ambient:

$$R_{thja} = (T_{j(max)} - T_A) / P_{diss}$$

P_{diss} is determined by the efficiency (η) of the 1-chip class-D amplifier. The efficiency measured in the TDA8920TH as a function of output power is given in figure 19 of section 15.2.12. From figure 18 in section 15.2.12 the power dissipation can be derived as function of output power.

In figure 10 derating curves are given for several values of the Rthj-a. A maximum junction temperature T_J=150 °C is taken into account. From this figure the maximum allowable power dissipation for a given heatsink size can be derived or the required heatsink size can be determined at a required dissipation level.

Example 1 :
P_{out} = 2x30W into 8Ω
T_{jmax}=150 °C
T_a=60 °C
$P_{diss,tot}$ = 6W (from figure 18 of section 15.2.12)

The required R_{thj-a} = 15 K/W can be calculated.
The R_{thj-a} of TDA8920TH in free air is 35 K/W. The R_{thj-c} of TDA8920TH is 2 K/W, so a heatsink of 13 K/W is required for this example.
In actual applications, other factors such as the average P_{diss} with music source (as opposed to a continuous sine wave) will determine the size of the heatsink required.

Example 2 :
P_{out} = 2x75W into 4Ω
T_{jmax}=150 °C
T_a=60 °C

$P_{diss,tot}$ = 17.5 W (from figure 18 of section 15.2.12).

The required Rthj-a = 5.14 K/W.
The R_{thj-a} of TDA8920TH in free air is 35 K/W. The R_{thj-c} of TDA8920TH is 2 K/W, so a heatsink of 3.14 K/W is required for this example.

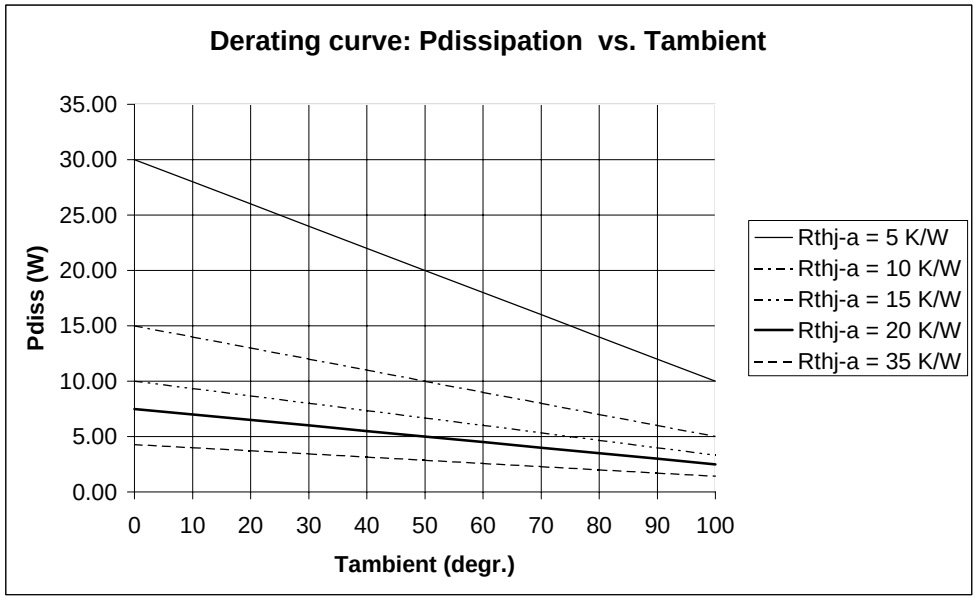


Figure 10: derating curves for power dissipation as a function of maximum ambient temperature

15.2.6 Output current limiting

To be fixed

15.2.7 Pumping effects

To be fixed

15.2.8 Reference design

The reference design for the single chip class-D audio amplifier for TDA8920TH is shown in figure 11. The Printed-Circuit Board (PCB) layout is shown in table 1. The bill of materials is given in Table 2.

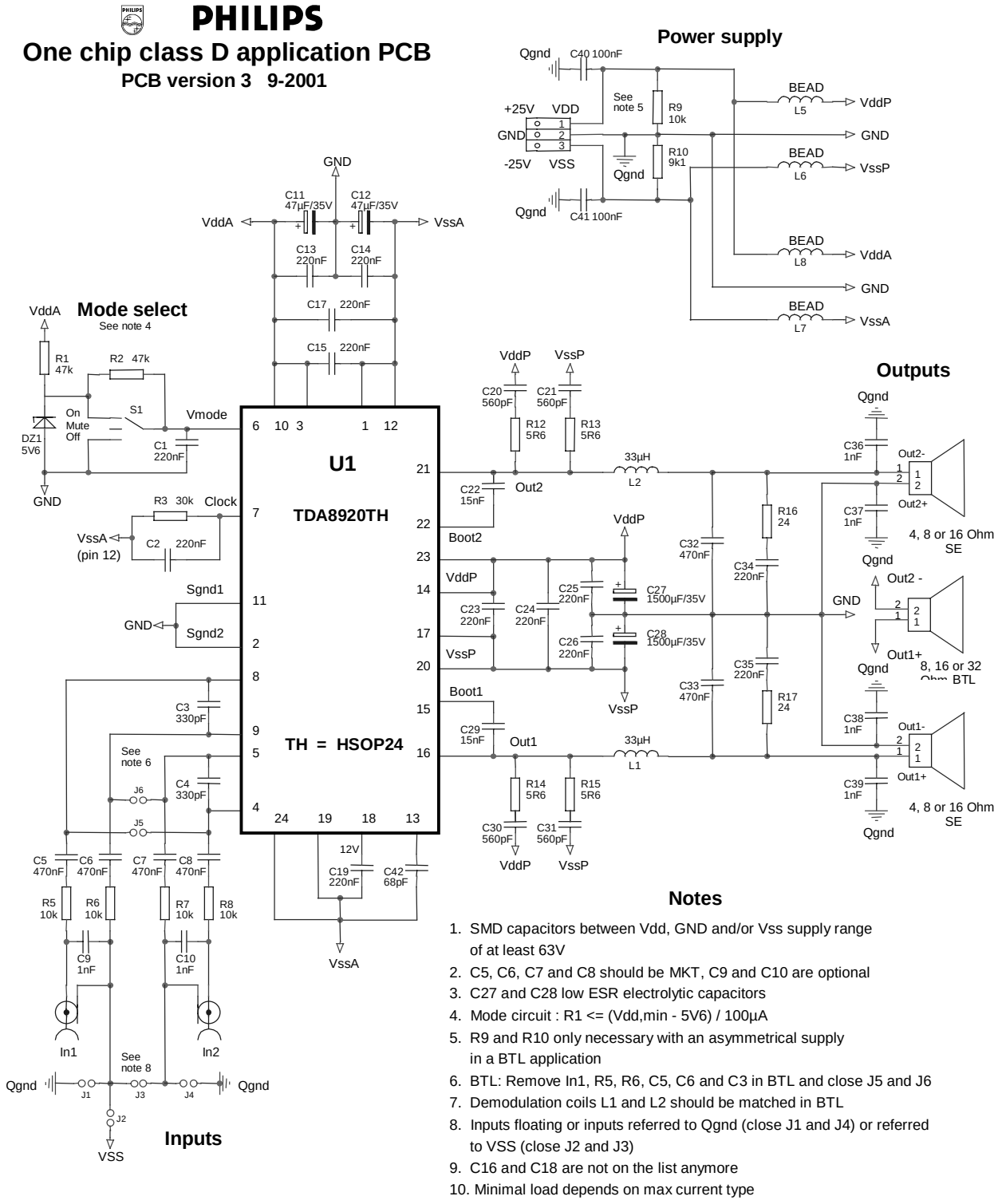


Figure 11: Single chip class-D audio amplifier application diagram for TDA8920TH

15.2.9 PCB information for HSOP24 encapsulation

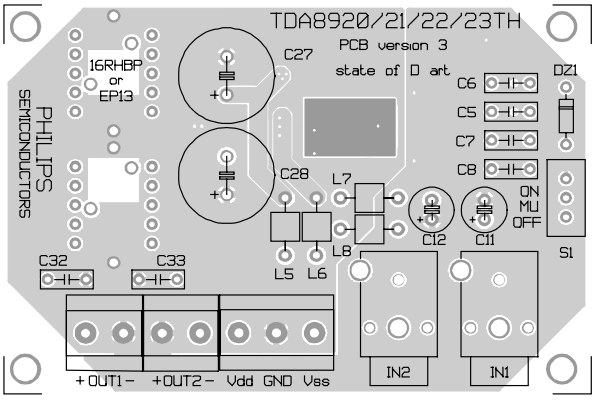
The size of the Printed Circuit Board is 77.47 mm x 51.28 mm, dual sided 70mm copper with 98 metallized through holes.

The standard configuration is Symmetrical Supply with stereo SE outputs.
The PCB is also suitable for mono BTL configuration as well for symmetrical supply as for asymmetrical supply.
It is possible to use several different output filter inductors as CDRH-, 16RHBP- or EP13-types to evaluate the performance versus price or size.

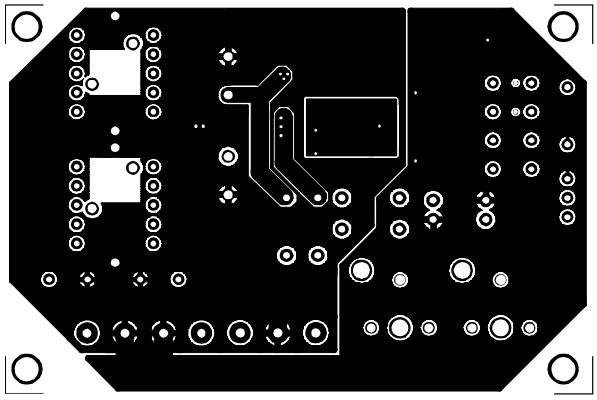
15.2.10 Classification

The application shows optimized signal performance and includes several EMI optimizations.

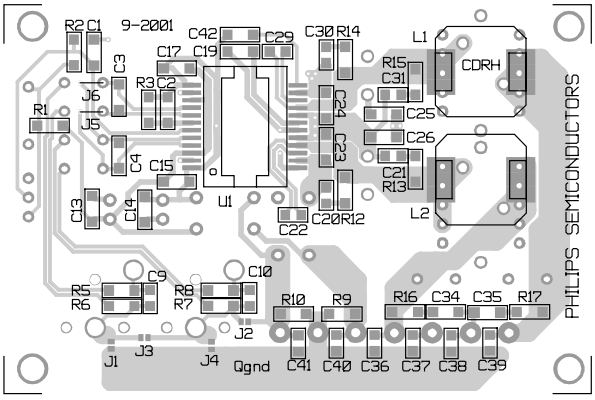
Table 1: Printed-circuit board layout for TDA8920TH



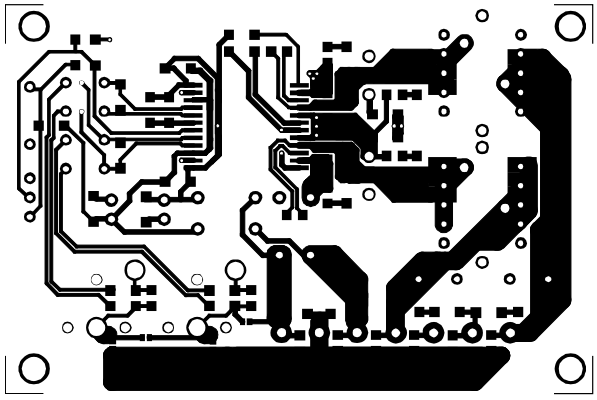
Top silk screen



Top copper



Bottom silk screen



Bottom copper

15.2.11 Reference design bill of materials

Table 2: Single-chip class-D audio amplifier PCB (Version 3; 09-2001) for TDA8920TH (see Fig 11 and table 1)

COMPONENT	DESCRIPTION	VALUE	COMMENTS
In1 and In2	Cinch input connectors		2 × Farnell: 152-396
Out1, Out2, V_{DD}, GND and V_{SS}	supply/output connectors		2 × Augat 5KEV-02; 1 × Augat 5KEV-03
S1	on/mute/off switch		PCB switch Knitter ATE 1 E M-O-M
U1	power stage IC	TDA8926J/27J	DBS17P package
U2	controller IC	TDA8929T	SO24 package
L2 and L4	demodulation filter coils	33 µH	2 × Sumida CDRH127-330
L5, L6 and L7	power supply ferrite beads		3 × Murata BL01RN1-A62
C1 and C2	supply decoupling capacitors for V_{DD} to V_{SS} of the controller	220 nF/63 V	2 × SMD1206
C3	clock decoupling capacitor	220 nF/63 V	SMD1206
C4	12 V decoupling capacitor of the controller	220 nF/63 V	SMD1206
C5	12 V decoupling capacitor of the power stage	220 nF/63 V	SMD1206
C6 and C7	supply decoupling capacitors for V_{DD} to V_{SS} of the power stage	220 nF/63 V	SMD1206
C8 and C9	bootstrap capacitors	15 nF/50 V	2 × SMD0805
C10, C11, C12 and C13	snubber capacitors	560 pF/100 V	4 × SMD0805
C14 and C16	demodulation filter capacitors	470 nF/63 V	2 × MKT
C15 and C17	resonance suppress capacitors	220 nF/63 V	2 × SMD1206
C18, C19, C20 and C21	common mode HF coupling capacitors	1 nF/50 V	4 × SMD0805
C22 and C23	input filter capacitors	33 nF/50 V	2 × SMD1206
C24, C25, C26 and C27	input capacitors	470 nF/63 V	4 × MKT
C28, C29, C30 and C31	common mode HF coupling capacitors	1 nF/50 V	2 × SMD0805
C32 and C33	power supply decoupling capacitors	220 nF/63 V	2 × SMD1206
C34 and C35	power supply electrolytic capacitors	1500 µF/35 V	2 × Rubycon ZL very low ESR (large switching currents)
C36, C37, C38 and C39	analog supply decoupling capacitors	220 nF/63 V	4 × SMD1206
C40 and C41	analog supply electrolytic capacitors	47 µF/35 V	2 × Rubycon ZA low ESR
C43	diagnostic capacitor	180 pF/50 V	SMD1206
C44	mode capacitor	220 nF/63 V	SMD1206
D1	5.6 V zener diode	BZX79C5V6	DO-35
D2	7.5 V zener diode	BZX79C7V5	DO-35
R1	clock adjustment resistor	27 kΩ	SMD1206
R4, R5, R6 and R7	input resistors	10 kΩ	4 × SMD1206
R10	diagnostic resistor	1 kΩ	SMD1206
R11, R12, R13 and R14	snubber resistors	5.6 Ω; >0.25 W	4 × SMD1206
R15 and R16	resonance suppression resistors	24 Ω	2 × SMD1206

To be fixed

COMPONENT	DESCRIPTION	VALUE	COMMENTS
R19	mode select resistor	39 kΩ	SMD1206
R20	mute select resistor	39 kΩ	SMD1206
R21	resistor needed when using an asymmetrical supply	10 kΩ	SMD1206
R22	resistor needed when using an asymmetrical supply	9.1 kΩ	SMD1206
R24	bias resistor for powering-up the power stage	200 kΩ	SMD1206

To be fixed

15.2.12 Curves measured in the reference design

Table 2: Curves measured in the reference design

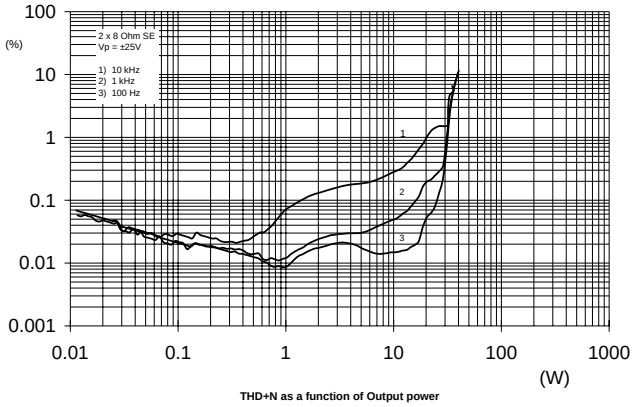


Fig. 12: THD+N as a function of output power

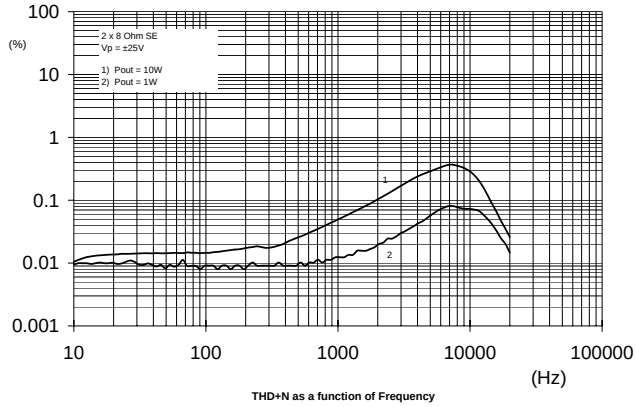


Fig. 13: THD+N as a function of input frequency

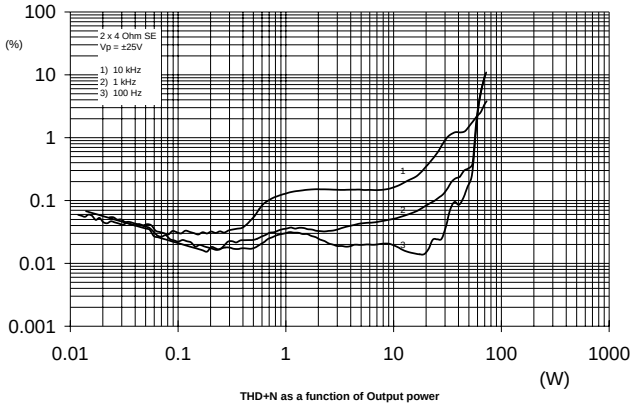


Fig. 14: THD+N as a function of output power

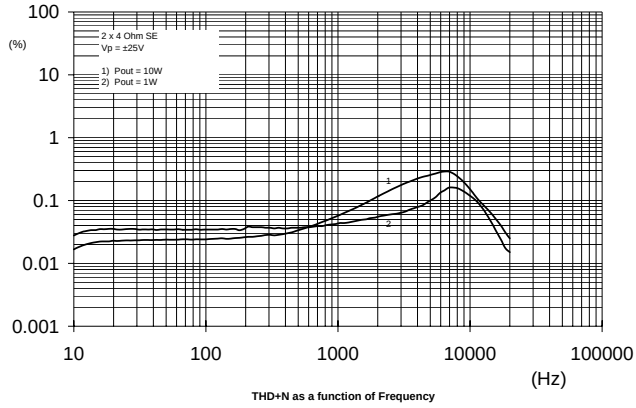


Fig. 15: THD+N as a function of input frequency

Table 2: Curves measured in the reference design

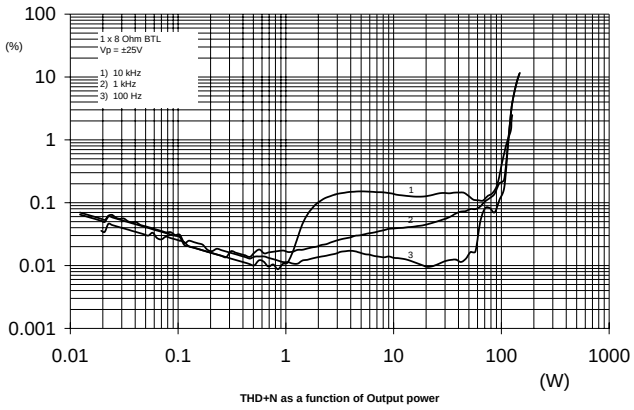


Fig. 16: THD+N as a function of output power

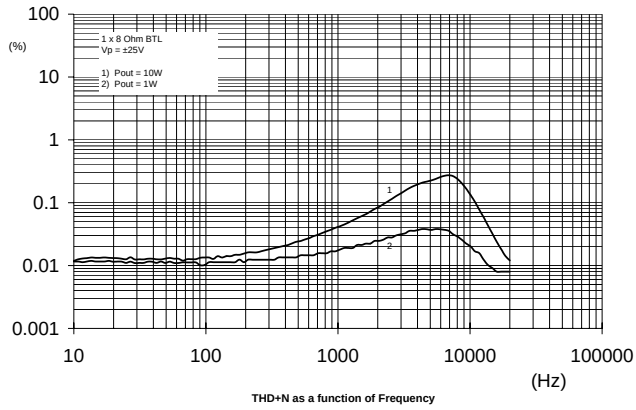


Fig. 17: THD+N as a function of input frequency

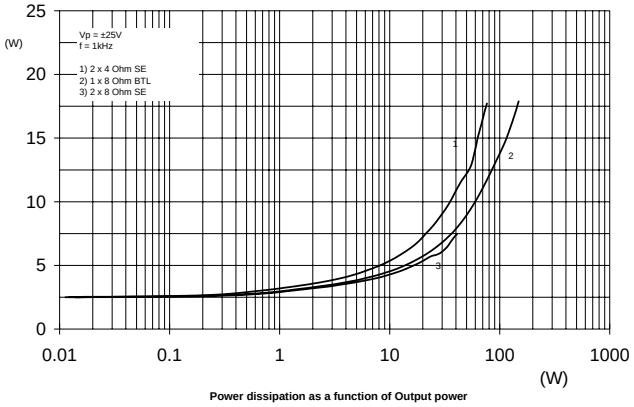


Fig. 18: Power dissipation as a function of output power

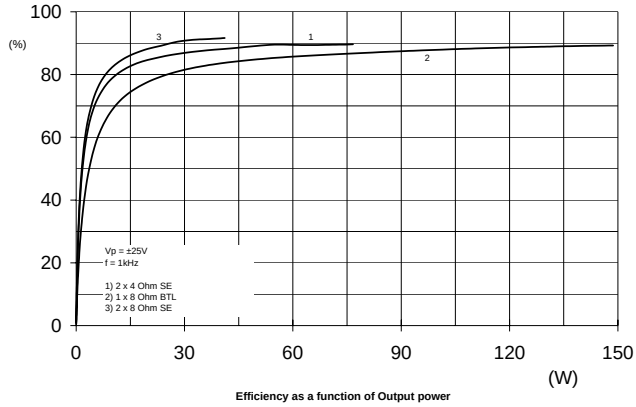


Fig. 19: Efficiency as a function of output power

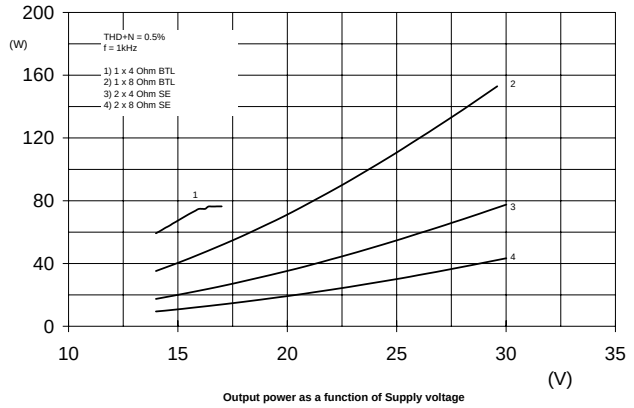


Fig. 20: Output power as a function of supply voltage

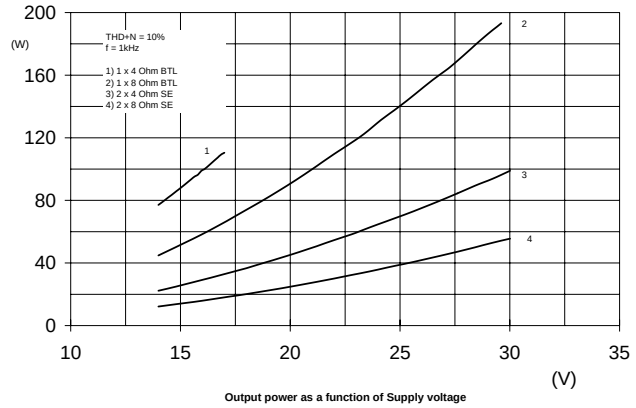


Fig. 21: Output power as a function of supply voltage

Table 2: Curves measured in the reference design

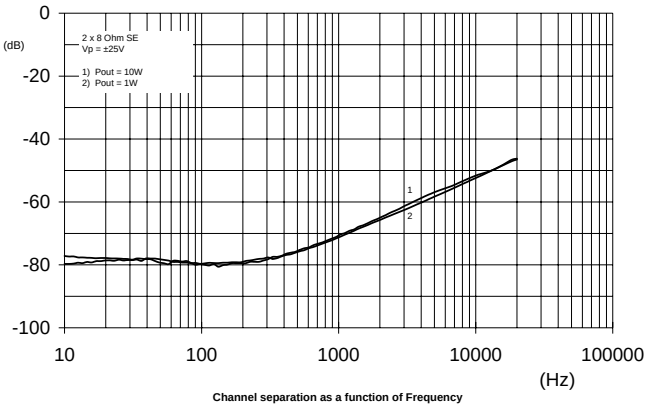


Fig.22: Channel seperation as a function of input frequency

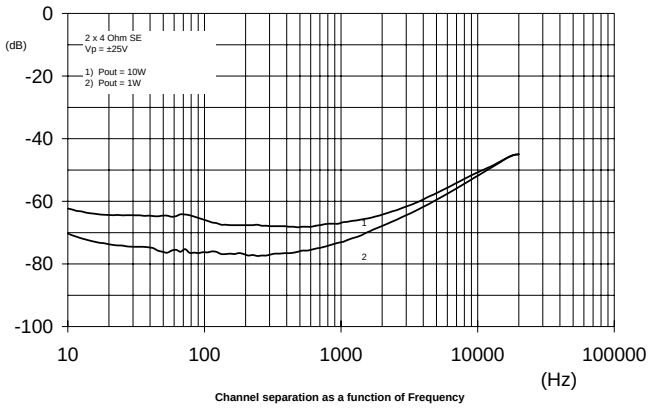


Fig.23: Channel seperation as a function of input frequency

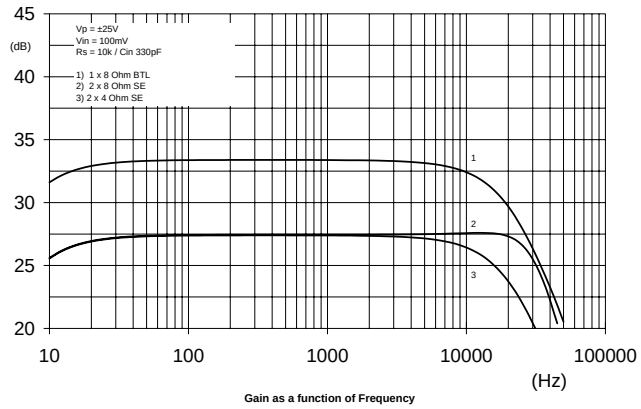


Fig.24: Gain as a function of input frequency

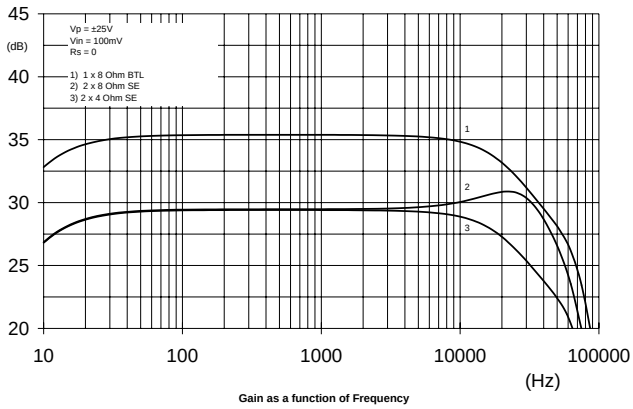


Fig.25: Gain as a function of input frequency

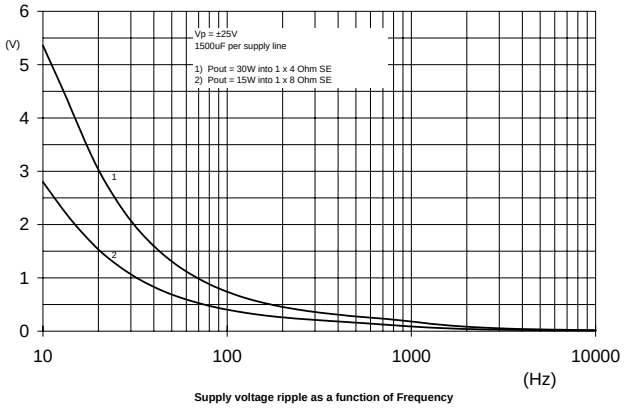


Fig.26: SVRR as a function of input frequency

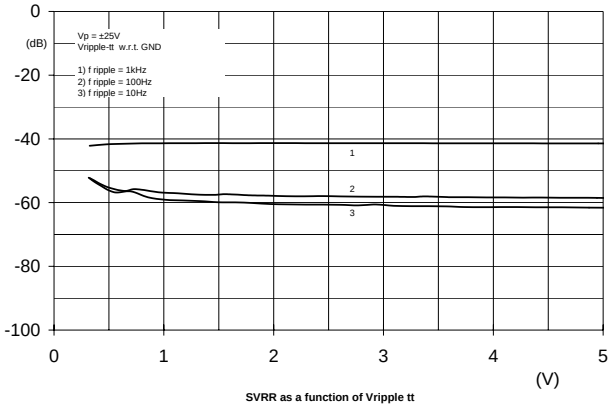


Fig.27: SVRR as a function of Vripple (p-p)

Table 2: Curves measured in the reference design

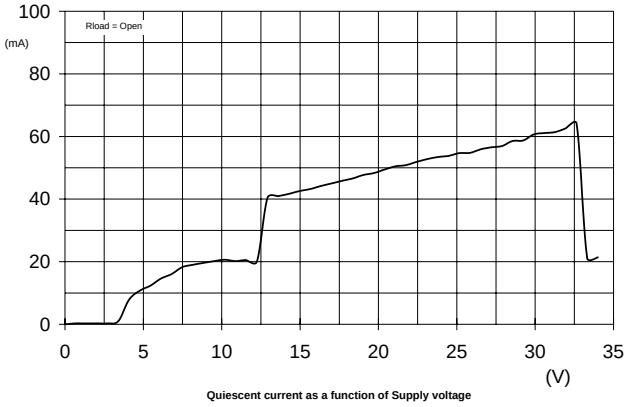


Fig.28: Quiescent current as a function of supply voltage

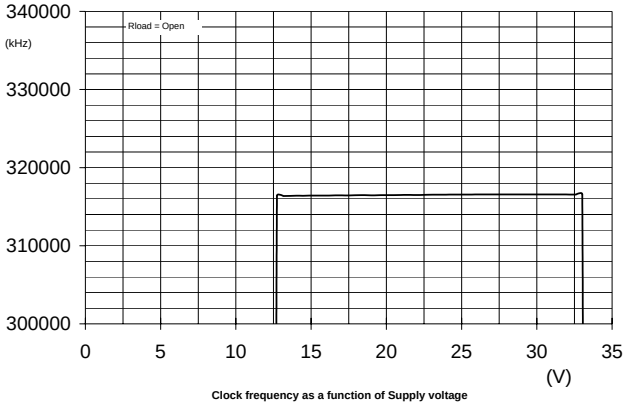


Fig.29: Clock frequency as a function of supply voltage

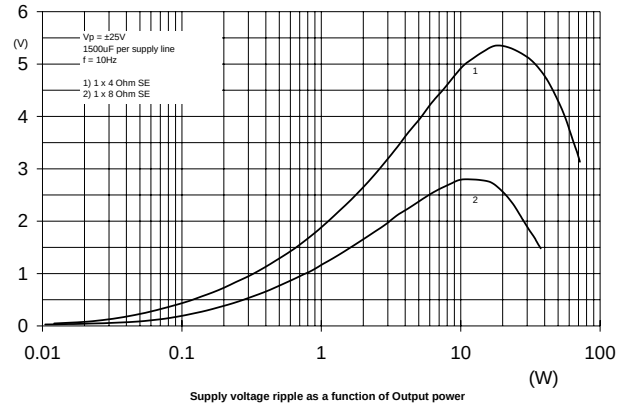


Fig.30: Supply voltage ripple as a function of output power

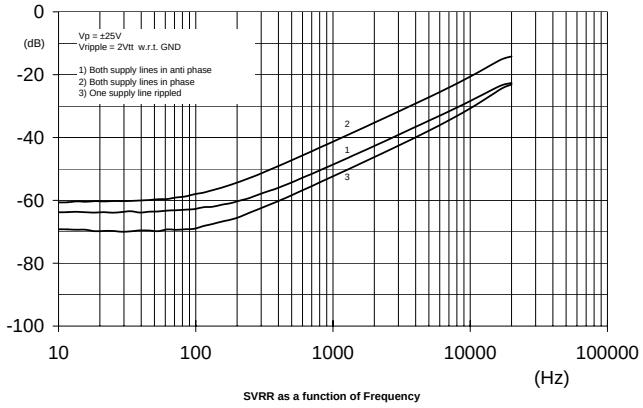


Fig.31: SVRR as a function of input frequency

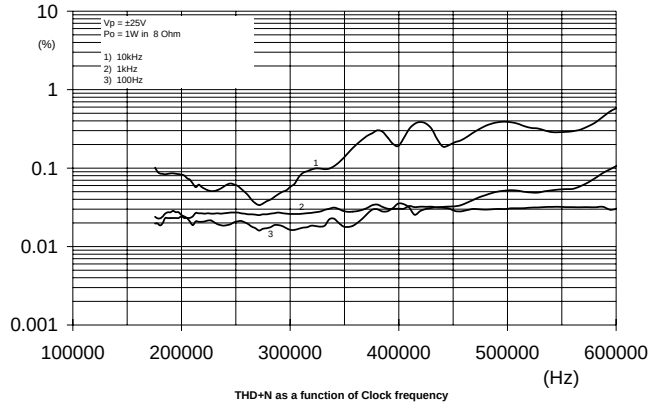


Fig.32: THD+N as a function of clock frequency

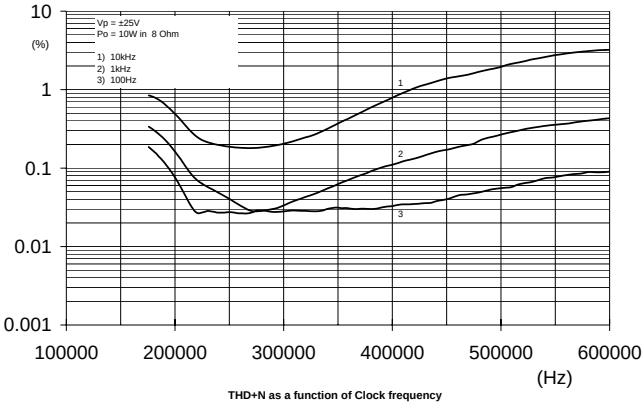


Fig.33: THD+N as a function of clock frequency

Table 2: Curves measured in the reference design

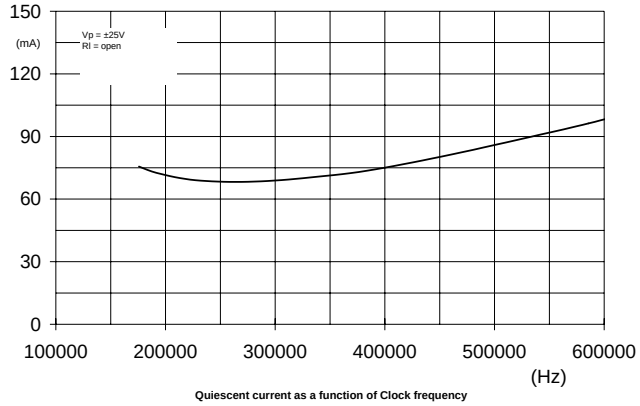


Fig.34: Quiescent current as a function of clock frequency

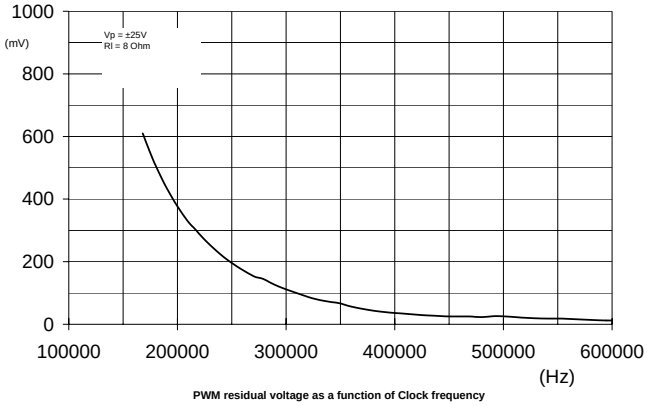


Fig.35: PWM residual voltage as a function of clock frequency

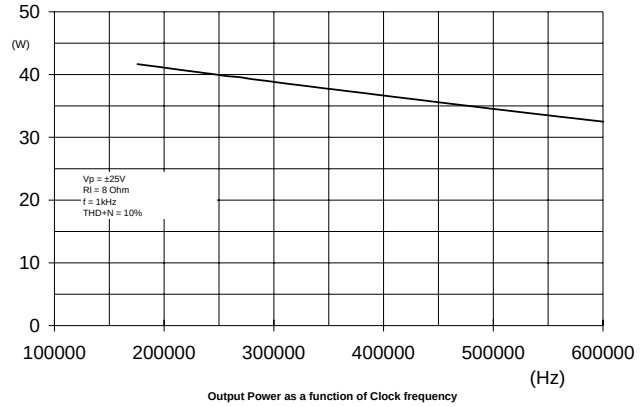
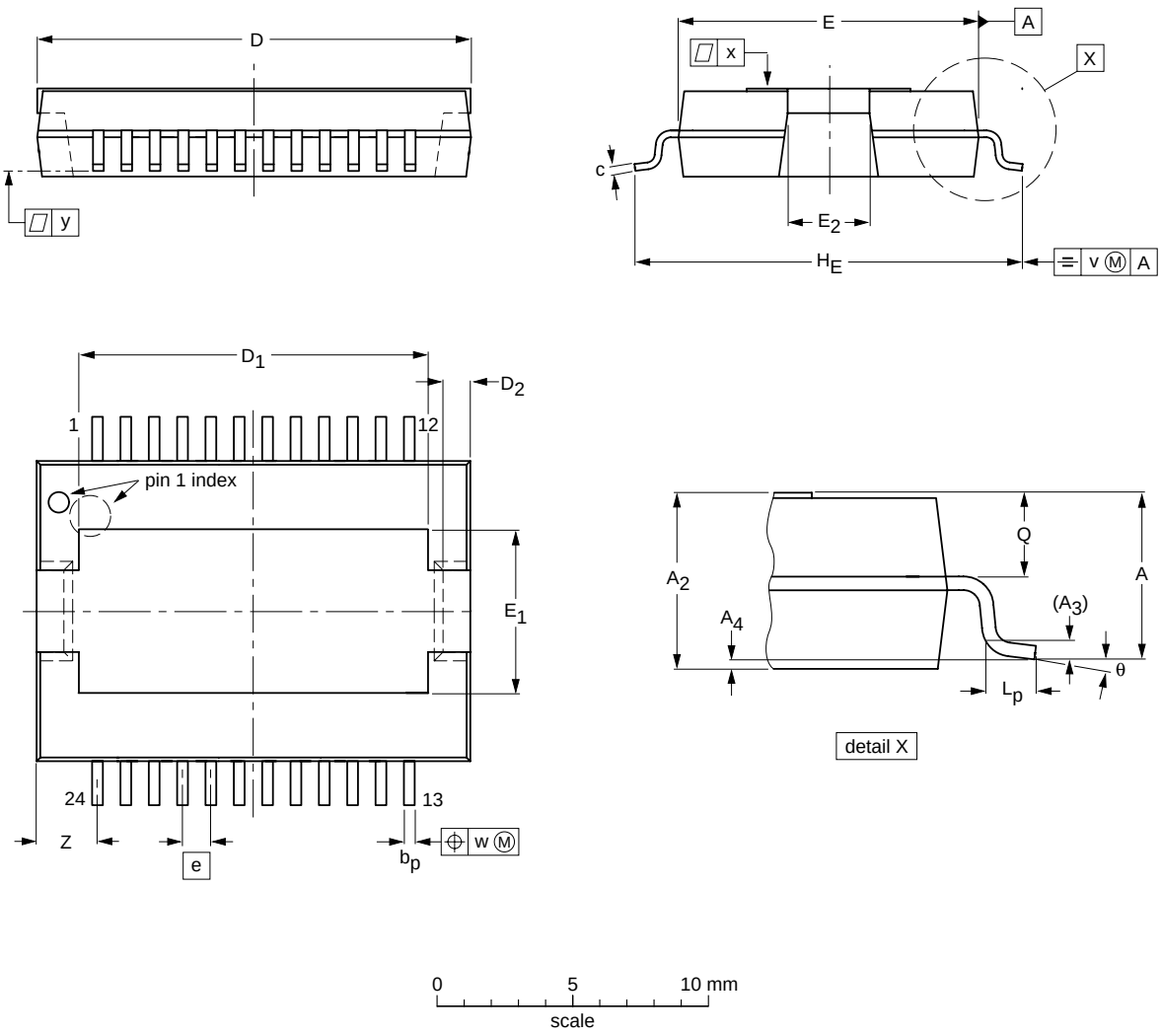


Fig.36: Output power as a function of clock frequency

16. Package outline

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.12 –0.02	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.0	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT566-2						00-03-24

17. Soldering

17.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Through-hole mount packages

17.2.1 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 C, contact may be up to 5 seconds.

17.3 Surface mount packages

17.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 C. The top-surface temperature of the packages should preferable be kept below 220 C for thick/large packages, and below 235 C for small/thin packages.

17.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45 angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 C.

17.4 Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW (1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable (2)	-	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	-
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable (3)	suitable	-
	PLCC (4), SO, SOJ	suitable	suitable	-
	LQFP, QFP, TQFP	not recommended (4), (5)	suitable	-
	SSOP, TSSOP, VSO	not recommended (6)	suitable	-

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45 angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18. Data sheet status

DATA SHEET STATUS (1)	PRODUCT STATUS (2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

19. Definitions

Short-form specification - The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition - Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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