Preliminary Data Sheet, DS1, Aug. 2003

VINETIC®-2VIP

Voice and Internet Enhanced Telephony Interface Circuit

PEB 3322 Version 1.4

Wired Communications

Never stop thinking.

Edition 2003-08-07

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Preface

This Preliminary Data Sheet describes the VINETIC®-2VIP, a member of the Voice and Internet Enhanced Telephony Interface Circuit (VINETIC®) chip set family. The VINETIC®-2VIP includes a voice processing DSP for two analog lines connected via two single-channel (or one dual-channel) SLIC chips.

Organization of this Document

This document is divided into 8 chapters. It is organized as follows:

- **Chapter 1, Family Overview**
  A general description of the chip set, key features/requirements, and typical applications.
- **Chapter 2, Pin Description**
  Pin layout and pin description.
- **Chapter 3, Hardware Behavior and Handling**
  Description of clocking, reset behavior, and test modes.
- **Chapter 4, Interface Description**
  Parallel (Intel, Motorola) and serial interfaces (PCM, SCI/SPI)
- **Chapter 5, Electrical Characteristics**
  Parameters, symbols, and limit values
- **Chapter 6, Package Outlines**
  Illustrations and dimensions of the package outlines
- **Chapter , Terminology**
  List of abbreviations and descriptions of symbols.
- **Chapter 7, Index**

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1 Family Overview

The VINETIC® is a family of devices for accessing the analog telephone line. VINETIC® devices are available in different granularity (0, 2, 4 and 8 analog voice channels) and also with different levels of DSP performance (VIP, M, C, S). The seamless connection to a broad range of SLICs provides the most effective solution for each application.

The VINETIC® performance allows the use on linecards as well as in CPE applications. Further integration on the existing boardspace is easily achieved by having an integrated DSP both for voice processing and packetization.

The VINETIC® provides system solutions for the following applications:

- Access Network:
  - Central Office - TDM
  - Digital Loop Carrier - TDM, VoATM, VoIP
  - FTTH - TDM, VoATM, VoIP
  - WLL - TDM, VoIP
- PBX:
  - Analog Linecard - TDM, VoIP
- Customer Premises Equipment:
  - Residential Gateway / Home Gateway / Internet Telephony Gateway (ITG) - VoIP
  - Integrated Access Device (IAD) - VoIP, VoATM
  - Cable Modems / Media Terminal Adapter (MTA) - VoIP
  - Analog Telephony Adapter (ATA) - VoIP

To cover these applications, the VINETIC® devices are pin- and software-compatible, allowing the maximum flexibility while offering the optimized feature set per application.

Executive Summary

The VINETIC® family integrates the necessary DSP and RAM/ROM for voice processing into the codec/SLIC chip set, thereby offering a unique set of features for voice-over-packet:

- **Cost and board space reduction** - Codec, DSP and RAM/ROM are integrated into one small package, ensuring significant cost and board space advantages.
- **Scalability** - VINETIC® supports each voice channel with the necessary amount of DSP performance due to the encapsulation of codec and DSP.
- **Flexibility** - The VINETIC® family provides two to eight analog ports and various levels of DSP performance, while remaining pin compatible (only for four or eight channels, respectively) and software compatible.
- **World-wide usage** - The VINETIC® can be adapted to different country requirements without hardware change (AC and DC path, ringing, metering, etc. are programmable).

- **Future-proof** - The integrated RAM (VINETIC®-4VIP) for downloading advanced codecs or own DSP software guarantees that the system will stay at the state-of-the-art technology also for future remote updates.
- Designed for Voice over Packet (**VoIP, VoDSL, Packetcable, VoATM**).

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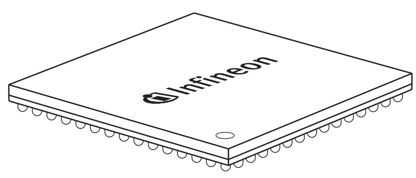
VINETIC® Voice and Internet Enhanced Telephony Interface Circuit

PEB 3322

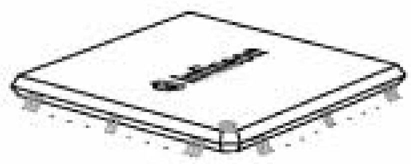
Version 1.4

1.1 Features VINETIC®-2VIP

- Fully programmable 2-channel codec with enhanced signal processing capabilities
- Glueless interface to the Infineon SLIC family: SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E, SLIC-P, and SLIC-LCP



P-LBGA-176-3



P-LQFP-176-2

1.1.1 Integrated DSP Features

- Integrated VoIP/VoDSL DSP with RAM
- Enhanced signal processing
- AAL2 and RTP/RTCP packetization
- Voice Activity Detection (VAD)
- Comfort Noise Generation (CNG)
- Algorithms for Line Echo Cancellation exceeding G.165, G.168, G.168-2000 (up to 16 ms tail length)
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (FSK) generator
- Integrated fax/modem detection, In-band tone detection
- Optimized filter structure for modem transmission, enhanced modem performance for improvement of V.90 transmission
- Multi-party conferencing
- Voice play-out (reordering, fixed and adaptive jitter buffer, clock synchronization)
- Compatible with ITU-T I.366.2 and packet cable specification
- Text-phone support V.18

Type	Package
PEB 3322	P-LBGA-176-3 or P-LQFP-176-2

1.1.2 Codec/SLIC Features

- Specification in accordance with ITU-T Recommendation G.712, ITU-T Recommendation Q.552 for interface Z and applicable LSSGR
- Internal balanced/unbalanced ringing capability of up to 85 Vrms/50 Vrms
- Sinusoidal and trapezoidal ringing (Crest factor = 1.2 - 1.6 programmable)
- External ringing support
- Programmable teletax (TTX) generation (metering)
- Programmable battery feeding with capability for driving long loops
- Ground/loop start signaling, Ground key detection
- Polarity reversal
- Message Waiting
- Automatic modes for POTS signaling and power management
- Advanced Integrated Test and Diagnostic Functions (AITDF) for local-loop monitoring and production testing
- On-hook transmission
- Power-optimized architecture with power management capability (integrated battery switches)

1.1.3 Interface Features

- PCM interface with 2 PCM highways: 8 kHz PCM transmission
- Serial control interface, SCI (Infineon) compatible, SPI compatible
- Parallel host interface: Intel/Motorola compatible
- SLIC interface compatible with DuSLIC® SLICs
- JTAG interface for boundary scan

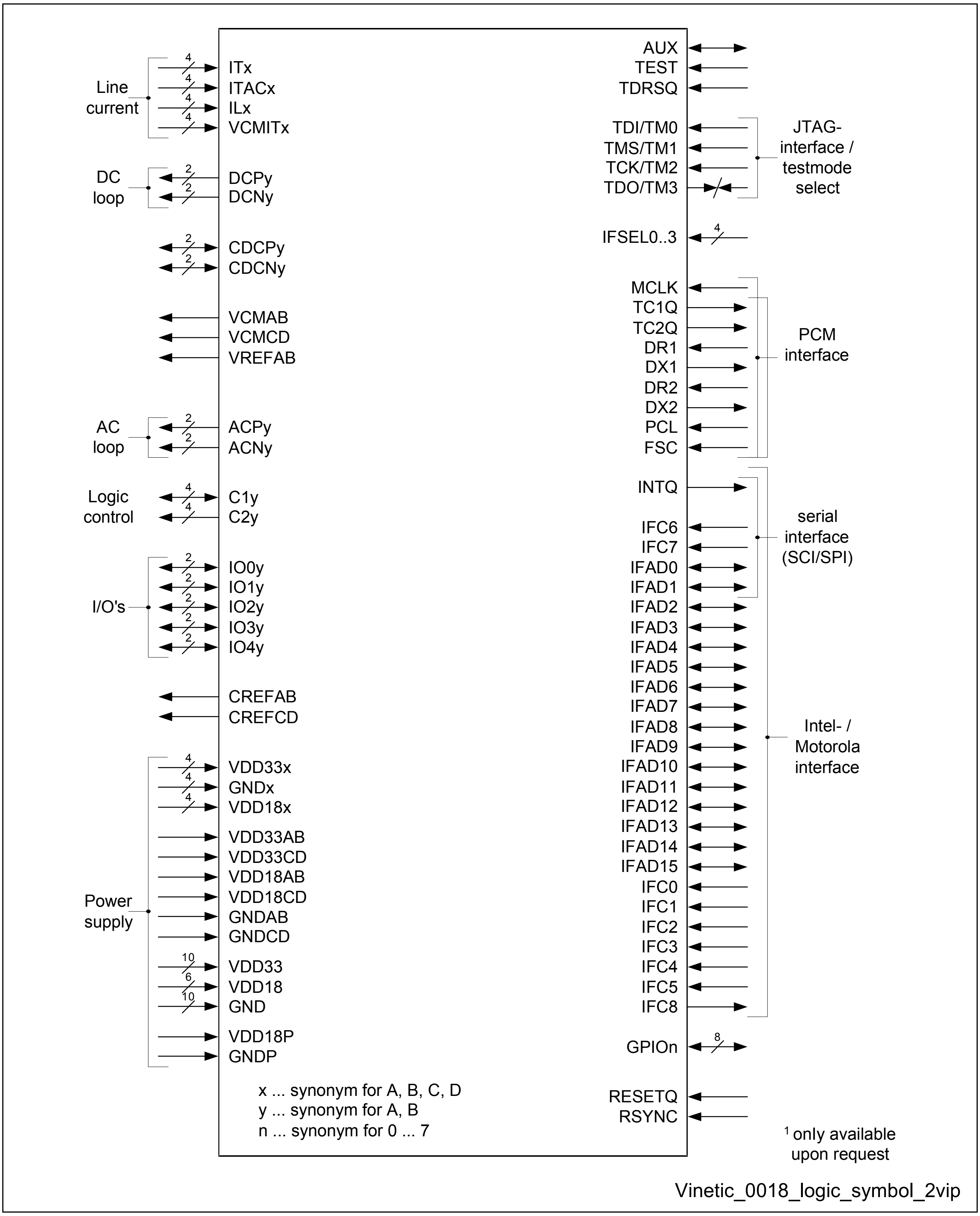


Figure 1 Logic Symbol VINETIC®-2VIP

1.2 Typical Applications

- Cable modem
- Small Office / Home Office Integrated Access Devices (SOHO-IAD) incl. (all flavors of) Digital Subscriber Line Network Termination (xDSL-NT)
- Integrated Services Digital Network Customer Premises Equipment (ISDN CPE) + Small Office / Home Office Private Branch eXchange (SOHO PBX)
- Router, Integrated Access Device (IAD), Internet Protocol Private Branch eXchange (IP-PBX)
- Next Generation Digital Loop Carrier (NG-DLC) Analog Linecard
-

2 Pin Description

2.1 P-LQFP-176-2 Pin Diagram

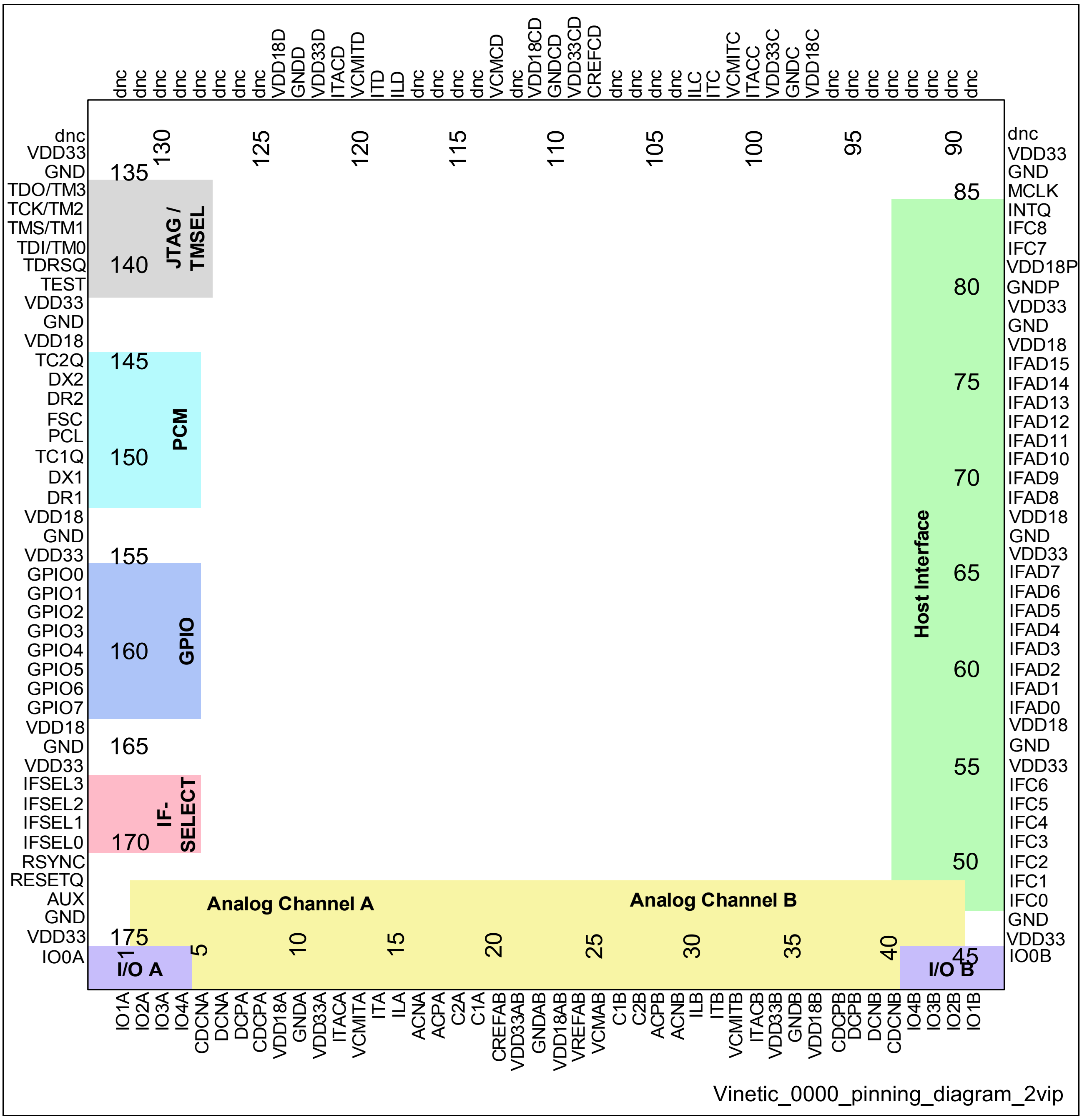


Figure 2 P-LQFP-176-2 Pin Diagram (Top View)

2.2 P-LBGA-176-3 Pin Diagram

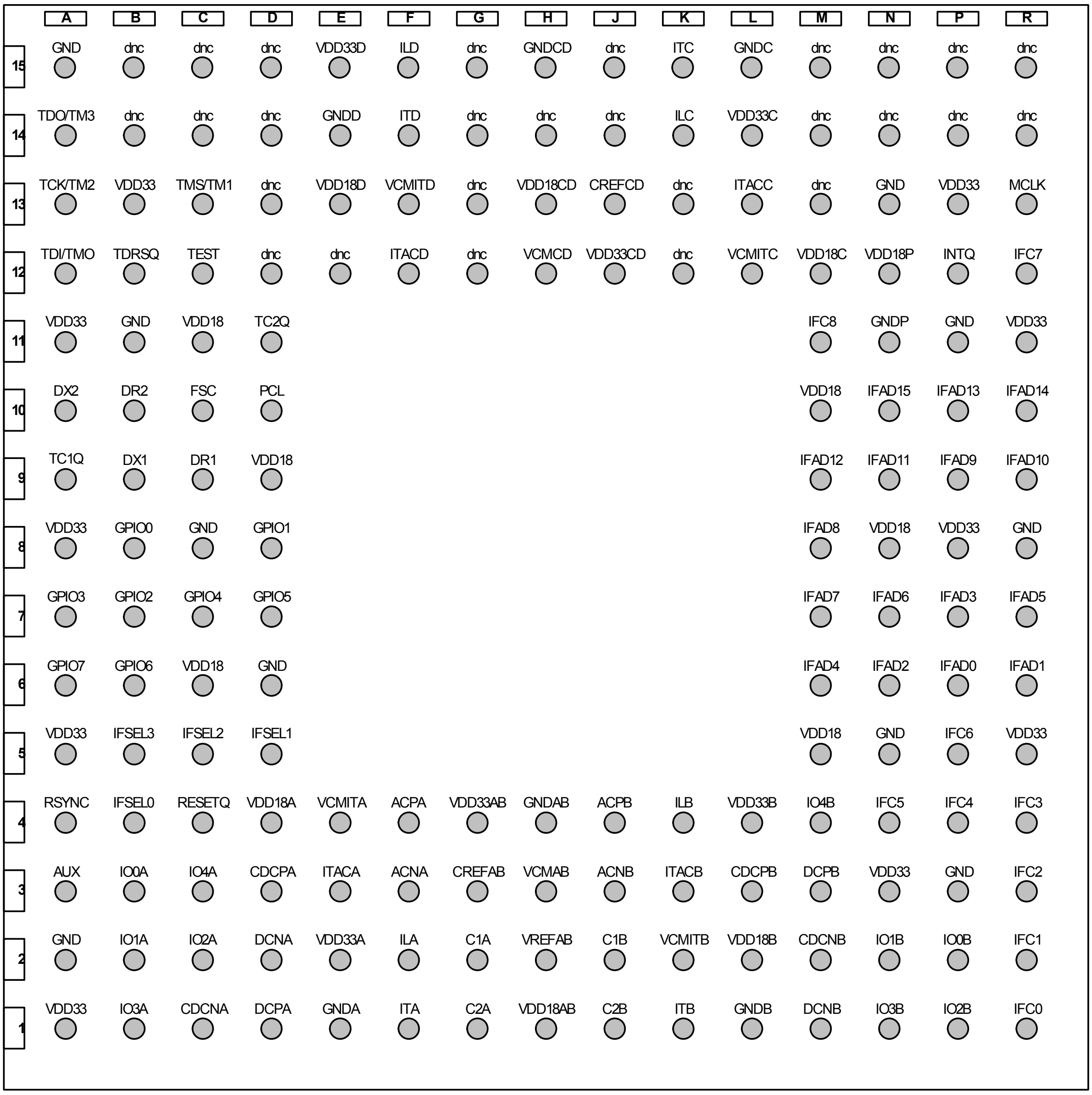


Figure 3 P-LBGA-176-3 Pin Diagram (Top View)

2.3 Pins Sorted by Function

2.3.1 Common Pins for the Analog Line Module

Table 1 Pins Analog Line Module Common

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
20 108	G3 J13	CREFAB CREFCD	I/O	Connection to external capacitor for low-pass filtering of the reference voltage
22 110	H4 H15	GNDAB GNDCD	Ground	Common ground for bias block
21 109	G4 J12	VDD33AB VDD33CD	Power	3.3 V power supply for bias
23 111	H1 H13	VDD18AB VDD18CD	Power	1.8 V power supply for bias
25 113	H3 H12	VCMAB VCMCD	O	Reference voltage for input pins ITA, ITB, ILA, ILB, ITACA, ITACB, VCMITA, VCMITB
24	H2	VREFAB	O	Reference voltage for differential two-wire interface, typically 1.5 V

2.3.2 Analog Pins

Table 2 Pins Analog Line Module

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
17 28	F4 J4	ACPA ACPB	O	Differential two-wire AC output voltage controlling the RING pin
16 29	F3 J3	ACNA ACNB	O	Differential two-wire AC output voltage controlling the TIP pin
7 38	D1 M3	DCPA DCPB	O	Two-wire output voltage (DCP)

Table 2 Pins Analog Line Module

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
6 39	D2 M1	DCNA DCNB	O	Two-wire output voltage (DCN)
8 37	D3 L3	CDCPA CDCPB	I/O	External capacitance for filtering
5 40	C1 M2	CDCNA CDCNB	I/O	External capacitance for filtering
11 34 99 122	E2 L4 L14 E15	VDD33A VDD33B DD33C VDD33D	Power	3.3 V power supply
9 36 97 124	D4 L2 M12 E13	VDD18A VDD18B VDD18C VDD18D	Power	1.8 V power supply
10 35 98 123	E1 L1 L15 E14	GNDA GNDB GNDC GNDD	Ground	Analog ground
15 30	F2 K4	ILA ILB	I	Longitudinal current input
14 31	F1 K1	ITA ITB	I	Transversal current input (AC + DC)
12 33	E3 K3	ITACA ITACB	I	Transversal current input (AC)
13 32	E4 K2	VCMITA VCMITB	I	Reference pin for transversal/longitudinal current sensing
18 27	G1 J1	C2A C2B	O	Ternary logic output controlling the SLIC operation mode
19 26	G2 J2	C1A C1B	O/I	Ternary logic output controlling the SLIC operation mode; indicating thermal overload of a SLIC if a current of typically 150 µA is drawn out of the SLICs C1 pin

Table 2 Pins Analog Line Module

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
4 41	C3 M4	IO4A IO4B	I/O	User-programmable general-purpose digital I/O pin with analog input functionality[1)]
3 42	B1 N1	IO3A IO3B	I/O	User-programmable general-purpose digital I/O pin with analog input functionality[1)]
2 43	C2 P1	IO2A IO2B	I/O	User-programmable general-purpose digital I/O pin with analog input functionality[1)]
1 44	B2 N2	IO1A IO1B	I/O	User-programmable general-purpose digital I/O pin (used for controlling the ring relay if external ringing is used)[1)]
176 45	B3 P2	IO0A IO0B	I/O	User-programmable general-purpose digital I/O pin (automatically used as output for controlling the C3 pin of the SLIC-P, except SLIC-P for extremely powersensitive applications without current limitation)[1)]
103 118	K14 F15	ILC ILD		connect to VCMCD or GND
102 119	K15 F14	ITC ITD		connect to VCMCD or GND
100 121	L13 F12	ITACC ITACD		connect to VCMCD or GND
101 120	L12 F13	VCMITC VCMITD		connect to VCMCD or GND

1) If not used, these pins should be connected to ground via a 10 kΩ resistor. If guaranteed that they are never configured as an output, these pins can directly be connected to ground.

2.3.3 Pins without Function

Table 3 Pins without Function

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
112	H14	dnc		do not connect
105 116	K12 G13	dnc dnc		do not connect
104 117	K13 G12	dnc dnc		do not connect
95 126	M14 D15	dnc dnc		do not connect
94 127	M15 D14	dnc dnc		do not connect
96 125	M13 E12	dnc dnc		do not connect
93 128	N15 D13	dnc dnc		do not connect
106 115	J14 G14	dnc dnc		do not connect
107 114	J15 G15	dnc dnc		do not connect
92 129	P15 D12	dnc dnc		do not connect
91 130	N14 C15	dnc dnc		do not connect
90 131	R15 C14	dnc dnc		do not connect
89 132	P14 B15	dnc dnc		do not connect
88 133	R14 B14	dnc dnc		do not connect

2.3.4 General Pins

Table 4 General Pins

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
172	C4	RESETQ	I	Hardware reset for the whole chip (low active)
171	A4	RSYNC	I	Ring synchronization pin for external ringing. If this pin is not used (when internal ringing is used), it should be connected to digital ground GND.
85	R13	MCLK[1]	I	Master clock for the PLL input (64*f_{FSC} to 1024*f_{FSC} in steps of 64*f_{FSC}, f_{FSC} ... frame synchronization frequency)

1) Requirements for pins MCLK, PCL and FSC see in **Chapter 3.2**.

2.3.5 General-Purpose Input/Output Pins

Table 5 General-Purpose Input/Output Pins[1]

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
156	B8	GPIO0	I/O	General-purpose I/O
157	D8	GPIO1	I/O	General-purpose I/O
158	B7	GPIO2	I/O	General-purpose I/O
159	A7	GPIO3	I/O	General-purpose I/O
160	C7	GPIO4	I/O	General-purpose I/O
161	D7	GPIO5	I/O	General-purpose I/O
162	B6	GPIO6	I/O	General-purpose I/O
163	A6	GPIO7	I/O	General-purpose I/O

1) If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. If guaranteed that it is never configured as an output, this pin can directly be connected to ground.
GPIO pins are controlled by PHI or EDSP.

2.3.6 Test-Mode Selection / JTAG (Boundary Scan) Interface Pins

Table 6 Test-Mode Selection / JTAG (Boundary Scan) Interface Pins

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
173	A3	AUX	I/O	For internal use only. Must be connected to digital ground (GND).
141	C12	TEST	I	Test mode pin (internal use only). Must be connected to digital ground GND.
140	B12	TDRSQ	I	JTAG reset. If JTAG is not used connect to digital ground for normal operation.
139	A12	TDI/TM0	I	TDRSQ=1: JTAG data input If JTAG is not used connect to digital ground.
138	C13	TMS/TM1	I	TDRSQ=1: JTAG test-mode switch If JTAG is not used connect to digital ground.
137	A13	TCK/TM2	I	TDRSQ=1: JTAG clock If JTAG is not used connect to digital ground.
136	A14	TDO/TM3	O/I	TDRSQ=1: JTAG data output If JTAG is used this pin is an output. If JTAG is not used connect to digital ground.

2.3.7 Interface-Type Selection Pins

Table 7 Interface-Type Selection Pins[1)]

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
170	B4	IFSEL0	I	Interface-select pin 0
169	D5	IFSEL1	I	Interface-select pin 1
168	C5	IFSEL2	I	Interface-select pin 2
167	B5	IFSEL3	I	Interface-select pin 3

1) see **Table 14**

2.3.8 PCM Interface Pins

Table 8 PCM Interface Pins

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
145	D11	TC2Q	O(oD)	PCM interface selected: Pin is output. Control pin for external driver for highway two of PCM interface (open drain)
146	A10	DX2	O(Z)	PCM interface selected: Data output for highway two of PCM interface (tristate)
147	B10	DR2	I	PCM interface selected: Data input for highway two of PCM interface
148	C10	FSC[1)]	I	Frame synchronization for PCM interface and PLL input
149	D10	PCL	I	Data clock for PCM interface
150	A9	TC1Q	O	PCM interface selected: Pin is output. Control pin for external driver for highway one of PCM interface (open drain)
151	B9	DX1	O(Z)	PCM interface selected: Data output for highway one of PCM interface (tristate)
152	C9	DR1	I	PCM interface selected: Data input for highway one of PCM interface

1) Requirements for pins MCLK, PCL and FSC see in **Chapter 3.2**

2.3.9 Host Interface Pins

*Note: For detailed descriptions see **Chapter 4**.*

Table 9 Host Interface Pins

Pin No.		Symb.	I/O	Intel Mux Mode	Intel Demux Mode	Motorola	SCI
P-LQFP-176-2	P-LBGA-176-3						
84	P12	INTQ (open drain)	O	INTQ	INTQ	INTQ	INTQ
48	R1	IFC0	I	GND	A1	ADDR1	GND
49	R2	IFC1	I	GND	A2	ADDR2	GND
50	R3	IFC2	I	GND	A3	ADDR3	GND
51	R4	IFC3	I	GND	A4	ADDR4	GND
52	P4	IFC4	I	RDQ	RDQ	GND	GND
53	N4	IFC5	I	WRQ	WRQ	RD/WRQ	GND
54	P5	IFC6	I	CSQ	CSQ	CSQ	CSQ
82	R12	IFC7	I	ALE	GND	GND	DCLK
83	M11	IFC8	O	RDYQ[1)]	RDYQ[1)]	RDYQ[1)]	RDYQ[1)]
58	P6	IFAD0	I/O	A0/DIO0	DIO0	DATA0	DIN[2)]
59	R6	IFAD1	I/O	A1/DIO1	DIO1	DATA1	DOUT[3)]
60	N6	IFAD2	I/O	A2/DIO2	DIO2	DATA2	GND
61	P7	IFAD3	I/O	A3/DIO3	DIO3	DATA3	GND
62	M6	IFAD4	I/O	A4[4)]/DIO4	DIO4	DATA4	GND
63	R7	IFAD5	I/O	A5[4)]/DIO5	DIO5	DATA5	GND
64	N7	IFAD6	I/O	A6[4)]/DIO6	DIO6	DATA6	GND
65	M7	IFAD7	I/O	A7[4)]/DIO7	DIO7	DATA7	GND
69	M8	IFAD8[5)]	I/O	A8[4)]/DIO8	DIO8	DATA8	GND
70	P9	IFAD9[5)]	I/O	A9[4)]/DIO9	DIO9	DATA9	GND
71	R9	IFAD10[5)]	I/O	A10[4)]/DIO10	DIO10	DATA10	GND
72	N9	IFAD11[5)]	I/O	A11[4)]/DIO11	DIO11	DATA11	GND
73	M9	IFAD12[5)]	I/O	A12[4)]/DIO12	DIO12	DATA12	GND
74	P10	IFAD13[5)]	I/O	A13[4)]/DIO13	DIO13	DATA13	GND
75	R10	IFAD14[5)]	I/O	A14[4)]/DIO14	DIO14	DATA14	GND
76	N10	IFAD15[5)]	I/O	A15[4)]/DIO15	DIO15	DATA15	GND

[1] RDYQ ... optional ready line (open source) on pin IFC8.
If used, this pin has to be connected to GND via a 560...3k3 Ω pull-down resistor, depending on the bus load.
If not used, this pin can be connected to VDD33 via a 10 kΩ pull-up resistor.

[2] If the driver for DIN signal may get high impedance, a pull up resistor of 10 kΩ should be applied.

[3] As the DOUT of the VINETIC® gets high impedance for CSQ = high level, a pull of 10 kΩ should be applied.

[4] These address pins are “don’t care”. They will not be evaluated by VINETIC® for address latching. See *Preliminary User’s Manual - Software Description* for the implemented interface protocol.

[5] In case of 8-bit interfaces, these pins can be connected to GND via a 10 kΩ pull-down resistor.

2.3.10 Digital Power/Ground Pins

Table 10 Digital Power/Ground Pins

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
57 68 77 144 153 164	M5 N8 M10 C11 D9 C6	VDD18 VDD18 VDD18 VDD18 VDD18 VDD18	Power	1.8 V power supply for the digital part
81	N12	VDD18P	Power	1.8 V power supply for the PLL. The PLL is most important for the overall performance of the chip. Special care should be taken on the filtering of the PLL supply.
46 55 66 79 87 134 142 155 166 175	N3 R5 P8 R11 P13 B13 A11 A8 A5 A1	VDD33 VDD33 VDD33 VDD33 VDD33 VDD33 VDD33 VDD33 VDD33 VDD33	Power	Digital 3.3 V power supply for I/O pads

Table 10 Digital Power/Ground Pins (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LQFP-176-2	P-LBGA-176-3			
47 56 67 78 86 135 143 154 165 174	P3 N5 R8 P11 N13 A15 B11 C8 D6 A2	GND GND GND GND GND GND GND GND GND GND	Ground	Digital ground
80	N11	GNDP	Ground	PLL Ground Connect the PLL ground to a high quality ground (see the Application Note *VINETIC-4x Layout Recommendations*).

3 Hardware Behavior and Handling

3.1 Block Diagram VINETIC®-2VIP

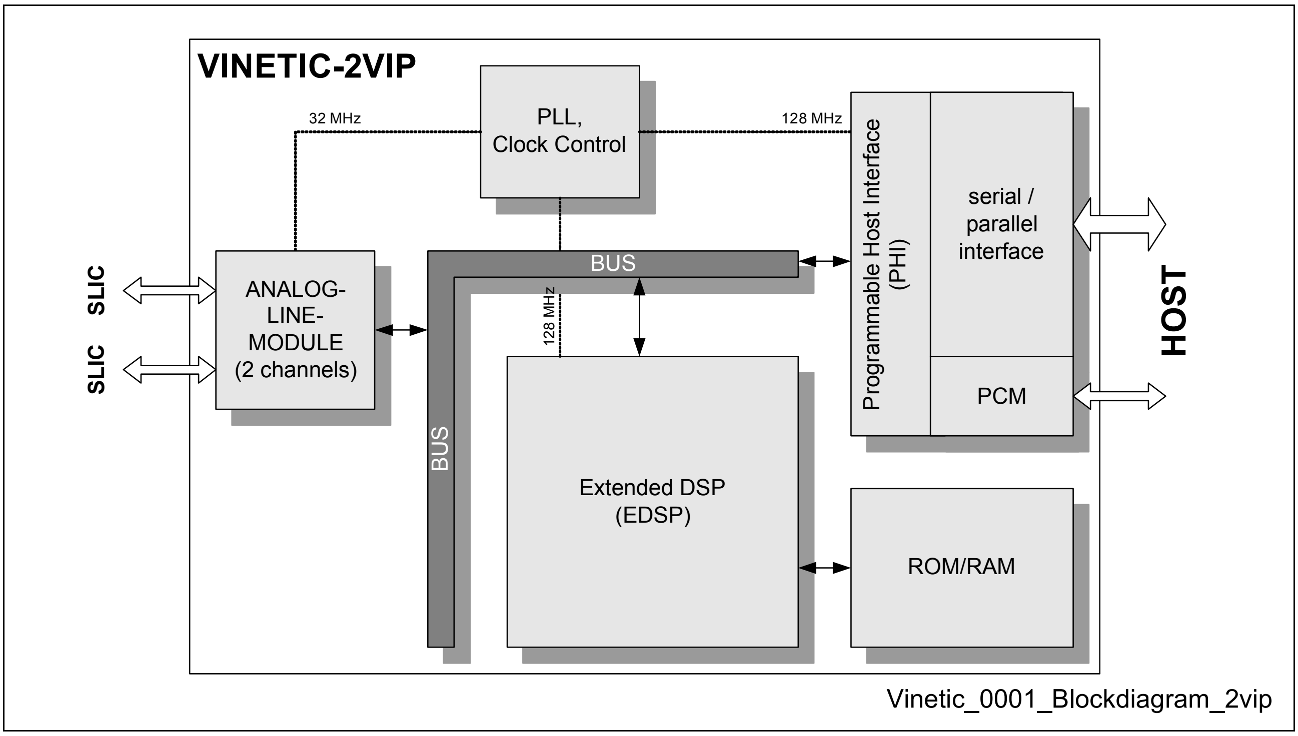


Figure 4 Block Diagram VINETIC®-2VIP

3.2 Clocking

The VINETIC®-2VIP needs at least three clocks: master clock (MCLK), frame synchronization (FSC), and PCM interface clock (PCL). All three clocks have to be provided regardless of the application. Even though the PCM interface might not be used, the clocks on FSC, MCLK, PCL have to be provided at all times to ensure operation of the device.

The Master clock MCLK has to be phase-locked to PCM interface clock PCL and frame synchronization FSC. It is recommended to directly connect MCLK and PCL.

The frame synchronization has to fulfill the specification as described in **"PCM Interface" on Page 49**.

Clock failure bits (see **Figure 6**) of the VINETIC®-2VIP are able to indicate a clock synchronization problem. The bit SYNC-FAIL detects a clock divider synchronization failure and the bit MCLK-FAIL reports a PLL synchronization failure (see *Preliminary User's Manual - Software Description*, register HWSR1).

Table 11 Clocks

Pin	Description	Frequency
MCLK	Master clock (mandatory). Has to be phase-locked to FSC and PCL. It is recommended to connect the MCLK pin with the PCL pin. For timing requirements of the MCLK signal refer to**Table 12**.	$64*f_{FSC}$ to $1024*f_{FSC}$ in steps of $64*f_{FSC}$
FSC	Frame synchronization (mandatory), Synchronizes internal clocks and voice interface.	f_{FSC} =8 kHz
PCL (PCM)	Clock for voice (PCM) interface (mandatory), If MCLK and PCL are connected, only multiples of 512 kHz are allowed.	PCM: 256 kHz to 8.192 MHz depending on the number of time slots, see **Table 24 "on Page 51**.
TCK	Clock for boundary scan controller (optional)	1 MHz to 10 MHz

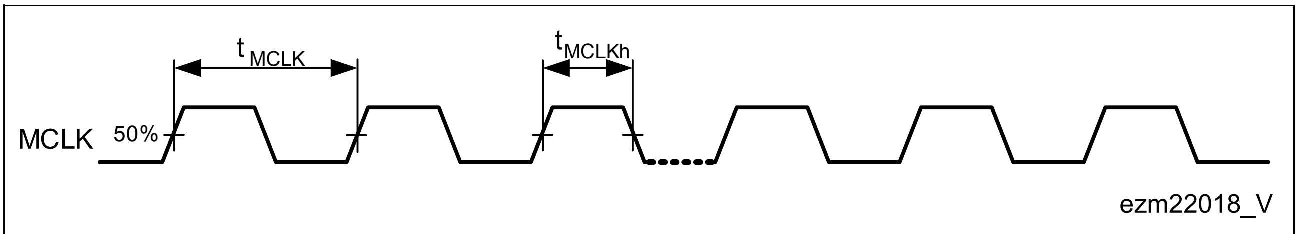


Figure 5 Timing Requirements MCLK

Table 12 Timing Requirements MCLK

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
Period MCLK[1]	t_{MCLK}	1/8192		1/512	ms
MCLK high time	t_{MCLKh}	$0.4 \times t_{MCLK}$		$0.6 \times t_{MCLK}$	µs
MCLK jitter phase noise density 1 kHz frequency offset		–	–	-80	dBc[2]/ Hz

[1] The MCLK frequency must be an integer multiple of the FSC frequency ($n*8*f_{FSC}$, n = 4..128).

[2] dBc = dB carrier.

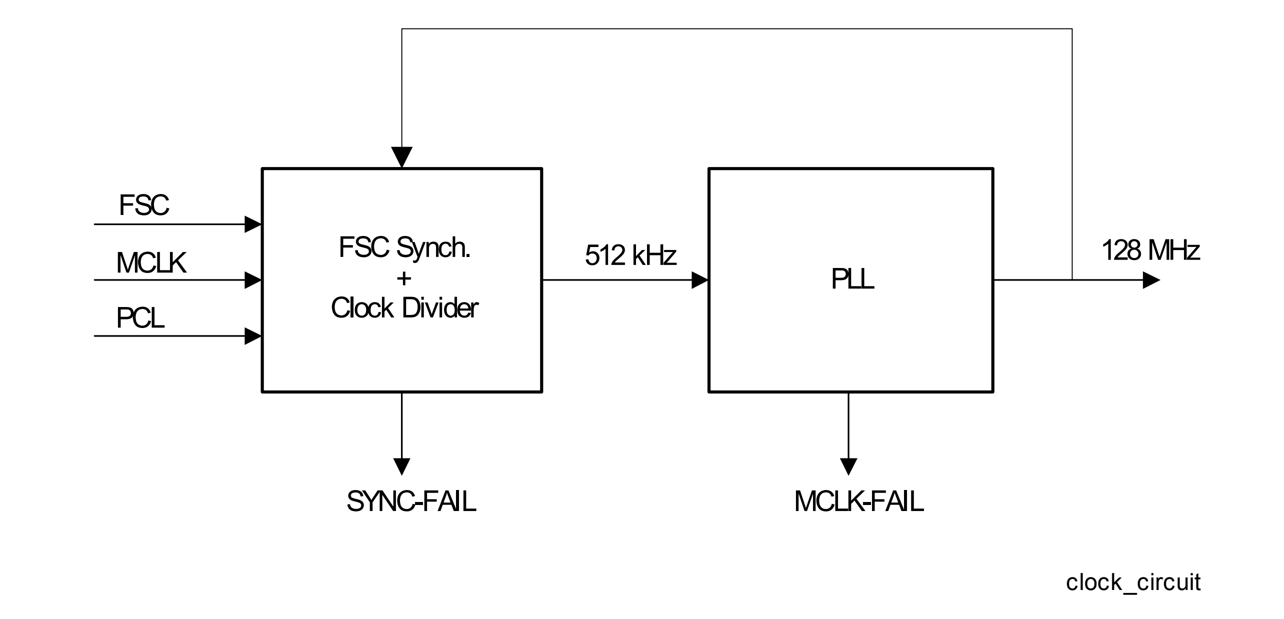


Figure 6 Clock Fail Bits

3.3 Reset

A hardware reset of the VINETIC®-2VIP is initiated by a power-on reset or by a hardware reset. A hardware reset requires setting the signal at the RESETQ input pin to low-level for at least 4 µs. The reset input pin has a spike rejection that will safely suppress spikes with a duration of less than 1 µs.

By pulling the RESETQ input pin to low, the chip will be reset (see **Figure 7 "VINETIC® Reset Sequence" on Page 30**) and the following actions will take place:

- All I/O pins are deactivated.
- All outputs are inactive (e.g. DX1/DX2).
- The internal PLL is stopped.
- Internal clocks are deactivated.
- The chip is in a Reset State. All analog Bias Voltages are switched off.

With the rising edge of the reset signal all external clocks need to be already stable, then the following actions will take place:

- Clock detection
- PLL synchronization
- The reset routine runs
- After the reset routine has finished, an interrupt is generated and the RESET bit in the ISR register is set.
- The EDSP will stay in boot state (see *Preliminary User's Manual - Software Description*, Chapter 3)
- The ALM Modules (Analog Channels) will go to the PDH (Power Down High Impedance) mode.

- The internal reset routine requires approximately 12 frames (12 × 125 µs = 1.5 ms) to be finished (including PLL start-up and clock synchronization).
- First access to the VINETIC® is possible after the INTQ signal = 0.

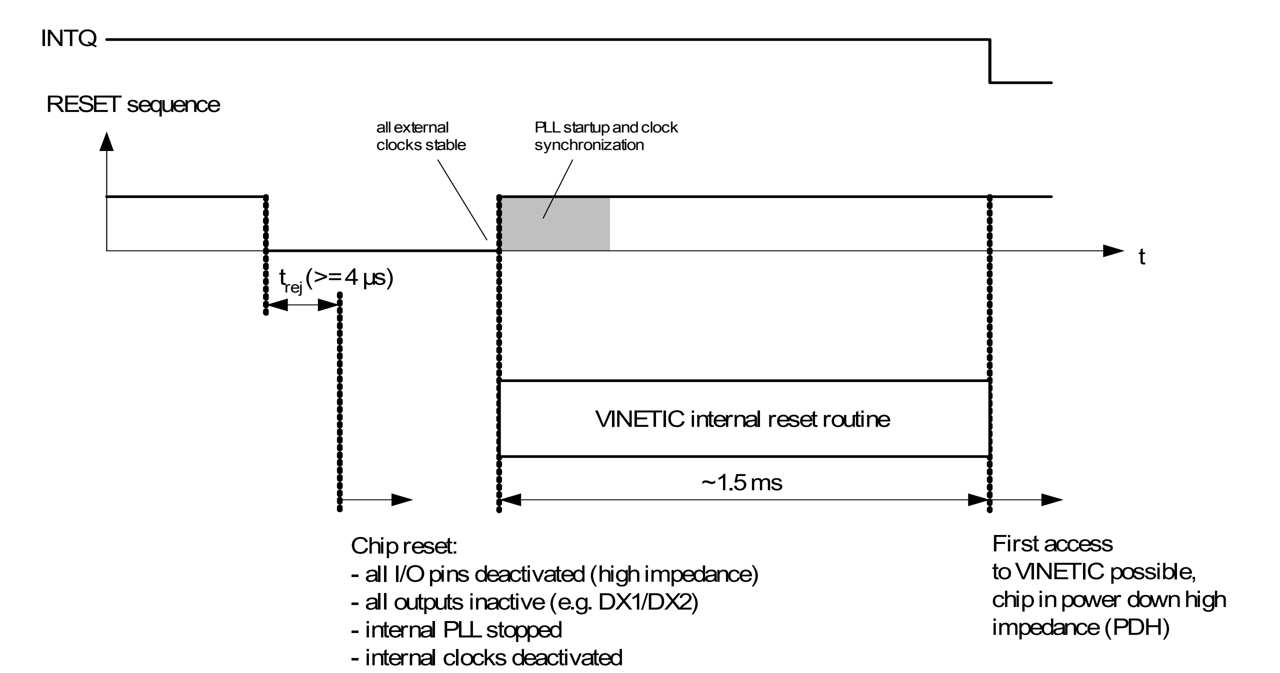


Figure 7 VINETIC® Reset Sequence

Figure 7 “VINETIC® Reset Sequence” on Page 30 shows the Reset sequence for either internal power-on reset or signal at RESETQ pin.

3.4 Power-On Reset

The internal power-on reset is only dependent on the 1.8 V digital power supply pins VDD18. The reset routine is running during power-on reset as well as during an external reset signal. The VINETIC®-2VIP will notify a reset by setting the RESET bit in the ISR. As the power-on reset should not be the regular way of resetting the VINETIC®-2VIP, it is recommended to perform a regular reset (via the RESETQ pin) after the 3.3 V and the 1.8 V supplies have been applied (the supply voltage 3.3 V should be applied before the supply voltage 1.8 V; see *Chapter 5.2.3*).

3.5 Test Modes of the VINETIC®-2VIP

The VINETIC®-2VIP can be set to different production and analysis test modes. The selection of the individual test is done with the test-mode selection pins TM0 to TM3 or via the JTAG interface and the test-enable pin TEST. Since the VINETIC®-2VIP shares the TM pins with the JTAG pins, four possibilities of test-mode selection are available.

Table 13 VINETIC®-2VIP Test Modes

Pins		Mode	Description
TEST	TDRSQ		
0	0	Normal operation	Normal operation of the chip (customer mode)
0	1	JTAG	JTAG operation (boundary scan)
1	0	TM-Test	for internal use only
1	1	TM-JTAG	for internal use only

3.5.1 Boundary Scan Test

The boundary scan test (BST) is a standardized method for testing boards, providing also a standard interface to communicate with test circuits on an IC as the VINETIC®-2VIP. The boundary scan standard specifies a four wire interface using the four signals TDI, TDO, TCK and TMS. Additionally, an optional test reset signal TDRSQ can be integrated.

These four (five) dedicated signals, the test access port (TAP), are connected to the TAP controller inside the VINETIC. The TAP controller is a state machine clocked with the rising edge of TCK and the state transitions are controlled by TMS. The VINETIC®-2VIP provides a fully IEEE 1149.1 compliant boundary scan support consisting of:

- Complete Boundary Scan
- A test access port controller (TAP controller)
- Five dedicated pins: TCK, TMS, TDI, TDO and a TRST to asynchronously reset the TAP controller
- Boundary Scan Description Language (BSDL) supplied

Boundary Scan Description Language (BSDL) is a standard way to describe the features and behavior of an IC like the VINETIC®-2VIP , that includes IEEE 1149.1 boundary scan. It is also a standard way to pass information to test-generation software.

3.6 Using a DMA

It is possible to read/write data from/to the VINETIC®-2VIP with one single DMA transfer. It is recommended to connect the address lines of the host to the address lines of the VINETIC®-2VIP as shown in the example in **Figure 8** (see also *Preliminary User's Manual - Software Description*).

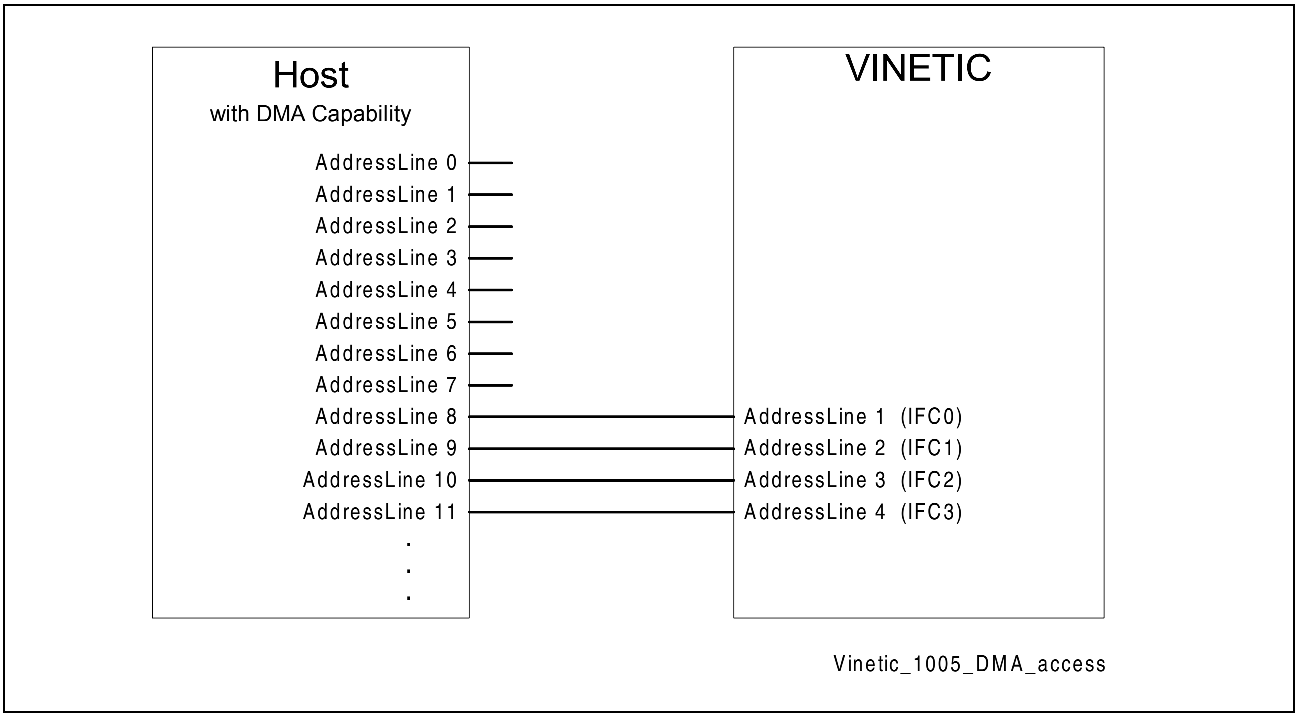


Figure 8 Connecting the Address Lines of Host and VINETIC®-2VIP

4 Interface Description

The digital interfaces of the VINETIC® are operated by a programmable host interface controller (PHI) and allow flexible and easy adaptation to various interfaces. For programming the VINETIC® and performing data/packet transfer from/to the VINETIC®, a parallel interface or a serial microcontroller interface can be used. Additionally, VINETIC® has an interface to PCM data. Certain interface types require a PHI download (for more information see the *PHI Download Status Sheet*).

VINETIC® 8/16-bit Parallel Interfaces

– The parallel interface can be operated in Intel 8/16-bit mode (multiplexed/ demultiplexed) or in 8/16-bit Motorola mode.

VINETIC® Serial Interfaces

– The VINETIC® serial microcontroller interface (µC interface = SCI) is compatible with the Motorola SPI and is electrically compatible with DuSLIC®. The PCM interface has 2 PCM highways and can be operated together with the serial µC interface or the parallel interface.

The VINETIC®-2VIP supports the widely used microcontrollers: e.g. MPC850, MPC860, MPC8260, C165UTAH, MIPS and ARM derivatives, etc..

All parallel and serial interfaces (host interfaces) use the same (multiplexed) pins. The desired interface type is selected by means of pin strapping with the pins IFSEL0, IFSEL1, IFSEL2 and IFSEL3.

Note: Host interface and PCM interface can be used in parallel.

Table 14 shows the possible interface configurations:

Table 14 Interface Configurations

No.	Interface Type	IFSEL3	IFSEL2	IFSEL1	IFSEL0
1	for future use	0	0	0	0
2	SCI[1)] (DuSLIC®) (serial) + PCM	0	0	0	1
3	8-bit INTEL multiplexed mode + PCM	0	0	1	0
4	8-bit INTEL demultiplexed mode + PCM	0	0	1	1
5	8-bit MOTOROLA mode + PCM	0	1	0	0
6	for future use	0	1	0	1
7	for future use	0	1	1	0
8	for future use	0	1	1	1
9	for future use	1	0	0	0

Table 14 Interface Configurations (cont'd)

No.	Interface Type	IFSEL3	IFSEL2	IFSEL1	IFSEL0
10	for future use	1	0	0	1
11	16-bit INTEL multiplexed mode + PCM	1	0	1	0
12	16-bit INTEL demultiplexed mode + PCM	1	0	1	1
13	16-bit MOTOROLA mode + PCM	1	1	0	0
14	for future use	1	1	0	1
15	for future use	1	1	1	0
16	for future use	1	1	1	1

1) compatible with Motorola SPI slave mode

Note: FSC, PCL and MCLK always have to be supplied even if no PCM interface is used.

Input/Output Waveform for AC Interface Timing Characteristics

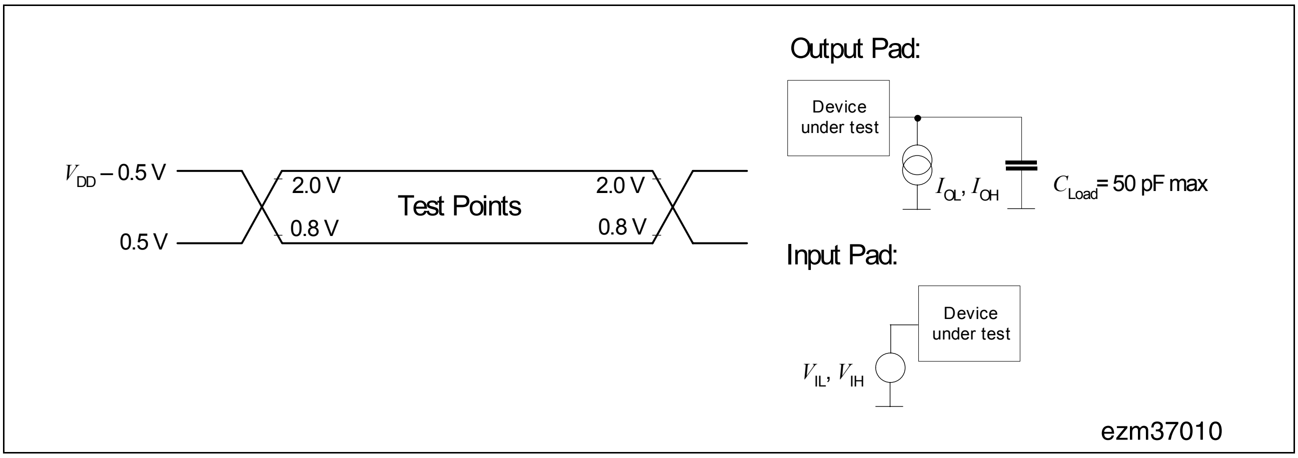


Figure 9 Waveform for AC Tests

During AC-Testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V. The CMOS outputs are measured at 0.5 V and V_{DD} – 0.5 V respectively.

4.1 Intel/Motorola-Mode Parallel Interfaces

4.1.1 Control for Intel/Motorola-Interfaces

Table 15 gives an overview about the address coding. VINETIC®-2VIP latches in four address bits. In the demultiplexed interface mode the address information is taken from pins IFC0, IFC1, IFC2 and IFC3 (host processors that only put out even addresses on their address bus must be connected shifted, i.e. address lines A1 - A4 instead of A0 - A3 must be connected to the respective VINETIC®-2VIP address pins).
In the multiplexed address mode the address information is taken from the pins IFAD0, IFAD1, IFAD2 and IFAD3. In this mode the EOM coding is changed in order to allow also the connection to processors that only put out even addresses.

Table 15 VINETIC®-2VIP Address Coding

Demux Mode	Intel Mux Mode	Description
IFC3..IFC0	IFAD3..IFAD0	
0000	0000	Reserved
0001	0001	Reserved
0010	0010	NWD (Next Word): Indicates that the next word (data or a command word) is following (optional). This indication will not be checked by the PHI.
0011	0100	EOM (End Of Message): Indicates the last data or command word.
. . .	. . .	Reserved
1100	1100	DIA (Direct ISR register Access): By applying this address and a read signalization on the control lines the ISR (including the RDYQ bit) will be returned immediately without recovery time restriction (always accessible). This signaling is needed if SW handshake is used.
. . .	. . .	Reserved
1111	1111	Reserved

4.1.2 Pinning Intel Interface

Table 16 Intel Interface Pins

Interface Name	Pin Name	Function	Input (I) Output (O) High Imp. (Z)
ALE	IFC7	Address latch enable (Mux mode only)	I
CSQ	IFC6	Chip select input, start of data transfer with WRQ/RDQ (active low)	I
WRQ	IFC5	Data-strobe input write (active low)	I
RDQ	IFC4	Data-strobe input read (active low)	I
RDYQ	IFC8	Ready line (active low) (open source)	O
A[4:1]	IFC3..0	Address lines (only Demux mode)	I
DIO[7:0]	IFAD7..0[1)]	Data bus/8-bit mode (Demux mode) Address or Data bus/8-bit mode (Mux mode)	I/O/Z
DIO[15:0]	IFAD15..0	Data bus/16-bit mode (Demux mode) Address or Data bus/16-bit mode (Mux mode)	I/O/Z

1) In case of 8-bit mode the pins IFAD8...IFAD15 can be connected to GND via a 10 kΩ pull-down resistor (in this case the pins must not be connected directly to GND or 3.3 V).

4.1.3 Timing Intel Demux Mode

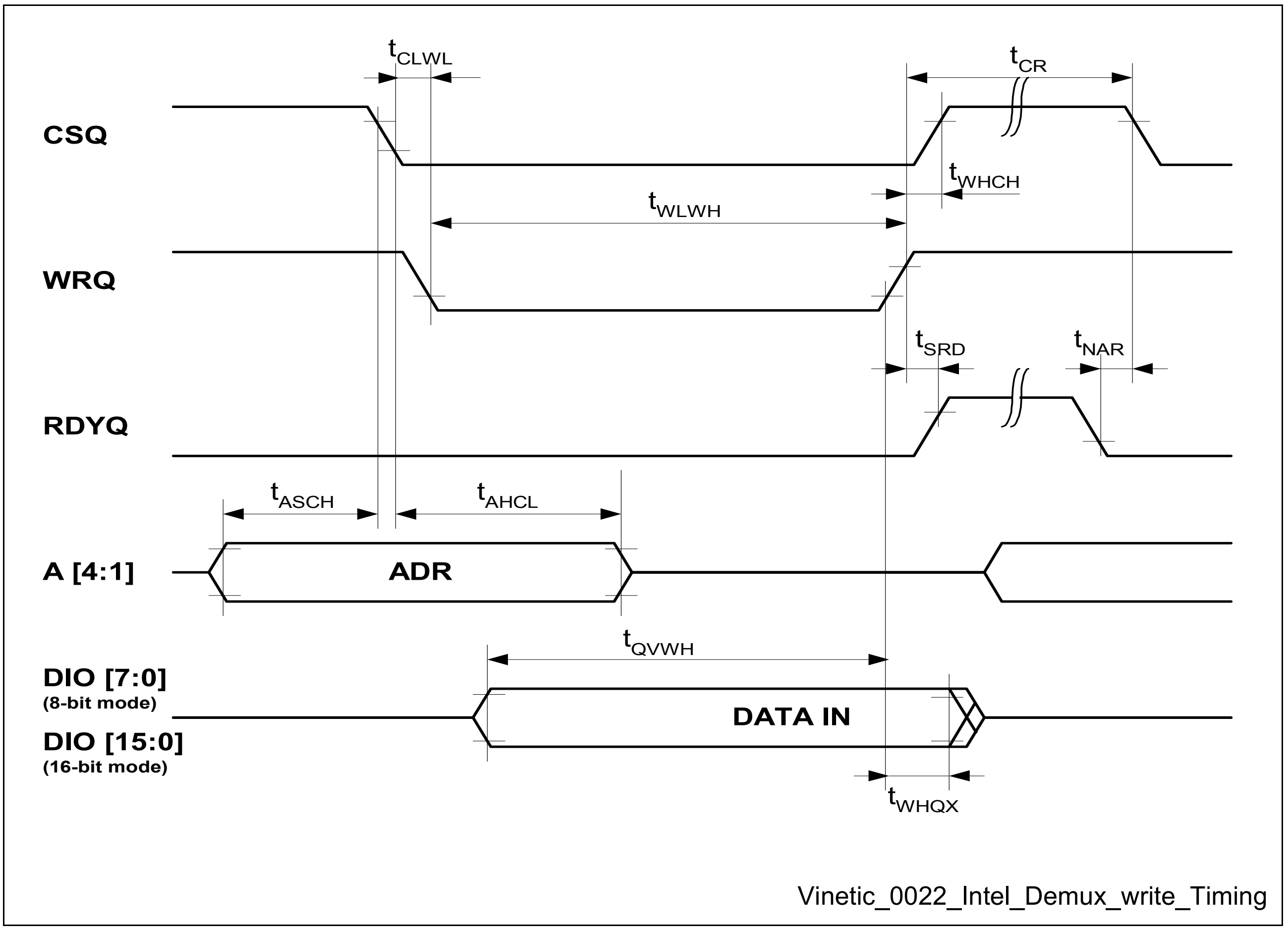


Figure 10 Write Access, Intel Demux Mode

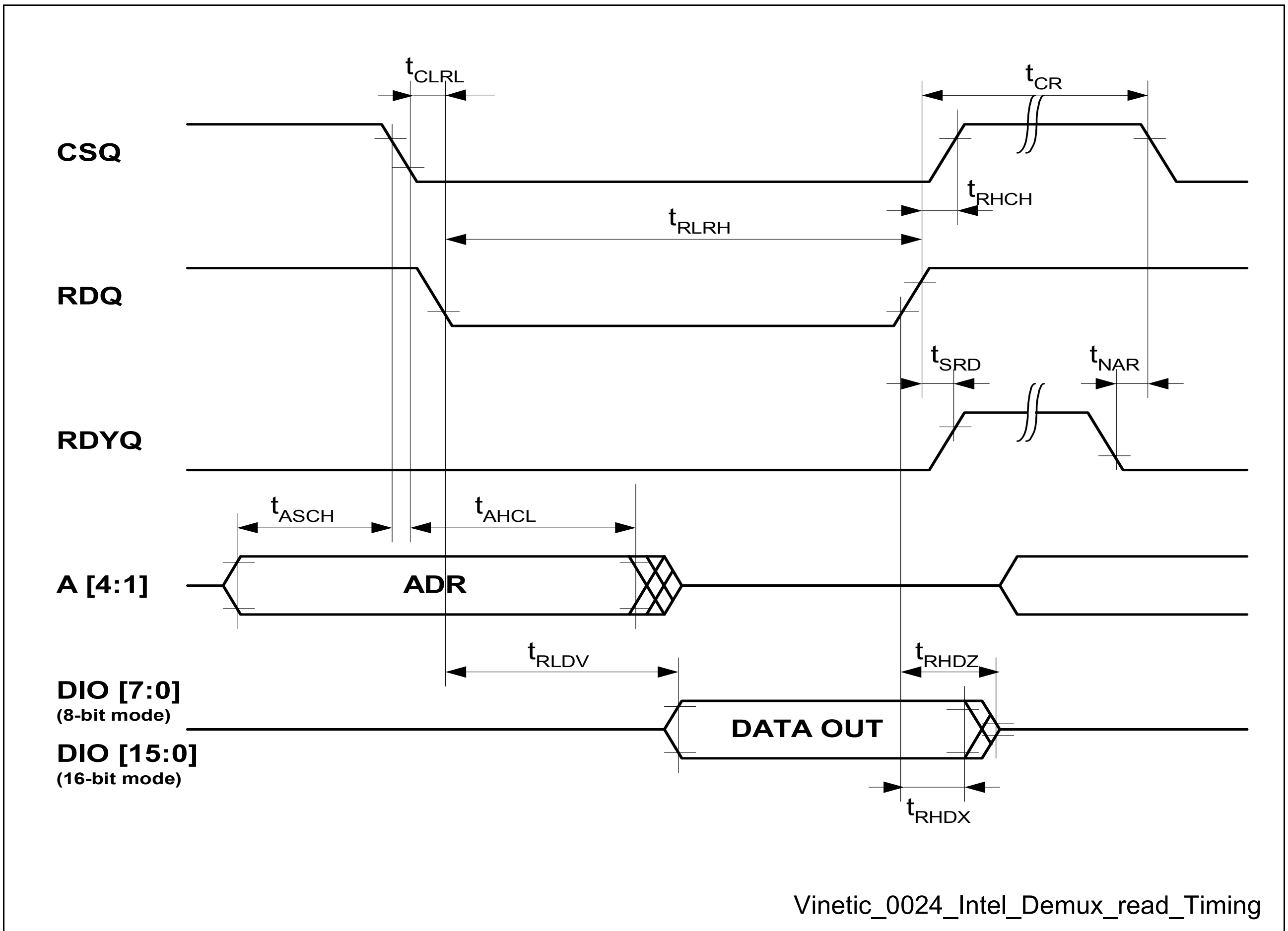


Figure 11 Read Access, Intel Demux Mode

4.1.4 Timing Intel Mux Mode

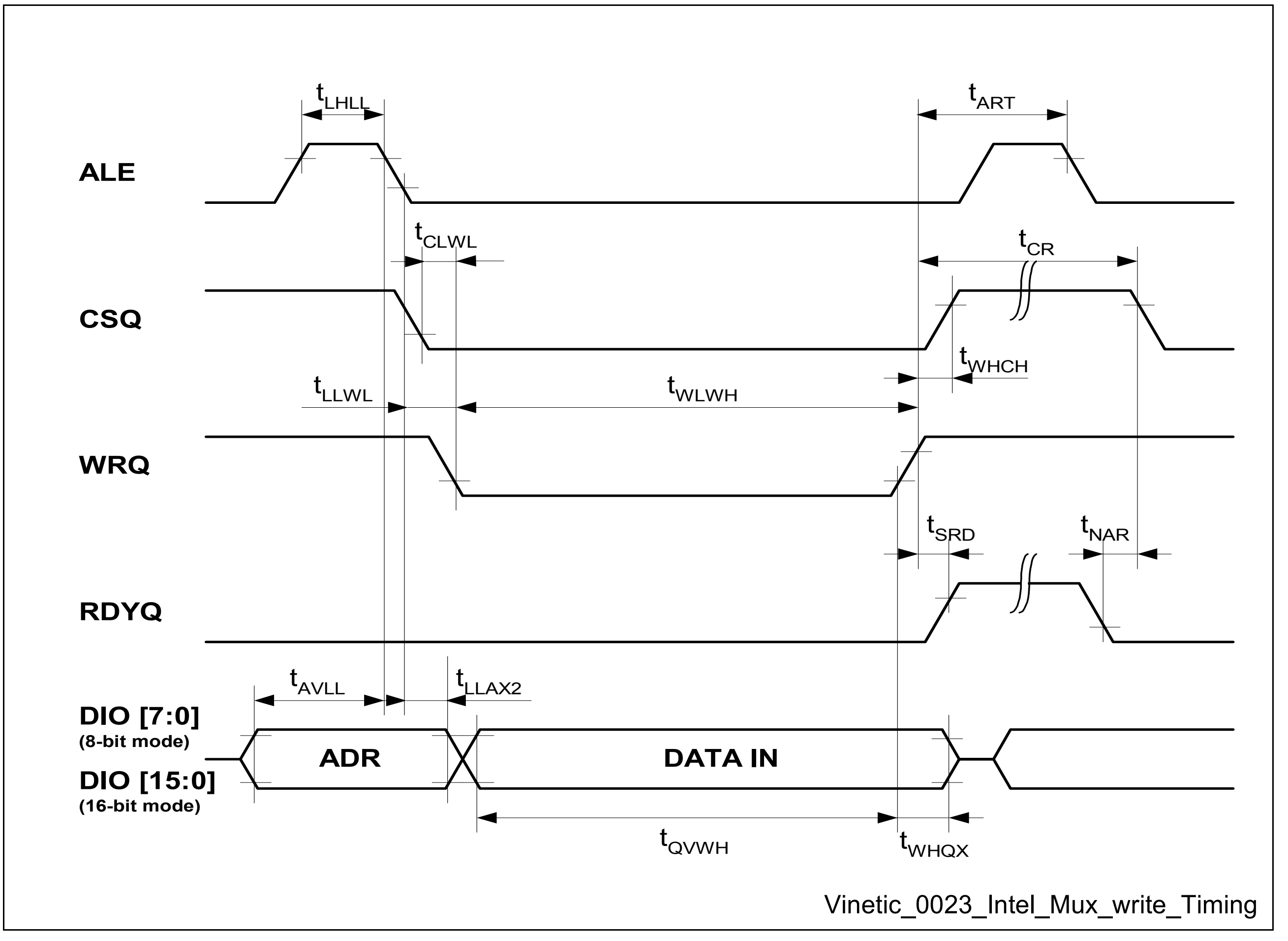


Figure 12 Write Access, Intel Mux Mode

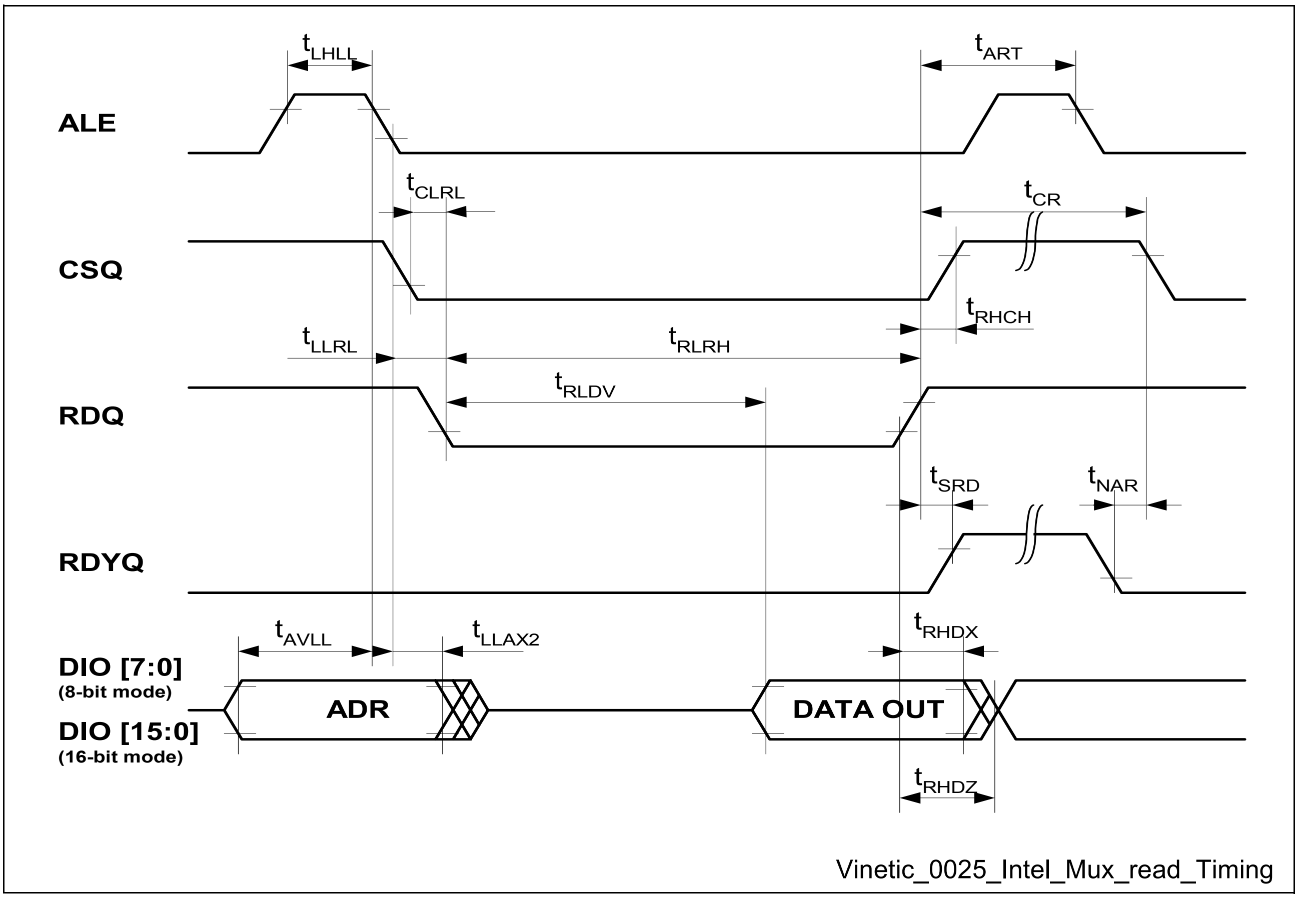


Figure 13 Read Access, Intel Mux Mode

Table 17 Timing Specification Intel Mux/Demux Mode

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
ALE high time	t_{LHLL}	20	–	ns
Address setup to ALE	t_{AVLL}	10	–	ns
Address hold after ALE inactive	t_{LLAX2}	10	–	ns
Address recovery time	t_{ART}	50	–	ns
Address setup to CSQ	t_{ASCH}	10	–	ns
Address hold after CSQ	t_{AHCL}	10	–	ns
RD active to valid data out	t_{RLDV}	–	30	ns
Data hold after RD inactive	t_{RHDX}	3	–	ns
Data float after RD inactive	t_{RHDZ}	–	35	ns
Data setup before WR inactive	t_{QVWH}	20	–	ns
Data hold after WR inactive	t_{WHQX}	5	–	ns

Table 17 Timing Specification Intel Mux/Demux Mode (cont'd)

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
RDQ active after ALE inactive	t_{LLRL}	20	–	ns
WRQ active after ALE inactive	t_{LLWL}	0	–	ns
RD pulse width	t_{RLRH}	50	–	ns
WR pulse width	t_{WLWH}	50	–	ns
CS low to WR low[1)]	t_{CLWL}	0	–	ns
WR high to CS high[1)]	t_{WHCH}	0	–	ns
CS low to RD low[1)]	t_{CLRL}	0	–	ns
RD high to CS high[1)]	t_{RHCH}	0	–	ns
Next access after interface ready	t_{NAR}	65[2)]	–	ns
Strobe signal to RDYQ delay time	t_{SRD}	–	125[3)]	ns
Command recovery time	t_{CR}	1350[4)]	–	ns

1) These parameters are for reference only, they can also be negative. The control inputs RDQ and WRQ are gated internally with CSQ. If the active CSQ is shorter (embedded), the active RDQ or WRQ always refer to the resulting gated signal.

2) If the PCM interface is not used, this time is 35 ns.

3) If the PCM interface is not used, this time is 95 ns.

4) If the PCM interface is not used, this time is 670 ns.

4.1.5 Pinning Motorola Interface

According to MPC850, MPC860, MPC8260 and to M68HCxx and M683xx family.

Table 18 Motorola Interface Pins

Interface Name	Pin Name	Function	Input (I) Output (O) High Imp. (Z)
ADDR[4:1]	IFC3..0	Address lines	I
DATA[15:0]	IFAD15..0	Data bus/16-bit mode, tristate	I/O/Z
DATA[7:0]	IFAD7..0[1)]	Data bus/8-bit mode, tristate	I/O/Z
CSQ	IFC6	Chip select, data strobe (for Motorola 16-bit mode) with RD/WRQ (active low)	I
RD/WRQ	IFC5	Read / write, data-strobe signal. (read →active high, write → active low)	I

Table 18 Motorola Interface Pins (cont'd)

Interface Name	Pin Name	Function	Input (I) Output (O) High Imp. (Z)
RDYQ	IFC8	Ready line (active low) (open source)	O
CLKOUT	no pin	Reference clock, not used	not used

1) In case of 8 bit mode the pins IFAD8...IFAD15 should be connected to GND via a 10 kΩ pull-down resistor (in this case the pins must not be connected directly to GND or 3.3 V).

4.1.6 Timing Motorola Interface

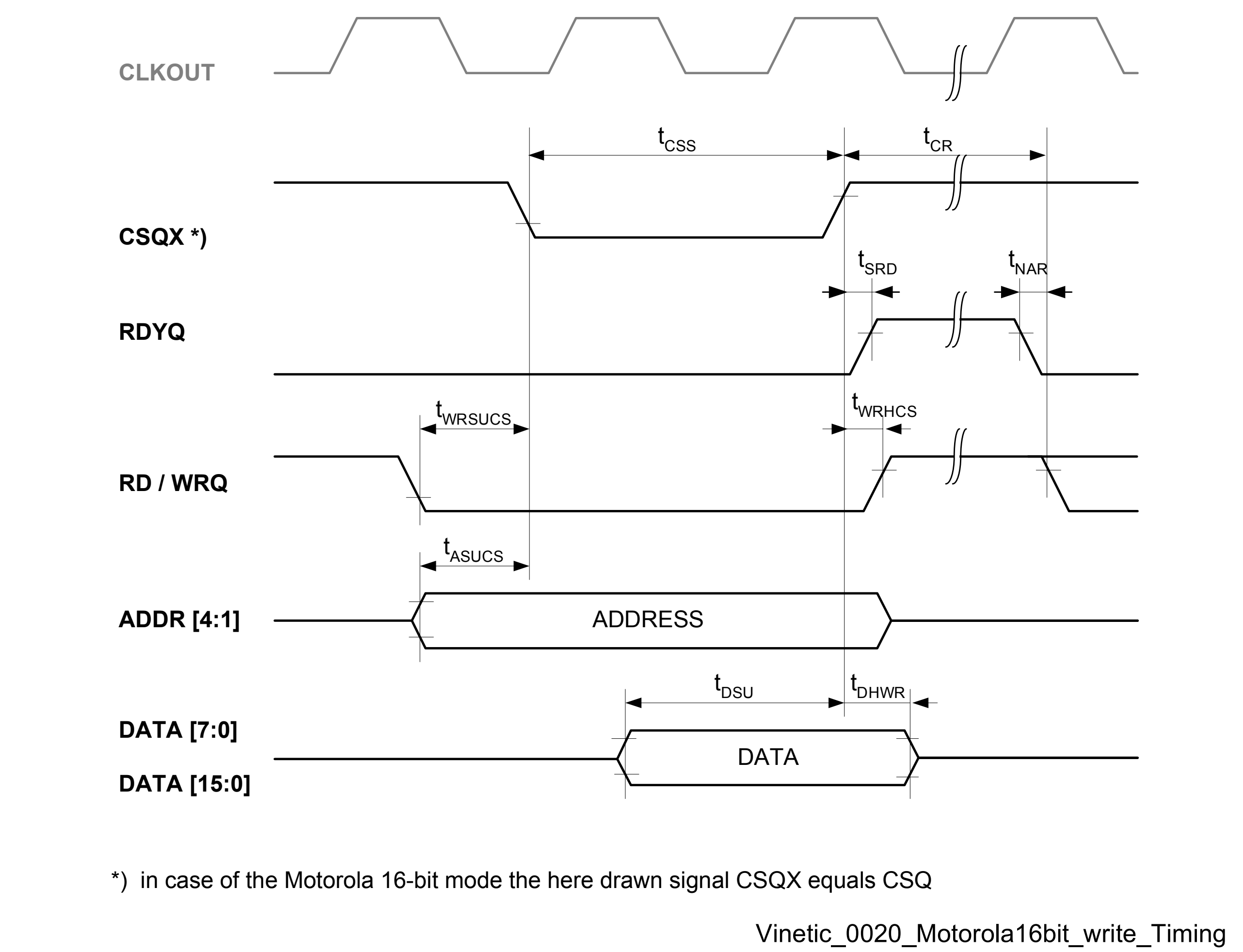


Figure 14 Write Access, Motorola Mode

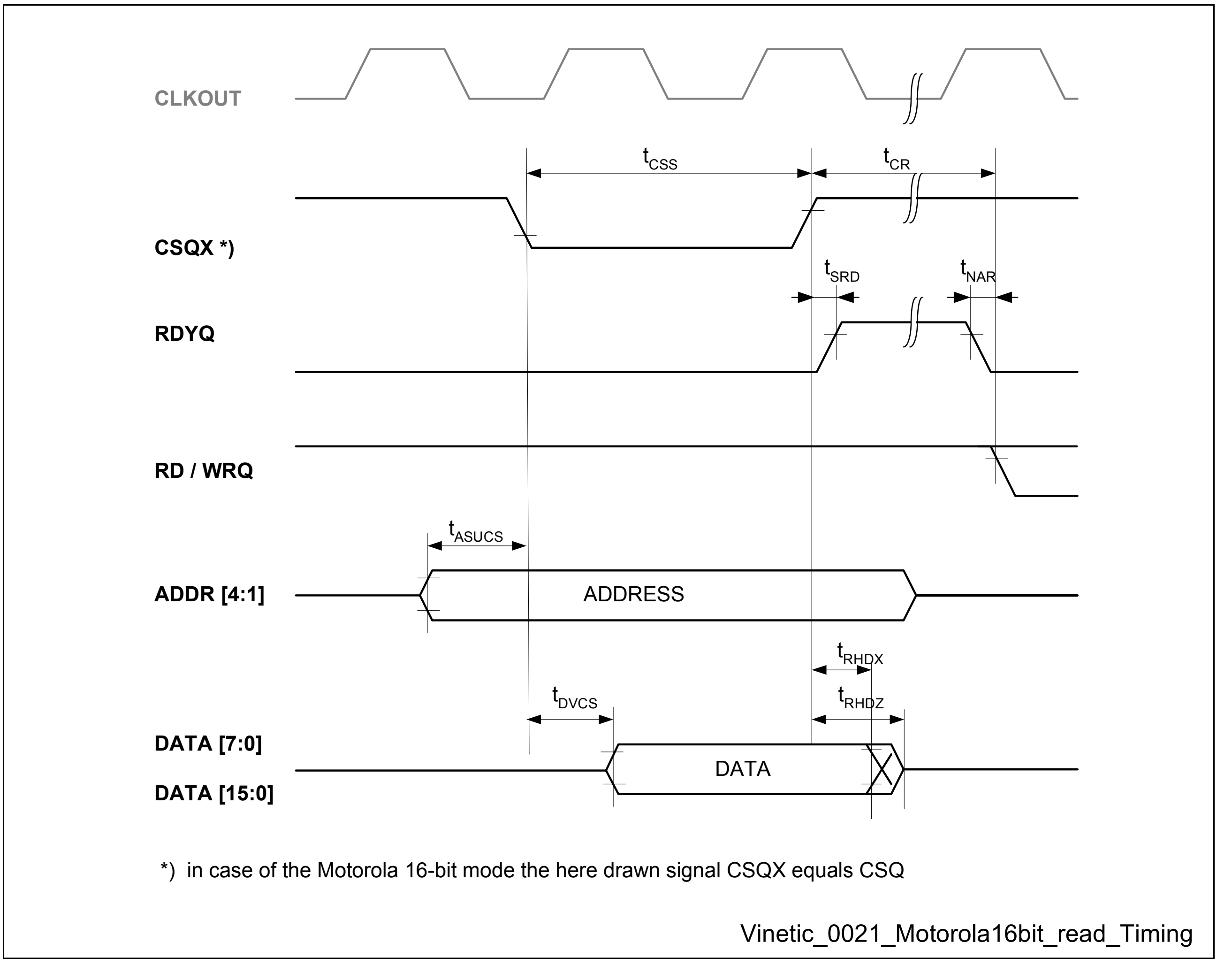


Figure 15 Read Access, Motorola Mode

Table 19 Timing Specifications for the Motorola Mode

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
CSQ strobe-pulse width	t_{CSS}	50	–	ns
Address setup time to CSQ	t_{ASUCS}	5	–	ns
Write setup time to CSQ	t_{WRSUCS}	5	–	ns
Write hold time to CSQ	t_{WRHCS}	5	–	ns
Data setup time to CSQ strobe	t_{DSU}	10	–	ns
Data hold time after write access	t_{DHWR}	5	–	ns
Next access after interface ready	t_{NAR}	65[1)]	–	ns
Strobe signal to RDYQ delay time	t_{SRD}	–	125[2)]	ns
Command recovery time	t_{CR}	1350[3)]	–	ns
Data valid after CSQ	t_{DVCS}	–	30	ns
Data hold after read access	t_{RHDX}	3	–	ns
Data float after read access	t_{RHDZ}	–	35	ns

1) If the PCM interface is not used, this time is 35 ns.

2) If the PCM interface is not used, this time is 95 ns.

3) If the PCM interface is not used, this time is 670 ns.

4.2 SCI / SPI Interface

The SCI interface of the VINETIC®-2VIP is compatible to Infineon's DuSLIC® serial interface. The SCI interface also represents one mode of the SPI interface of the Motorola PowerQuicc family (SPI slave mode).

Note: The VINETIC®-2VIP always works as a slave.

4.2.1 Pinning SCI Interface

Table 20 SCI Interface Pins

Interface Name	Pin Name	Function	Input (I) Output (O) High Imp. (Z)
CSQ	IFC6	Chip select signal starting a read or write access to VINETIC®-2VIP	I
DCLK	IFC7	Data Clock supplied to VINETIC®-2VIP	I
DIN	IFAD0	Data input carries data from the master device to the VINETIC®-2VIP	I
DOUT	IFAD1	Data output carries data from VINETIC®-2VIP to a master device	O/Z

4.2.2 Timing SCI Interface

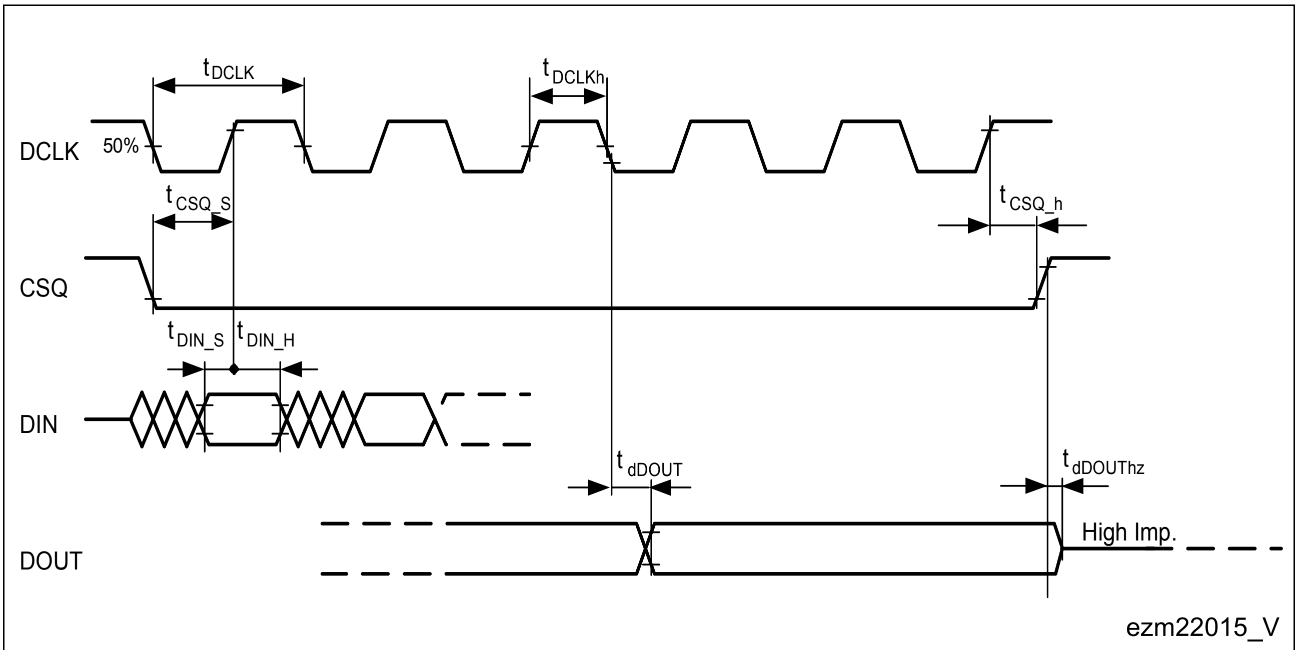


Figure 16 SCI Interface Timing

Table 21 Timing Values SCI Interface

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
Period DCLK	t_{DCLK}	1/8192	–	–	ms
DCLK high time	t_{DCLKh}	–	$0.5 \times t_{DCLK}$	–	µs
CSQ setup time	t_{CSQ_s}	10	–	–	ns
CSQ hold time	t_{CSQ_h}	30	–	–	ns
DIN setup time	t_{DIN_s}	10	–	–	ns
DIN hold time	t_{DIN_h}	10	–	–	ns
DOUT delay time[1]	t_{dDOUT}	30	–	$t_{dDOUT\_min} + 0.4$[ns/pF] $\times C_{Load}$[pF])	ns
DOUT delay time to high Z	$t_{dDOUThz}$	–	–	tbd	ns

[1] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load})

4.2.3 Data Access via the SCI Interface

There are two different command types. Short commands have just one word. Read/write commands have two command words with the address offset information located in the second word.

A write command (see **Figure 17**) consists of two command words and the following data words. The first command word determines whether the command is read or write, how the command field is to be used, and which VINETIC® channel (A, B, C, or D) is written. The second command word contains the address offset.

A read command (see **Figure 18**) consists of two command words written to DIN. After the second command word is applied to DIN, a dump-word consisting of 1s is written to DOUT. Data transfer starts with the first word following the 'dump-word'.

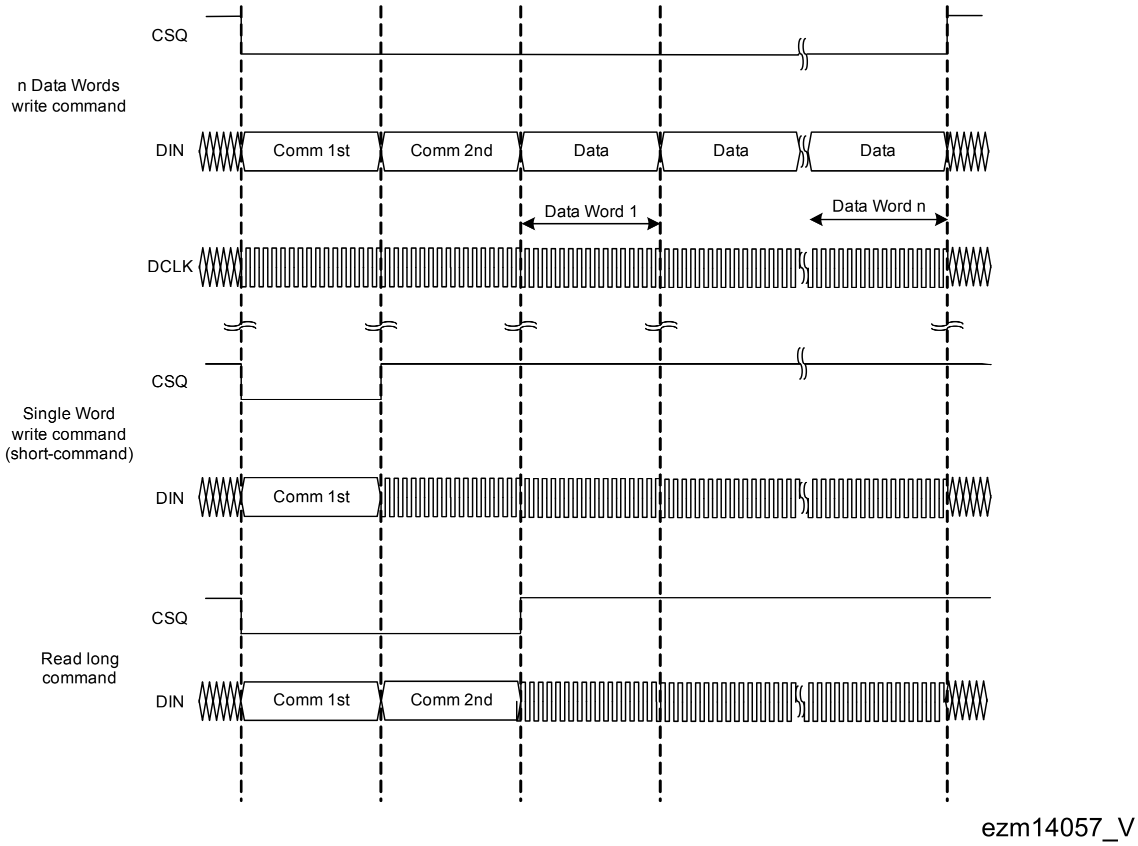


Figure 17 SCI Interface Write Access

*Note: Serial Microcontroller Interfaces Write Access shown in **Figure 17** is for n data words and single word commands.*

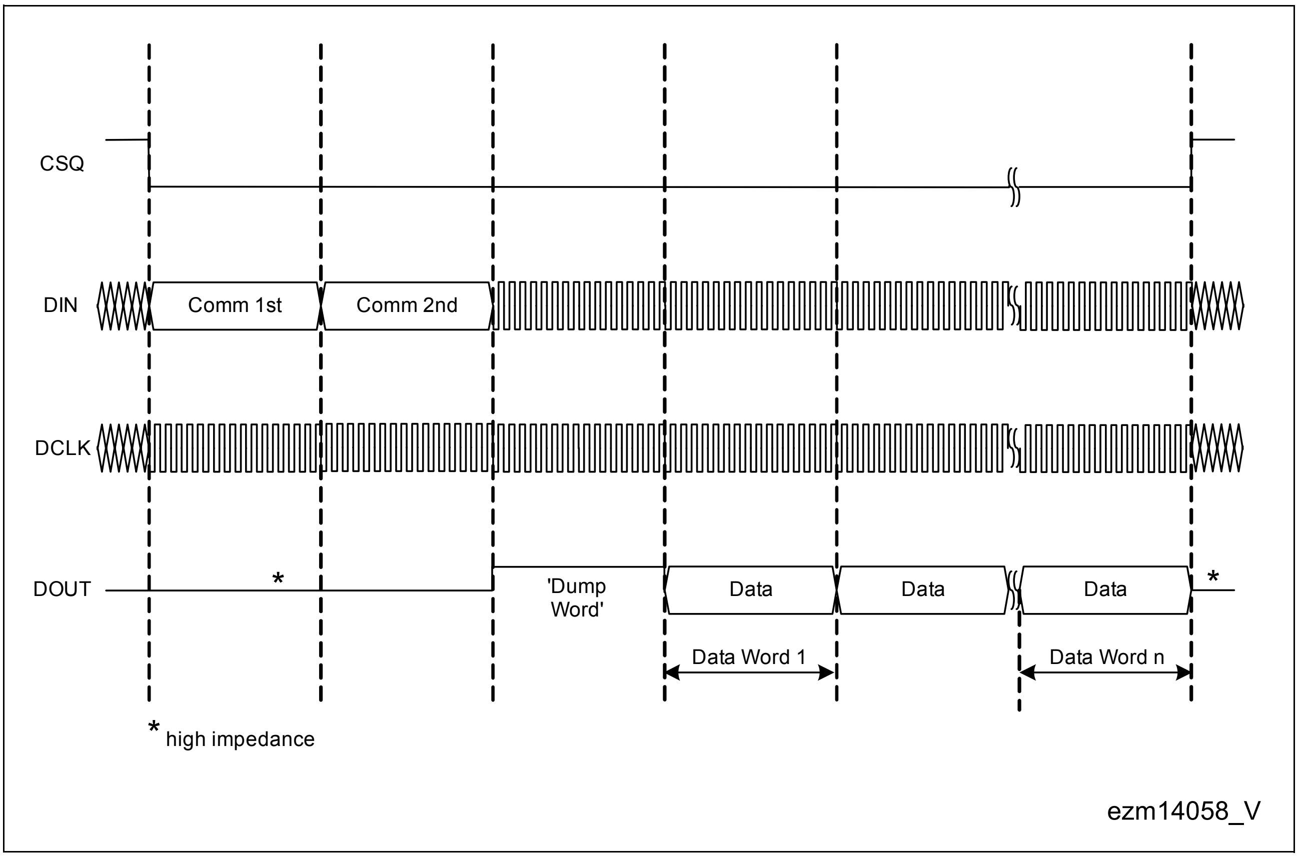


Figure 18 SCI Interface Read Access

4.3 PCM Interface

The serial PCM interface is used to transfer A-Law or µ-Law or ADPCM-compressed voice data. The PCM interface can also transfer linear data. In this case, two successive time slots are used. The eight signals of the PCM interface are used as follows (two available PCM highways):

4.3.1 Pinning PCM Interface

Table 22 PCM Interface Pins

Interface Name	Pin Name	Function	Input (I) Output (O) High Imp. (Z)
PCLK	PCL	Data clock	I
FSC	FSC	Frame synchronization	I
DX1	DX1	Data output for highway one of PCM interface	O/Z
DR1	DR1	Data input for highway one of PCM interface	I
DX2	DX2	Data output for highway two of PCM interface	O/Z
DR2	DR2	Data input for highway two of PCM interface	I
TC1Q	TC1Q	Control pin for external driver for highway one of PCM interface (open drain)	O
TC2Q	TC2Q	Control pin for external driver for highway two of PCM interface (open drain)	O

The FSC pulse identifies the beginning of a receive and transmit frame for both highways (see **Figure 19 "General PCM Interface Timing" on Page 50**). The PCLK clock signal synchronizes the data transfer on the DX1 (DX2) and DR1 (DR2) lines. In each active time slot, bytes are serialized with the MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data on DR1 (DR2). If double clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to latch the contents of the data line DR1 (DR2).

The VINETIC®-2VIP allows a flexible programming of the PCM interface. The programmable receive and transmit offsets are the same for both highways. For more information, see the *Preliminary User's Manual - Software Description*.

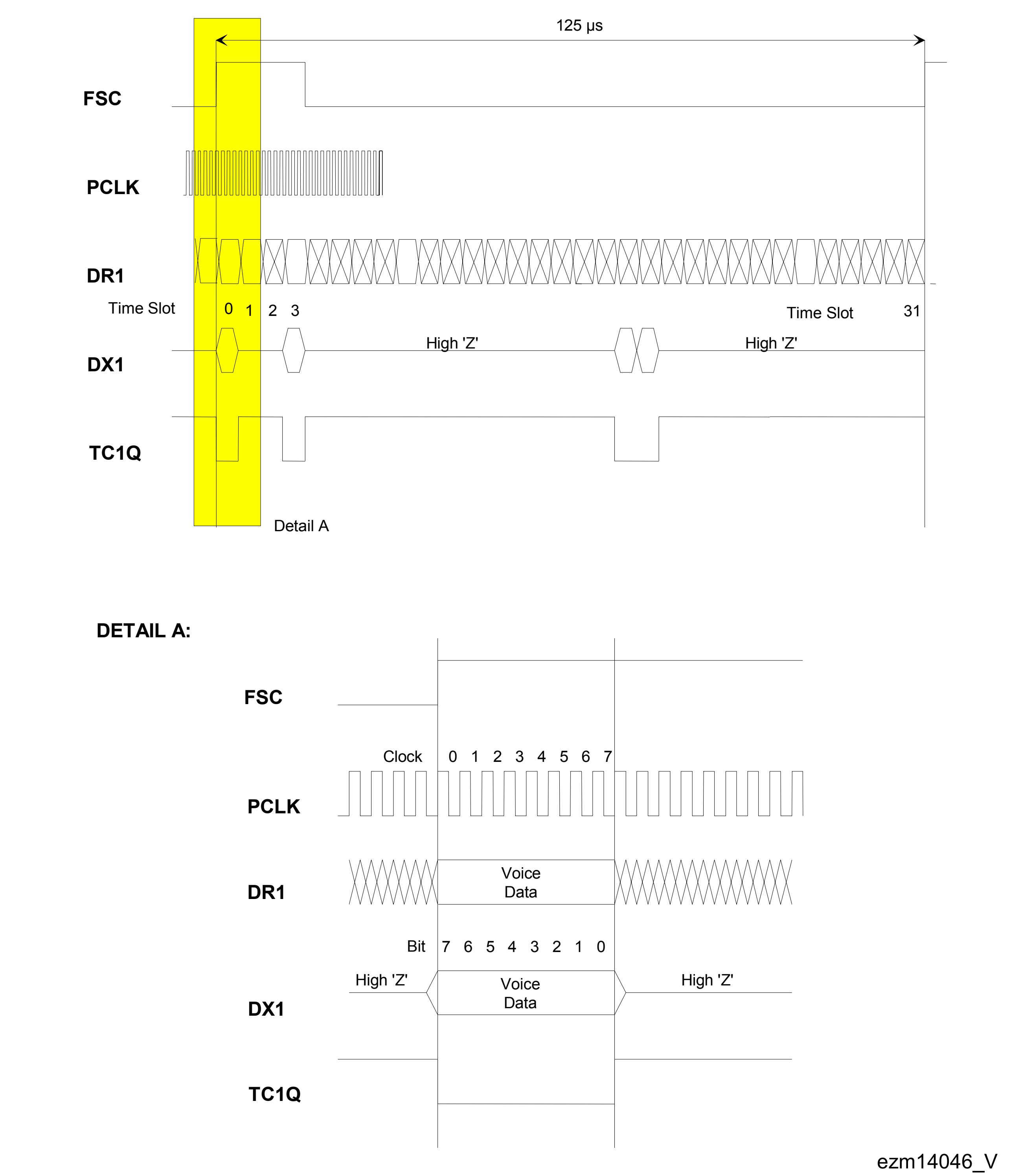


Figure 19 General PCM Interface Timing

The data rate of the interface can vary from 256 kbit/s to 8192 kbit/s for each highway. A frame may consist of up to 128 time slots of 8 bits each. The time slot and PCM highway assignment for each VINETIC®-2VIP channel can be programmed. Receive and transmit time slots can also be programmed individually (see *Preliminary User's Manual - Software Description*).

Table 23 PCM Bit Usage for A/μ-Law and ADPCM Coding

<table>
<tr><th></th><th colspan="8">DR Byte (downstream)</th><th colspan="8">DX Byte (upstream)</th></tr>
<tr><th></th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>G.711 (A-Law, μ-Law)</td><td colspan="8">data</td><td colspan="8">data</td></tr>
<tr><td>ADCPM:</td><td colspan="8"></td><td colspan="8"></td></tr>
<tr><td>40 kBit/S</td><td></td><td></td><td></td><td colspan="5">data</td><td>0</td><td>0</td><td>0</td><td colspan="5">data</td></tr>
<tr><td>32 kBit/s</td><td></td><td></td><td></td><td></td><td colspan="4">data</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="4">data</td></tr>
<tr><td>24 kBit/s</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">data</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">data</td></tr>
<tr><td>16 kBit/s</td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">data</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">data</td></tr>
</table>

For ADPCM data (see **Table 23**): In upstream direction the encoded bits are inserted at the least significant bits and the upper bits are set to zero. In the downstream direction the encoded bits are expected at the least significant bits and the upper bits are ignored.

When VINETIC® is transmitting data on DX1 (DX2), the TC1Q (TC2Q) pin is switched to low to enable an external connected driving device.

Table 24 shows PCM interface frequency examples; other frequencies between 256 kHz and 8.192 MHz are also possible (such as 1536 kHz). The number of valid time slots is defined by the formulas at the end of **Table 24**:

Table 24 VINETIC®-2VIP PCM Interface Configuration

Clock Rate PCLK [kHz]	**Single/Double Clock** [1/2]	**Time Slots** [per highway]	**Data Rate** [kbit/s per highway]
256	1	4	256
512	2	4	256
512	1	8	512
768	2	6	384
768	1	12	768
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048

Table 24 VINETIC®-2VIP PCM Interface Configuration (cont'd)

4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
$f = n*8*f_{FSC}$, $n \in [4,128]$[1)]	1	f/64	f
$f = n*16*f_{FSC}$, $n \in [4,64]$[1)]	2	f/128	f/2

1) n ... integer values, f_{FSC} = 8 kHz

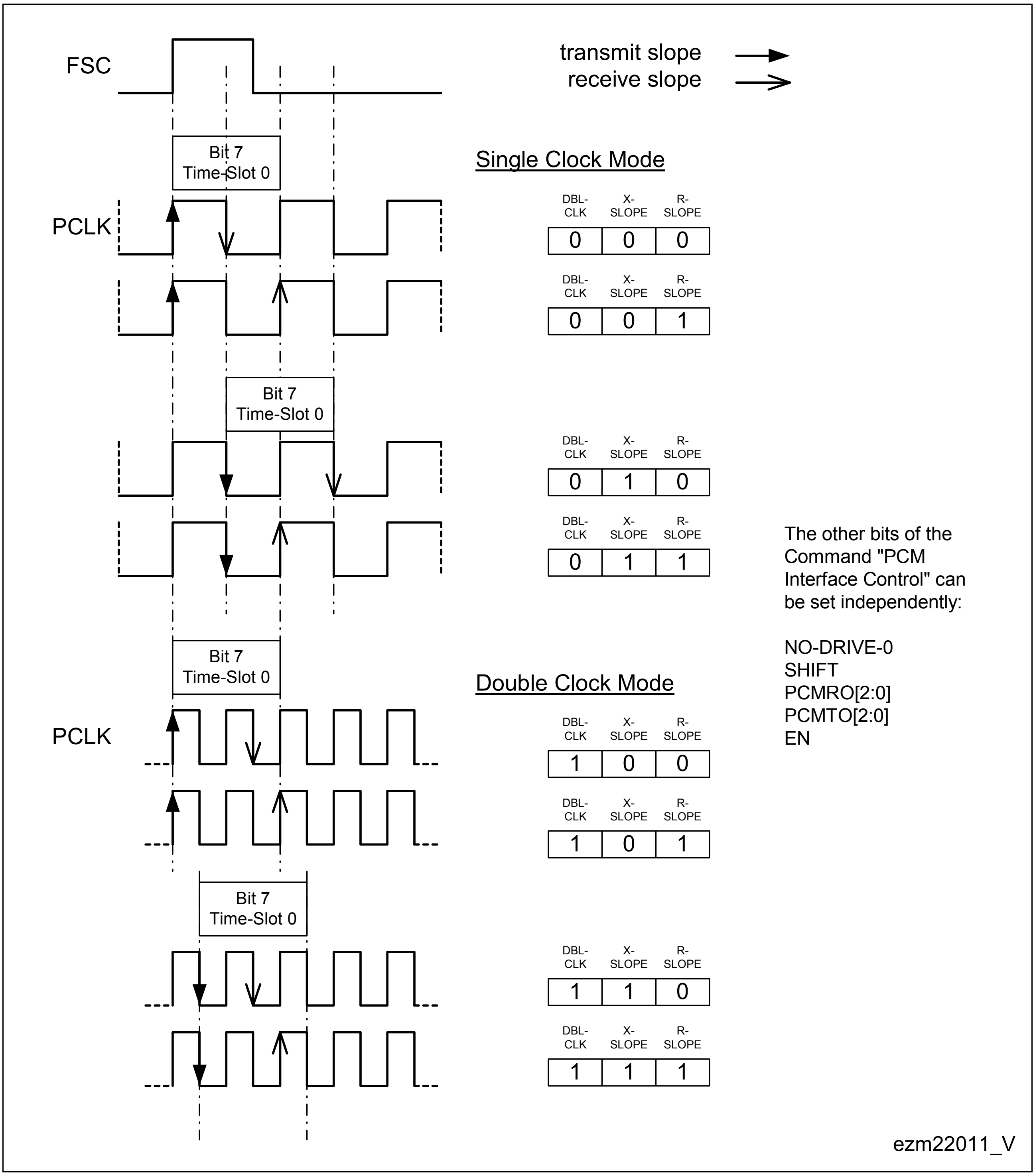


Figure 20 Setting the Slopes with the Command "PCM Interface Control"

4.3.2 Timing PCM Interface

4.3.2.1 Single-Clocking Mode

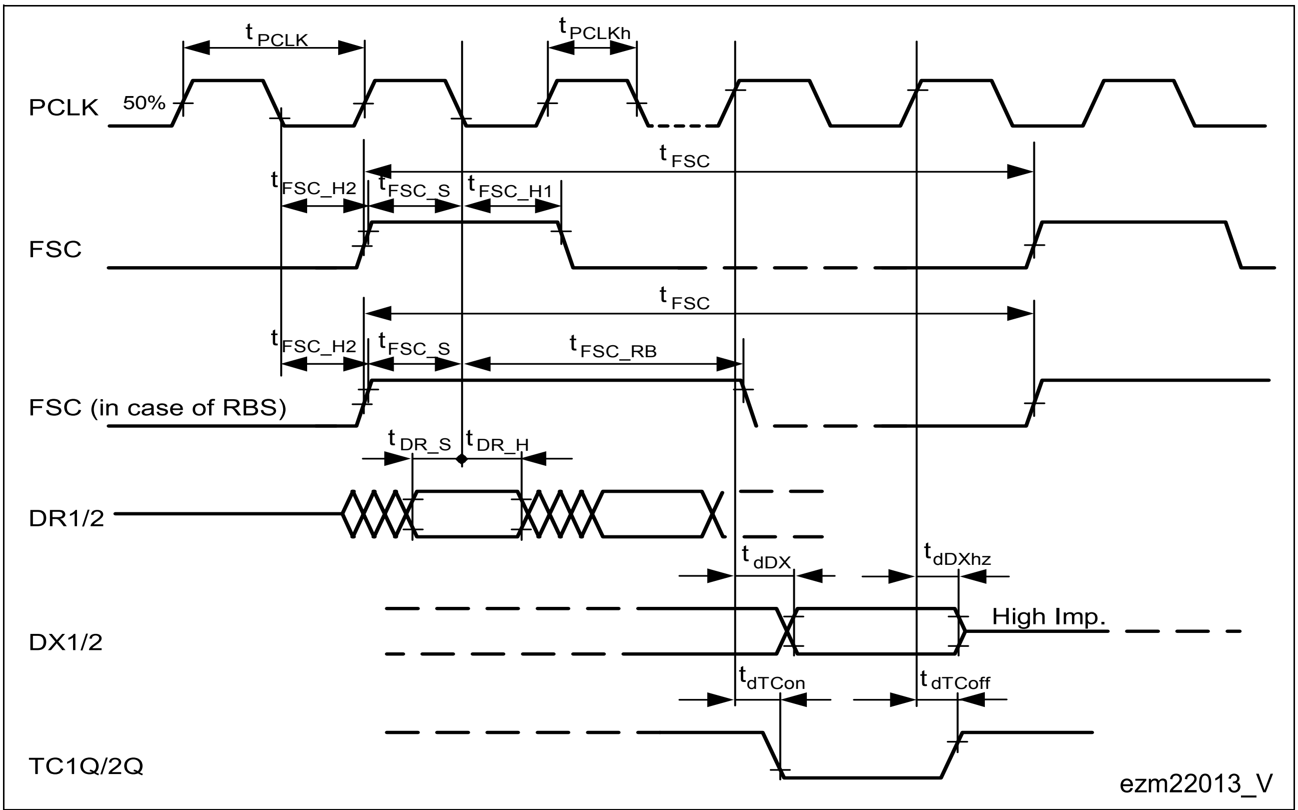


Figure 21 PCM Interface Timing – Single-Clocking Mode

Table 25 Timing Values PCM Interface (Single-Clocking Mode)

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
Period PCLK[1)]	t_{PCLK}	1/8192		1/256	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$		$0.6 \times t_{PCLK}$	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_S}	10	–	–	ns
FSC hold time 1	t_{FSC_H1}	40	–	$t_{FSC} - t_{PCLK} - t_{FSC\_S}$[2)]	ns
FSC hold time in case of RBS	t_{FSC_RB}	$t_{FSC\_H1} + t_{PCLK}$	–	$t_{FSC} + 2 \times t_{PCLK} - t_{FSC\_S}$[2)]	ns
FSC hold time 2	t_{FSC_H2}	40	–	–	ns

Table 25 Timing Values PCM Interface (Single-Clocking Mode) (cont'd)

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
DR1/2 setup time	t_{DR_S}	10	–	–	ns
FSC jitter time		–	–	+/- 0.2 x t_{PCLK}	ms
DR1/2 hold time	t_{DR_H}	10	–	–	ns
DX1/2 delay time[3]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] x C_{Load}[pF])	ns
DX1/2 delay time to high Z	t_{dDXhz}	–	–	50	ns
TC1Q/2Q delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] $\times$ C_{Load}[pF])	ns
TC1Q/2Q delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 $\times$ R_{Pullup}[kΩ] $\times$ C_{Load}[pF])	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*8*f_{FSC}, n = 4..128).

2) This is to ensure that the FSC can be sampled low at least for one t_{PCLK} within t_{FSC}.

3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

4.3.2.2 Double-Clocking Mode

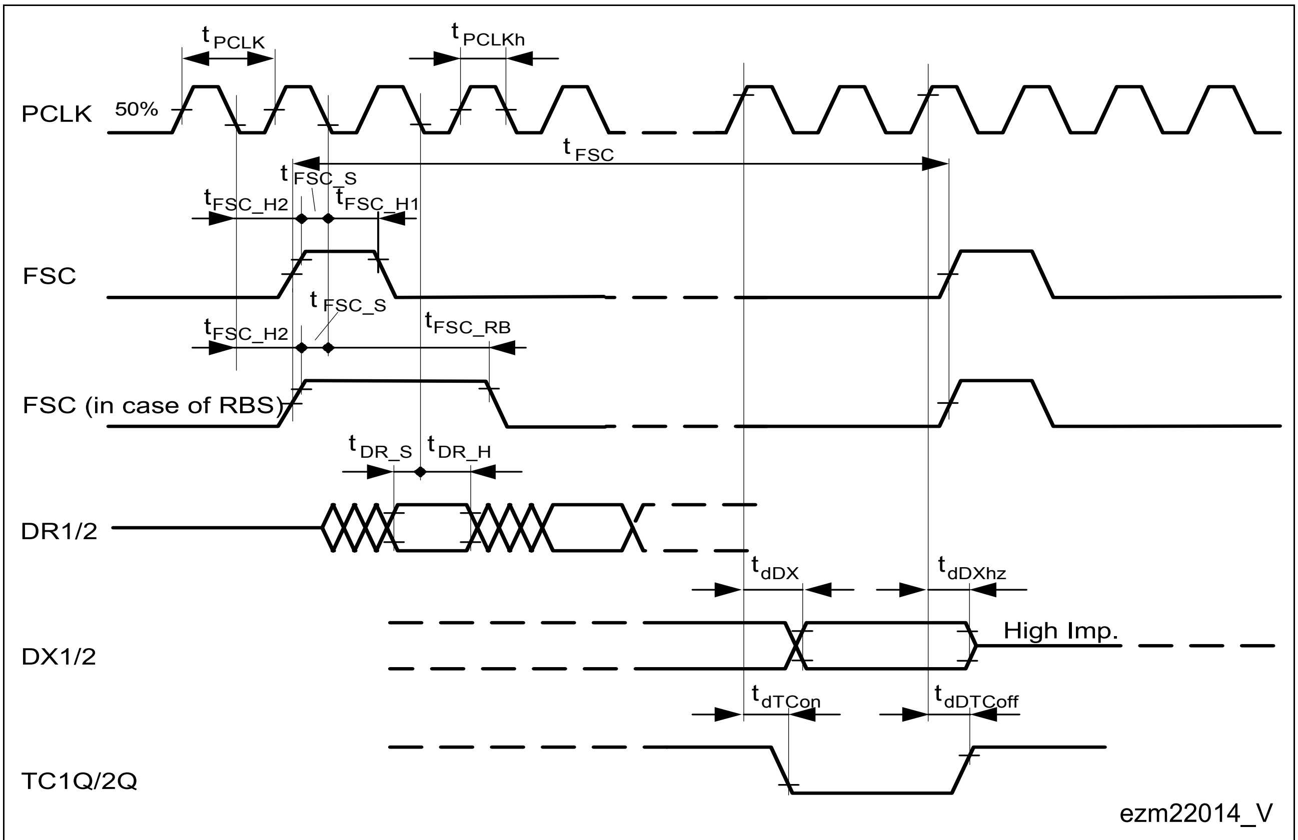


Figure 22 PCM Interface Timing – Double-Clocking Mode

Table 26 Timing Values PCM Interface (Double-Clocking Mode)

Parameter	Symbol	Limit Values Min.	Typ.	Max.	Unit
Period PCLK[1)]	t_{PCLK}	1/8192	–	1/512	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	–	$0.6 \times t_{PCLK}$	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_S}	10	–	–	ns
FSC hold time 1	t_{FSC_H1}	40	–	$t_{FSC} - t_{PCLK} - t_{FSC\_S}$[2)]	ns
FSC hold time 2	t_{FSC_H2}	40	–	–	ns
FSC hold time in case of RBS	t_{FSC_RB}	$t_{FSC\_H1} + t_{PCLK}$	–	$t_{FSC} + 2 \times t_{PCLK} - t_{FSC\_S}$[2)]	ns
FSC jitter time		–	–	+/- 0.2 x t_{PCLK}	ms
DR1/2 setup time	t_{DR_S}	10	–	–	ns

Table 26 Timing Values PCM Interface (Double-Clocking Mode) (cont'd)

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
DR1/2 hold time	t_{DR_H}	10	–	–	ns
DX1/2 delay time[3]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] × C_{Load}[pF])	ns
DX1/2 delay time to high Z	t_{dDXhz}	–	–	50	ns
TC1Q/2Q delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] × C_{Load}[pF])	ns
TC1Q/2Q delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 × R_{Pullup}[kΩ] × C_{Load}[pF])	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*16*f_{FSC}, n = 4..64).

2) This is to ensure that the FSC can be sampled low at least for one t_{PCLK} within t_{FSC}.

3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

4.4 Test Interface (JTAG Interface)

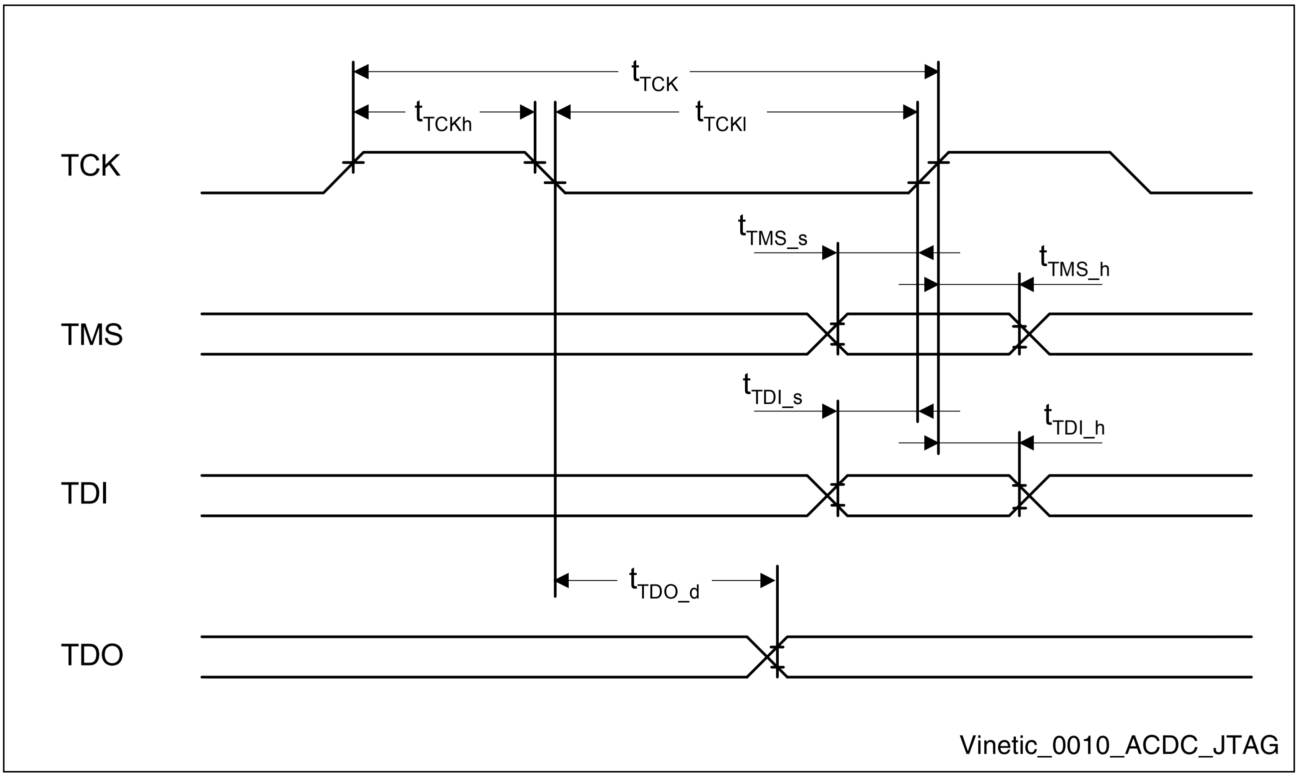


Figure 23 Test Interface (JTAG Interface) Timing

Table 27 Test Interface (JTAG Interface) Clocks

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
TCK Clock Period	t_{TCK}	100			ns	Pin TCK/TM2
TCK High Time	t_{TCKh}	40			ns	
TCK Low Time	t_{TCKl}	40			ns	

Table 28 Test Interface (JTAG Interface) Timing Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
TMS setup time	t_{TMS_s}	40			ns	Pin TMS/ TM1
TMS hold time	t_{TMS_h}	40			ns	
TDI setup time	t_{TDI_s}	40			ns	Pin TDI/TM0
TDI hold time	t_{TDI_h}	40			ns	

Table 28 Test Interface (JTAG Interface) Timing Parameters (cont'd)

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Hold: TDRSQ after TCK	t_{TDRSQ_h}	10			ns	Pin TDRSQ
TDO valid delay	t_{TDO_d}	100		$t_{dDOUT\_min} + 0.4[ns/pF] \times C_{Load}[pF])$	ns	Pin TDO/ TM3

4.5 SLIC Interface

The SLIC-S/-S2 PEB 4264/-2 and the SLIC-E/-E2 PEB 4265/-2 are controlled by ternary logic signals via the C1y[1)] and C2y[1)] pins.

The SLIC-P PEB 4266 and the SLIC-LCP PEB 4262 are controlled by ternary logic signal via the C1y[1)], C2y[1)] pins and a binary logic signal via the IO0y[1)] (SLIC-P) or IO1y[1)] (SLIC-LCP) pin.

For application circuits, please refer to the *Preliminary User's Manual - System Reference*.

1) y stands for A and B - the two analog channels of the VINETIC®-2VIP

5 Electrical Characteristics

5.1 Absolute Maximum Ratings VINETIC®-2VIP

Table 29 Absolute Maximum Ratings VINETIC®-2VIP

Parameter[1)]	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Supply pins VDD18, VDD18i, VDD18P referred to the corresp. ground pins GND, GNDi, GNDP	–	–0.3	1.98	V	–
Supply pins VDD33, VDD33i referred to the corresponding ground pins GND, GNDi	–	–0.3	3.6		
Ground pins GNDi referred to any other ground pin GNDj, GNDP	–	–0.3	0.3	V	–
Supply pins VDD18, VDD18i referred to any other supply pin VDD18j, VDD18P	–	–0.3	0.3	V	–
Analog input and output pins Pins CREFAB, CREFCD	–	–0.3 –0.3	3.6 1.98	V V	V_{DD33i} = 3.3 V, V_{DD18i} = 1.8 V, V_{GNDi} = 0 V
Digital input and output pins	–	–0.3	3.6	V	V_{DD33} = 3.3 V, V_{DD18} = 1.8 V, V_{GND} = 0 V
Digital input leakage current	I_L	–2	2	μA	$-0.3 \leq V_{in} \leq V_{DD33}$
DC input or output current at any input or output pin	–	–	100	mA	(free from latch-up)
Storage temperature	T_{STG}	–65	125	°C	–
Ambient temperature under bias	T_A	–40	85	°C	–
Power dissipation[2)]	P_D	–	1.2 1.4	W	P-LQFP-176-2 P-LBGA-176-3
ESD Robustness					
ESD voltage	–	–	2	kV	Human body model[3)]
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[4)]

[1] i, j = A, AB, B, C, CD, D

[2] according to JEDEC (four-layer board)

[3] MIL STD 883D, method 3015.7 and ESD Assn. standard S5.1-1993

[4] EOS/ESD Assn. Standard DS5.3-1993

5.2 Operating Range VINETIC®-2VIP

$V_{GND} = V_{GNDA} = V_{GNDB} = V_{GNDC} = V_{GNDD} = V_{GNDAB} = V_{GNDCD} = V_{GNDP} = 0$ V

Table 30 Operating Range VINETIC®-2VIP

Parameter	Symbol	Limit Value			Unit	Test Condition
		Min.	Typ.	Max.		
Supply pins VDD18, VDD18i referred to the corresp. ground pins GND, GNDi (i = A, AB, B, C, CD, D, P)		1.71	1.8	1.89	V	
Supply pins VDD33, VDD33i referred to the corresp. ground pins GND, GNDi (i = A, AB, B, C, CD, D)		3.14	3.3	3.47	V	
Analog input pins IO2y, IO2y, IO4y, ILx, ITx, VCMITx, ITACx referred to the corresp. ground pins GNDx (x = A, B, C, D; y = A, B)		0	–	3.3	V	$V_{DD33i} = 3.3$ V
Analog output pins DCPx, DCNx ACPx, ACNx VREFAB, VCMy C1x, C2x referred to the corresp. ground pins GNDx, GNDy (x = A, B; y = AB)		 0.3 0.3 1.3 0	 – – –	 2.7 2.7 1.7 3.3	 V V V V	$V_{DD33i} = 3.3$ V $R_{Load} > 900\ \Omega$ $R_{Load} > 9\ k\Omega$ $I_{Load} = \pm 4$ mA $I_{Load} < 250\ \mu A$

Table 30 Operating Range VINETIC®-2VIP (cont'd)

Parameter	Symbol	Limit Value			Unit	Test Condition
		Min.	Typ.	Max.		
Analog pins for passive devices CDCPx, CDCNx CREFy referred to the corresp. ground pins GNDx, GNDy (x = A, B, ; y = AB, CD)		 0 0.5	 – 0.7	 3.3 0.9	 V V	V_{DD33i} = 3.3 V
Digital input/output pins (I/O pins, GPIO pins)						
High-level input voltage	V_{IH}	2.0		3.6	V	V_{OUT} >= V_{OH} (min)
Low-level input voltage	V_{IL}	– 0.3		0.8	V	V_{OUT} <= V_{OL} (max)
High-level output voltage	V_{OH}	2.4			V	I_{OH} = – 5 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
Input leakage current	I_{IL}			1	µA	V_{DD33} = 3.3 V V_{GND} = 0 V; all other pins are floating; V_{IN} = 0 V
Output leakage current	I_{OZ}			1	µA	V_{DD33} = 3.3 V V_{GND} = 0 V; V_{OUT} = 0 V
Input capacitance at digital signal pins (except IO0x, IO1x, IO2x, IO3x, IO4x; x = A, B, C, D)		–		5	pF	
Input transition rise or fall time at digital signal pins except IO0x, IO1x, IO2x, IO3x, IO4x; x = A, B, C, D)		0	–	5	ns	
Ambient temperature under bias	T_A	–40	–	+85	°C	

5.2.1 Thermal Resistances

Table 31 Thermal Resistances

Parameter	Symbol	Typical Value	Unit	Condition
Junction to case	R_{th}	5	K/W	
Junction to Ambient for 4 Layer 100x100 JEDEC Board	R_{th} R_{th}	32 35	K/W K/W	P-LBGA-176-3 P-LQFP-176-2

5.2.2 Power Consumption VINETIC®-2VIP

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DD18} = V_{DD18A} = V_{DD18AB} = V_{DD18B} = V_{DD18C} = V_{DD18CD} = V_{DD18D} = V_{DD18P}$ = 1.8 V ±5 %;

$V_{DD33} = V_{DD33A} = V_{DD33AB} = V_{DD33B} = V_{DD33C} = V_{DD33CD} = V_{DD33D}$ = 3.3 V ±5 %

$V_{GND} = V_{GNDA} = V_{GNDAB} = V_{GNDB} = V_{GNDC} = V_{GNDCD} = V_{GNDD} = V_{GNDP}$ = 0 V

Table 32 Power Consumption VINETIC®-2VIP

Parameter	Symbol	Limit Values			Unit	Test Condition/Remark
		min	typ	max		
Power consumption in operation modes[1]						
Deep Sleep	$P_{DDDSleep}$	–	45	68	mw	
Sleep all channels	$P_{DDSleep, 1.8V}$ $P_{DDSleep, 3.3V}$	– –	70 35	87.5 44	mW mW	(MCLK, PCLK = 2 MHz)
Power down (PDH) all channels	$P_{DDPDH, 1.8V}$ $P_{DDPDH, 3.3V}$	– –	70 25	87.5 32	mW mW	
Power Down (PDRH) all channels	$P_{DDPDRH,1.8V}$ $P_{DDPDRH,3.3V}$	– –	100 53	130 66	mW mW	
Active one channel, Power Down (PDH) other channel	$P_{DDAct1,1.8V}$ $P_{DDAct1,3.3V}$	– –	110 - 400[2] 58	480[2] 72	mW mW	
Active one channel, Power Down Resistive other channel	$P_{DDAct1,1.8V}$ $P_{DDAct1,3.3V}$	– –	130 - 400[2] 73	480[2] 91	mW mW	basic EDSP load included: 4 ch. ALM + PCM (~15 Mcycle/s)

Table 32 Power Consumption VINETIC®-2VIP (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition/Remark
		min	typ	max		
Active 2 channels	$P_{DDAct2,1.8V}$	–	140 - 400[2]	480[2]	mW	basic EDSP load included: 2 ch. ALM + PCM (~10 Mcycle/s)
	$P_{DDAct2,3.3V}$	–	155	190	mW	
EDSP module[3]						
Active	$P_{DDEDSP,1.8V}$	~1.6 * Mcycle			mW /Mcycle	EDSP power consumption

[1] In Active modes the values of both supply rails 3.3 V and 1.8 V have to be added.

[2] Depends on the used EDSP load.

[3] For estimation of power consumption with different EDSP loads.

5.2.3 Power-Up Sequence VINETIC®-2VIP

The voltage at the 3.3 V power supply pins (VDD33, VDD33i) should be applied before the 1.8 V power supply pins (VDD18, VDD18j, VDD18P) are supplied.

Table 33 Power-Up Sequence VINETIC®-2VIP

Parameter[1]	Symbol	Limit Value			Unit	Test Condition
		min.	typ.	max.		
Time between power-up of VDD33, VDD33i and VDD18, VDD18j, VDD18P	t_{PU}	0	–	–	ms	

[1] i, j = A, AB, B, C, CD, D

Note: No voltage should be applied to any input or output pin before the VDD33 voltages are applied. A latch-up effect might occur; in that case all voltages have to be switched off.

5.3 Transmission Characteristics VINETIC®-2VIP

The specifications given in this section are derived from linecard requirements, which can only be fulfilled by the complete VINETIC® system comprising both chips, a VINETIC®-2VIP voice codec and a SLIC chip.

Functionality and performance are guaranteed for T_A = 0 to 70 °C by production testing. Operation at an extended temperature range of –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodical sampling and testing of production devices at the temperature extremes.

Test Conditions

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DD18} = V_{DD18A} = V_{DD18AB} = V_{DD18B} = V_{DD18C} = V_{DD18CD} = V_{DD18D} = V_{DD18P}$ = 1.8 V ±5 %;

$V_{DD33} = V_{DD33A} = V_{DD33AB} = V_{DD33B} = V_{DD33C} = V_{DD33CD} = V_{DD33D}$ = 3.3 V ±5 %

$V_{GND} = V_{GNDA} = V_{GNDAB} = V_{GNDB} = V_{GNDC} = V_{GNDCD} = V_{GNDD} = V_{GNDP}$ = 0 V

Register BCR1: TEST-EN = 1, (TTX-EN = 0)

Register BCR2: TH-DIS = 1, IM-DIS = 1,

Register RTR: RING-OFFSET = [1 0] , PCM2DC = 1, LM-ONCE = 0

Register TSTR2: OPIM-AN = 1, OPIM-HW = 1, AC-XGAIN = 1, AC-RGAIN = 1

Register TSTR3: DC-POFI-HI = 1

Unless otherwise stated, the default settings and the CROM-coefficients are used.

A digital AC or DC level of 0 dBm0 is defined as 3.14 dB below the full digital scale.

An analog AC or DC level of 0 dBm corresponds to 0.775 Vrms.

5.3.1 AC Transmission VINETIC®-2VIP

Table 34 AC Transmission (Active Mode) I

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
Insertion Loss (with CROM coefficient set)							
1	A-D (see **Figure 25**)	PCM_{OUT}	V_G = –24.6 dBm f = 1014 Hz	–0.2	0	+0.2	dBm0
2	D-A (see **Figure 25**)	V_{AC}	PCM_{in} = 0 dBm0 f = 1014 Hz	–14.67	–14.47	–14.27	dBm

Table 34 AC Transmission (Active Mode) I (cont'd)

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
3	Gain variation with temperature –40 … +85 °C	–	–	–	–	±0.1	dB

Frequency Response

No.	Parameter	Symbol	Conditions	min.	typ.	max.	Unit
	Receive loss Frequency variation	G_{RAF}	Reference frequency 1014 Hz, input signal level 0 dBm0, any PCM mode				
4			f = 300 Hz	–0.30	–0.10	0.10	dB
5			f = 2400 Hz	-0.03	0.17	0.37	dB
6			f = 3000 Hz	0.01	0.21	0.41	dB
	Transmit loss Frequency variation	G_{XAF}	Reference frequency 1014 Hz, output signal level 0 dBm0, any PCM mode				
7			f = 300 Hz	0.26	0.46	0.66	dB
8			f = 2400 Hz	–2.31	–2.11	–1.91	dB
9			f = 3000 Hz	–3.37	–3.17	–2.97	dB

Gain Tracking

No.	Parameter	Symbol	Conditions	min.	typ.	max.	Unit
	Transmit gain Signal level variation	G_{XAL}	Sinusoidal test method f = 1014 Hz, reference level –10 dBm0, any PCM mode				
10			VF_XI = –55 to –50 dBm0	–1.4	–	1.4	dB
11			VF_XI = –50 to –40 dBm0	–0.5	–	0.5	dB
12			VF_XI = –40 to +3 dBm0	–0.25	–	0.25	dB

Table 34 AC Transmission (Active Mode) I (cont'd)

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
	Receive gain Signal level var.	G_{RAL}	Sinusoidal test method f = 1014 Hz, reference level –10 dBm0				
13			D_R0 = –55 to –50 dBm0	–0.4	–	1.4	dB
14			D_R0 = –50 to –40 dBm0	–0.5	–	0.5	dB
15			D_R0 = –40 to +3 dBm0	–0.25	–	0.25	dB

Table 35 AC Transmission in (Active Mode) II

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
Overload Compression A/D (see Figure 24)							
Harmonic Distortion - 2nd Harmonic THD2, 3rd Harmonic THD3							
1	Transmit any PCM mode	THD2	out.ref.: –7 dBm0 300 - 3400 Hz	–	–	–44	dB
2	Receive any PCM mode	THD2	inp.ref.: –7 dBm0 300 - 3400 Hz	–	–	–44	dB
3	Transmit any PCM mode	THD3	out.ref.: –7 dBm0 300 - 3400 Hz	–	–	–44	dB
4	Receive any PCM mode	THD3	inp.ref.: –7 dBm0 300 - 3400 Hz	–	–	–44	dB
Idle Channel Noise							
5	At ACN, ACP (receive) any PCM mode	N_{RP}	Psophometric	–	–94	–87	dBmp
6	PCM side (transmit) linear PCM mode	N_{TP}	Psophometric	–	–84	–79	dBm0p

Table 35 AC Transmission in (Active Mode) II (cont'd)

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
Total Distortion (Sinusoidal Test Method)							
	Signal to total-distortion transmit	$STDA_X$	f = 1014 Hz , A-Law				
7			–45 dBm0	27.5	29	–	dB
8			–40 dBm0	32.5	34	–	dB
9			0 dBm0	39.2	41	–	dB
	Signal to total-distortion receive	$STDA_R$	f = 1014 Hz , A-Law				
10			–45 dBm0	25.4	26.9	–	dB
11			–40 dBm0	31.6	33.1	–	dB
12			0 dBm0	39.5	40.8	–	dB
	Signal to total-distortion transmit	$STDM_X$	f = 1014 Hz , µ-Law				
13			–45 dBm0	31.9	32.4	–	dB
14			–40 dBm0	33.6	35.1	–	dB
15			0 dBm0	38.5	40.0	–	dB
	Signal to total-distortion receive	$STDM_R$	f = 1014 Hz , µ-Law				
16			–45 dBm0	28.7	30.2	–	dB
17			–40 dBm0	32.5	33.8	–	dB
18			0 dBm0	39.0	40.5	–	dB
Group Delay							
19	Transmit delay, absolute	D_{XA}	f = 500 - 2800 Hz	tbd	710	tbd	µs
20	Receive delay, absolute	D_{RA}	f = 500 - 2800 Hz	tbd	600	tbd	µs
21	Group-delay distortion, receive and transmit, relative to 1500 Hz (see **Figure 28**)	D_{XR}	f = 500 - 600 Hz	–	–	300	µs
22			f = 600 - 1000 Hz	–	–	150	µs
23			f = 1000 - 2600 Hz	–	–	100	µs
24			f = 2600 - 2800 Hz	–	–	100	µs
25			f = 2800 - 3000 Hz	–	–	300	µs

Table 36 Power-Supply Rejection Ratio

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
	Power-supply rejection ratio		70 mVrms				
1	Receive V_{DD} at DCP/DCN at ACP/ACN	PSR_R	f = 1014 Hz f = 0 kHz to 4 kHz f = 4 kHz to 50kHz	40 tbd tbd	tbd tbd tbd	–	dB
2	Transmit V_{DD} at PCM	PSR_X	f = 1014 Hz f = 0 kHz to 4 kHz f = 4 kHz to 50kHz	53.6 tbd tbd	tbd tbd tbd	–	dBm0

Table 37 Crosstalk[1)]

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
1	TX to TX	$CT_{X\text{-}X}$	any channel to any other channel	–	tbd	-75	dB
2	TX to RX	$CT_{X\text{-}R}$	any channel to any channel	–	tbd	-75	dB
3	RX toTX	$CT_{R\text{-}X}$	any channel to any other channel	–	tbd	-75	dB
4	RX or RX	$CT_{R\text{-}R}$	any channel to any channel	–	tbd	-75	dB

1) guaranteed by design

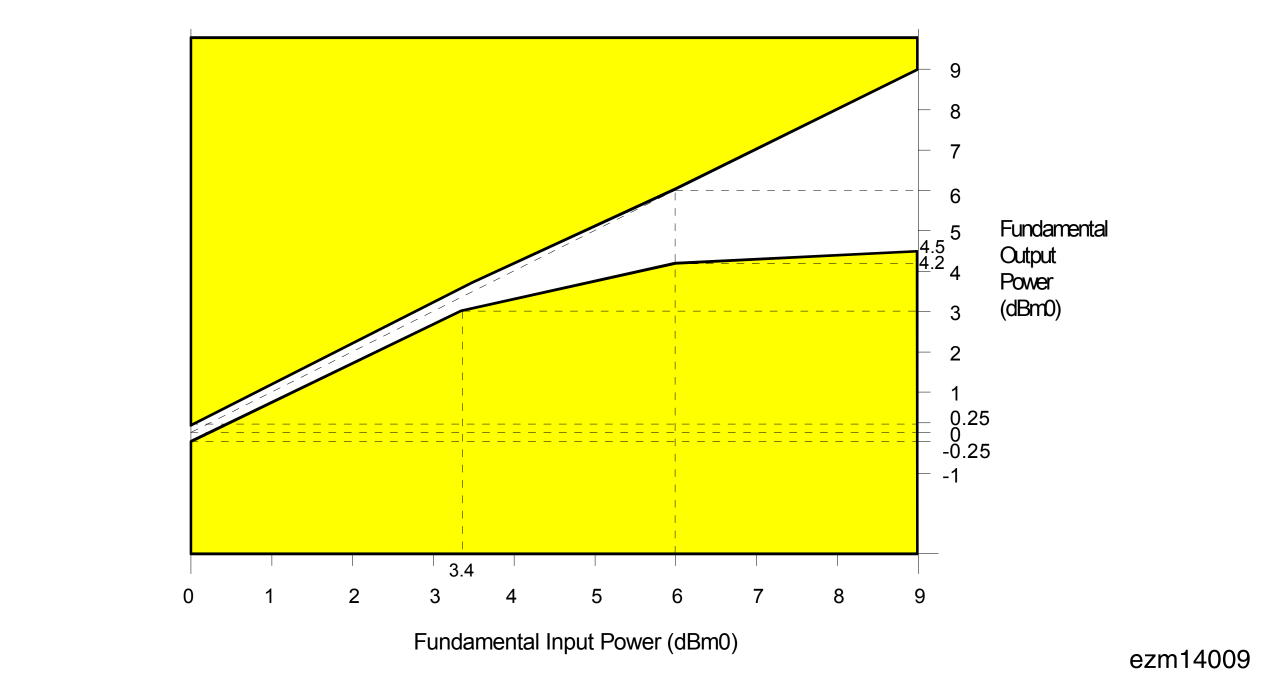


Figure 24 Overload Compression A/D

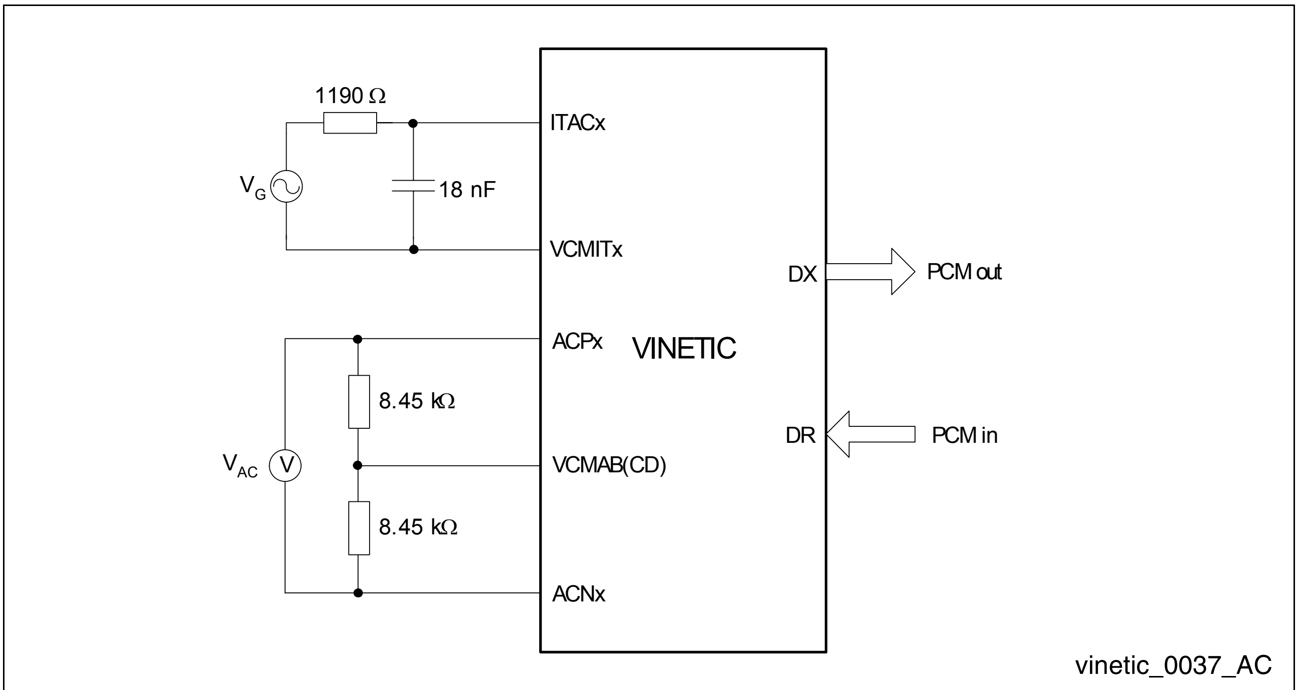


Figure 25 AC Transmission Test Circuit

5.3.1.1 Gain Tracking (Receive or Transmit)

In the figures below, the gain deviations stay within the limits.

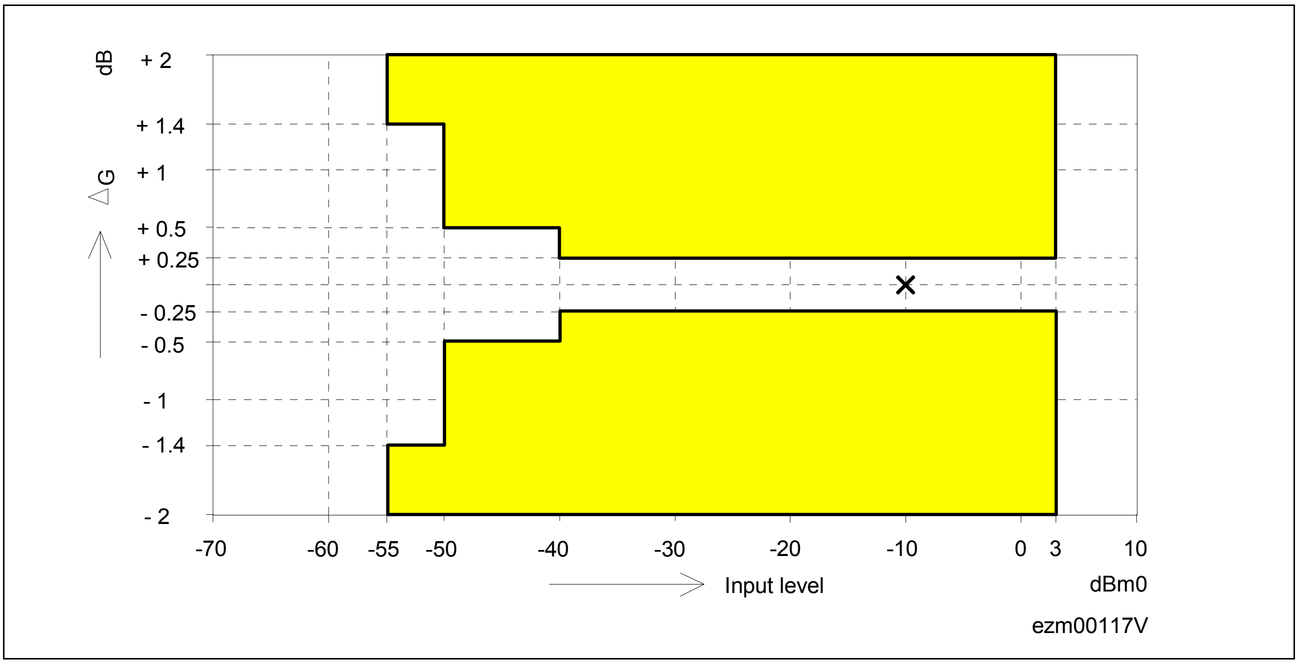


Figure 26 Gain Tracking Receive

Measured with a sine wave of f = 1014 Hz, the reference level is –10 dBm0.

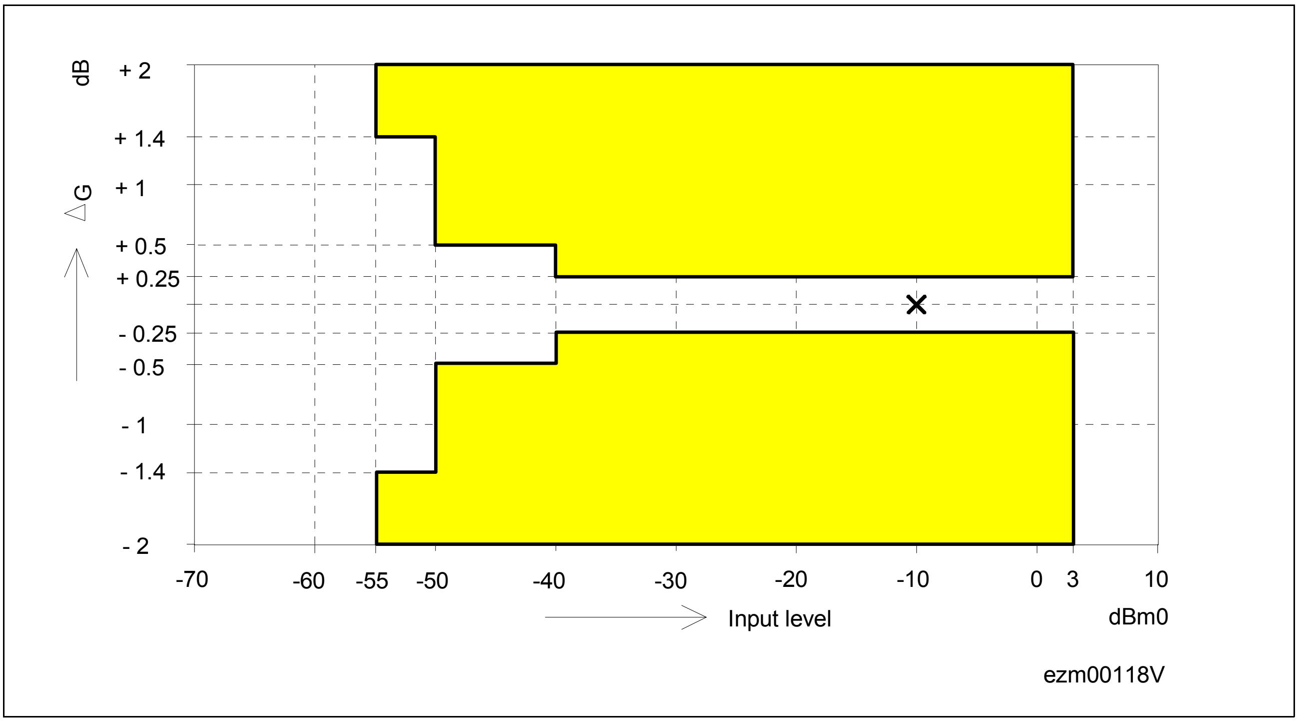


Figure 27 Gain-Tracking Transmit

Measured with a sine wave of f = 1014 Hz, the reference level is –10 dBm0.

5.3.1.2 Group Delay

The group delay depends among other factors on receive and transmit filters, and therefore specific filter programming or packet transfers may cause additional group delays. The absolute group delay also depends on the programmed time slot.

Figure 28 shows that the group delay distortion is below the limits.

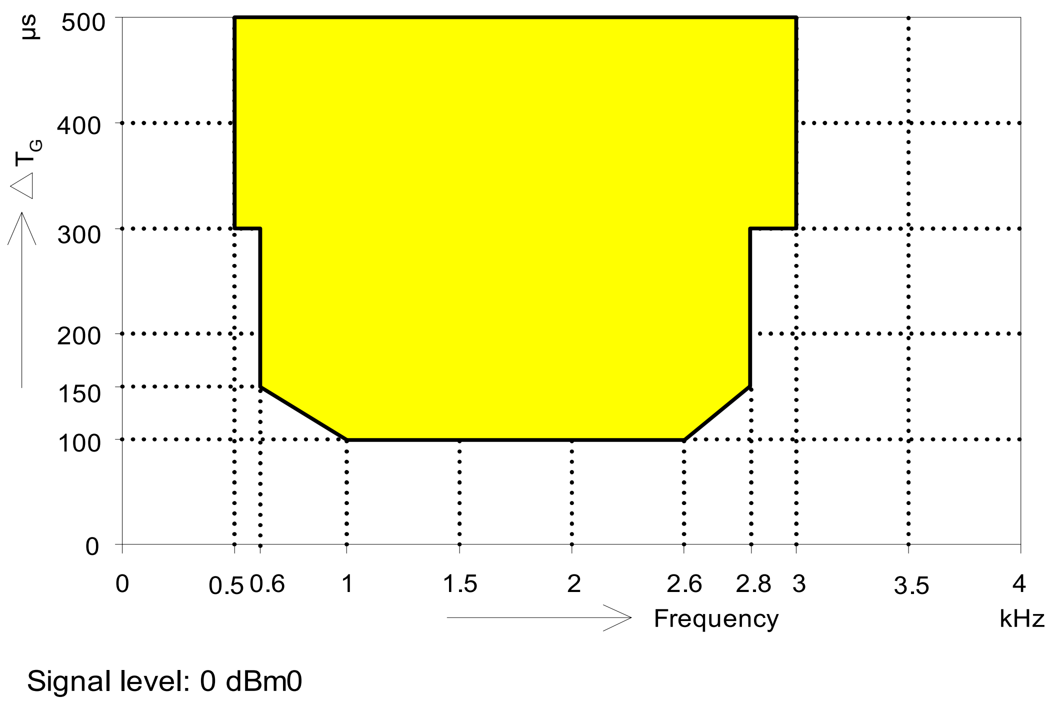


Figure 28 Group-Delay Distortion Receive and Transmit

5.3.2 DC Transmission VINETIC®-2VIP

T_A = –40 °C to 85 °C, unless otherwise stated.

No capacitor between the CDCP/CDCN pins connected (see Figure 29).

Table 38 DC Transmission

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
Insertion Loss							
1	A-D (see Figure 29)	PCM_{OUT}	V_G = -0.098dBm f = 250 Hz any PCM Mode	–0.2	0	+0.2	dBm0

Table 38 DC Transmission (cont'd)

No.	Parameter	Symbol	Conditions	Limit Values			Unit
				min.	typ.	max.	
2	D-A (see Figure 29)	V_{AC}	PCM_{in} = 0 dBm0 any PCM Mode f = 250 Hz Active High Ring Pause	 4.84 4.84	 5.04 5.04	 5.24 5.24	 dBm dBm
3	Gain variation with temperature –40 … +85 °C	–	–	–	–	±0.1	dB

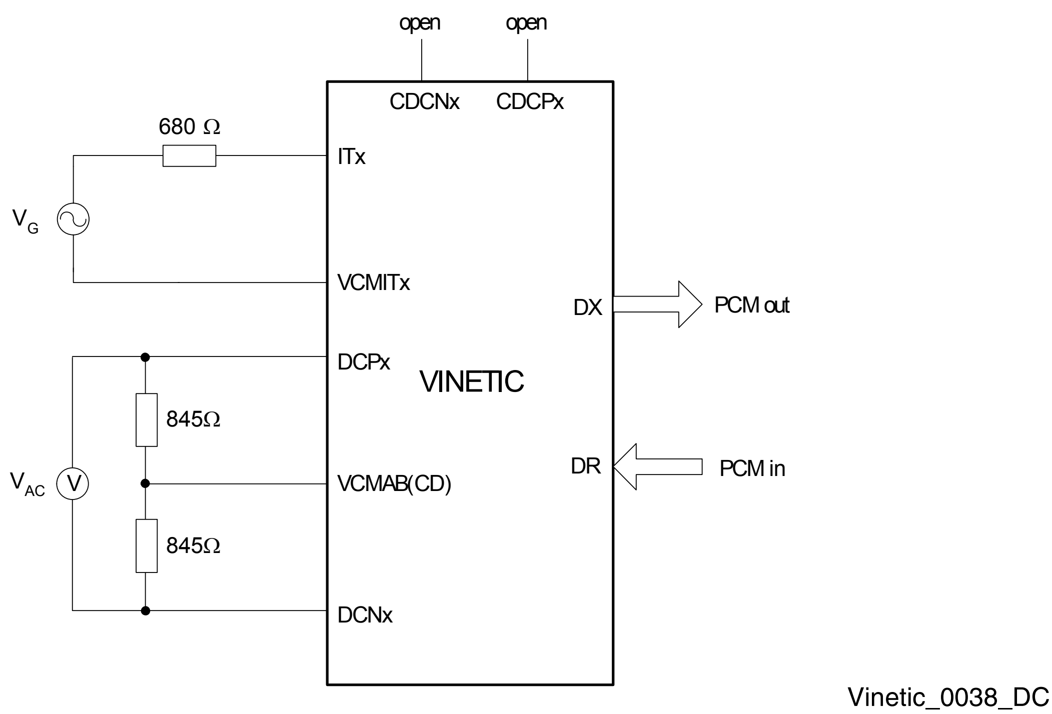


Figure 29 DC Transmission Test Circuit

5.4 Miscellaneous Characteristics

T_A = –40 °C to 85 °C, unless otherwise stated.
VDD33 = VDD33i = VDD33j = 3.3V ±5 %
(i = A, B; j = AB, CD)

Table 39 Comparator Thresholds and SLIC Interface

No.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Off-hook Detection Threshold at Pin IT_i							
1	Off-hook threshold	V_{OffThr}	–	V_{VCMITi} + 0.272 V_{VCMITi} – 0.272	–	V	Sleep Mode
Ground Key Detection Threshold at Pins IL_i							
2	Ground key threshold low	V_{GKpLo} V_{GKnLo}	–	V_{VCMITi} + 0.272 V_{VCMITi} – 0.272	–	V	Active Mode
3	Ground key threshold high	V_{GKpHi} V_{GKnHi}	–	V_{VCMITi} + 0.640 V_{VCMITi} – 0.640	–	V	
4	Ground key hysteresis	V_{GKHyst}	–	0.060	–	V	
SLIC Interface Pins $C1_i$, $C2_i$							
	Output voltage at pins $C1_i$, $C2_i$						
5	Low level (L)	V_{OLHV}	–0.3	–	0.6	V	
6	Mid level (M)	V_{OMHV}	1.2	1.65	2.1	V	
7	High level (H)	V_{OHHV}	2.7	–	–	V	
SLIC Overtemperature Comparator at Pins $C1_i$							
8	Current drained at pin C1	I_{OTLo}		–	30	µA	Normal operation
		I_{OTHi}	120		200		Overtemp. detected

6 Package Outlines

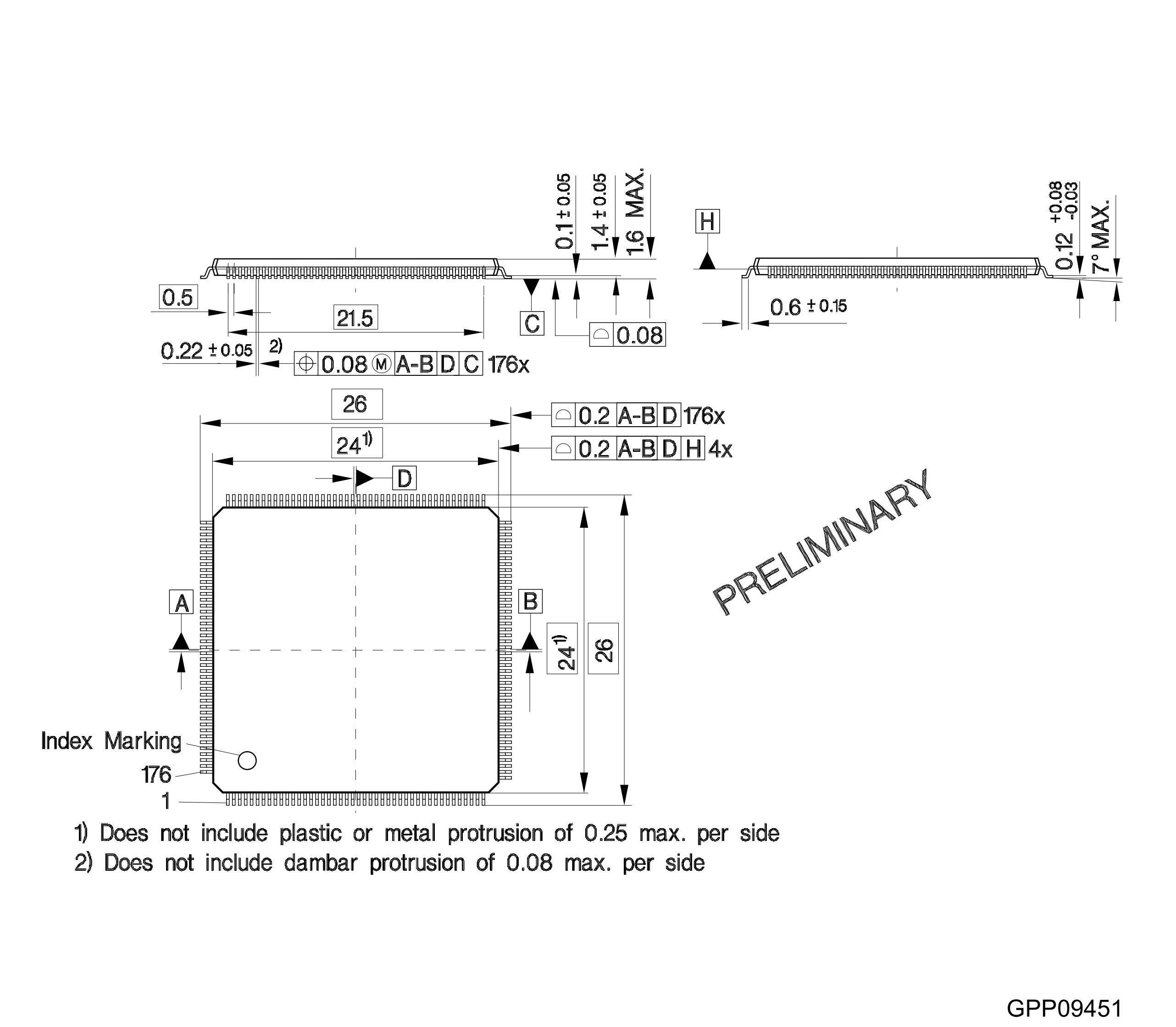


Figure 30 **P-LQFP-176-2** (Plastic Low Profile Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

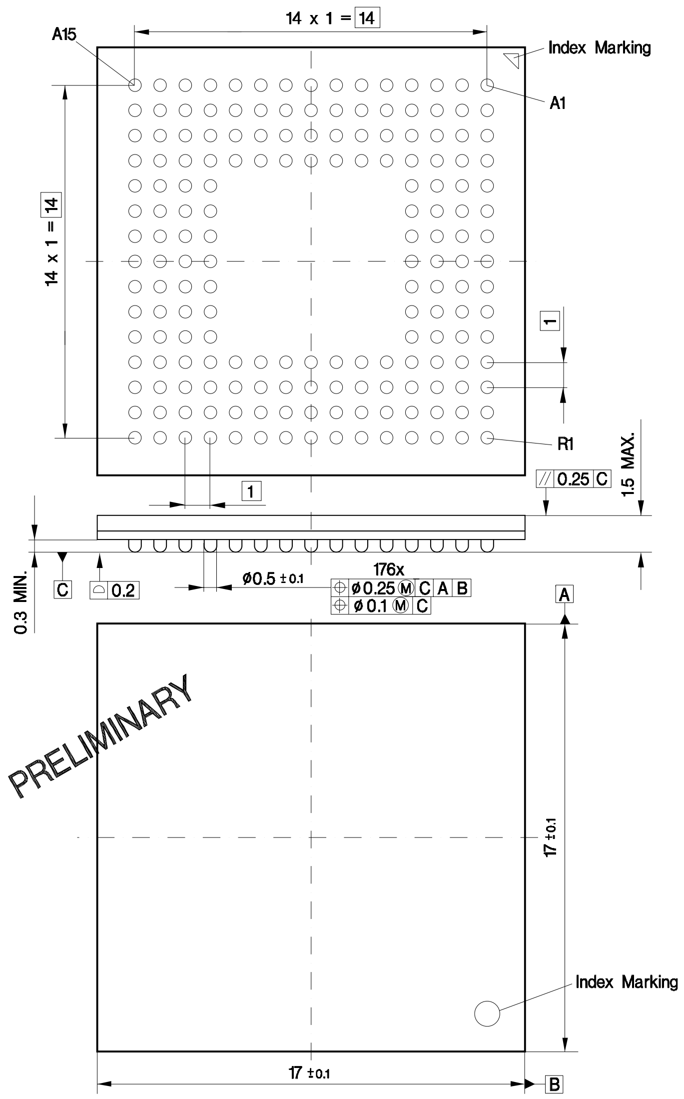


Figure 31 **P-LBGA-176-3** (Plastic Low Profile Ball Grid Array Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

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Terminology

A	
A/D	Analog to digital
AAL2	ATM Adaption Layer 2
AC	Alternative Current
ADC	Analog Digital Converter
AITDF	Advanced Integrated Test and Diagnostic Functions
ATD	Answering Tone Detector
ATM	Asynchronous Transfer Mode
C	
CAS	Channel Associated Signaling
CNG	Comfort Noise Generation
Codec	Coder Decoder
CPE	Customer Premises Equipment
CRAM	Coefficient RAM
D	
DAC	Digital Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency
E	
EDSP	Enhanced Digital Signal Processor
EXP	Expander
F	
FRR	Frequency Response Receive filter
FRX	Frequency Response Transmit filter
FSK	Frequency Shift Keying
G	
GPIO	General Purpose Input / Output
H	
HW	Hardware

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I	
IAD	Integrated Access Device
ITU	International Telecommunication Union
IP	Internet Protocol
ISDN	Integrated Services Digital Network
J	
JTAG	Joint Test Action Group
L	
LSSGR	Local area transport access Switching System Generic Requirements
N	
NG-DLC	Next Generation Digital Loop Carrier
NT	Network Terminal
P	
PBX	Private Branch eXchange
PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
R	
RAM	Random Access Memory
RBS	Robbed Bit Signaling
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
S	
SLIC	Subscriber Line Interface Circuit (same for all versions)
SOHO	Small Office / Home Office
T	
TG	Tone Generator
TH	Transhybrid Balancing
TS	Time Slot
TTX	Teletax (Metering)
U	
UTD	Universal Tone Detection

V

VAD	Voice Activity Detection
VINETIC®	Voice and Internet Enhanced Telephony Interface Concept
VINETICOS	Voice and Internet Enhanced Telephony Interface Concept Coefficients Calculation Software
VoATM	Voice over ATM
VoDSL	Voice over DSL
VoIP	Voice over IP

X

xDSL	(all flavors of) Digital Subscriber Line

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