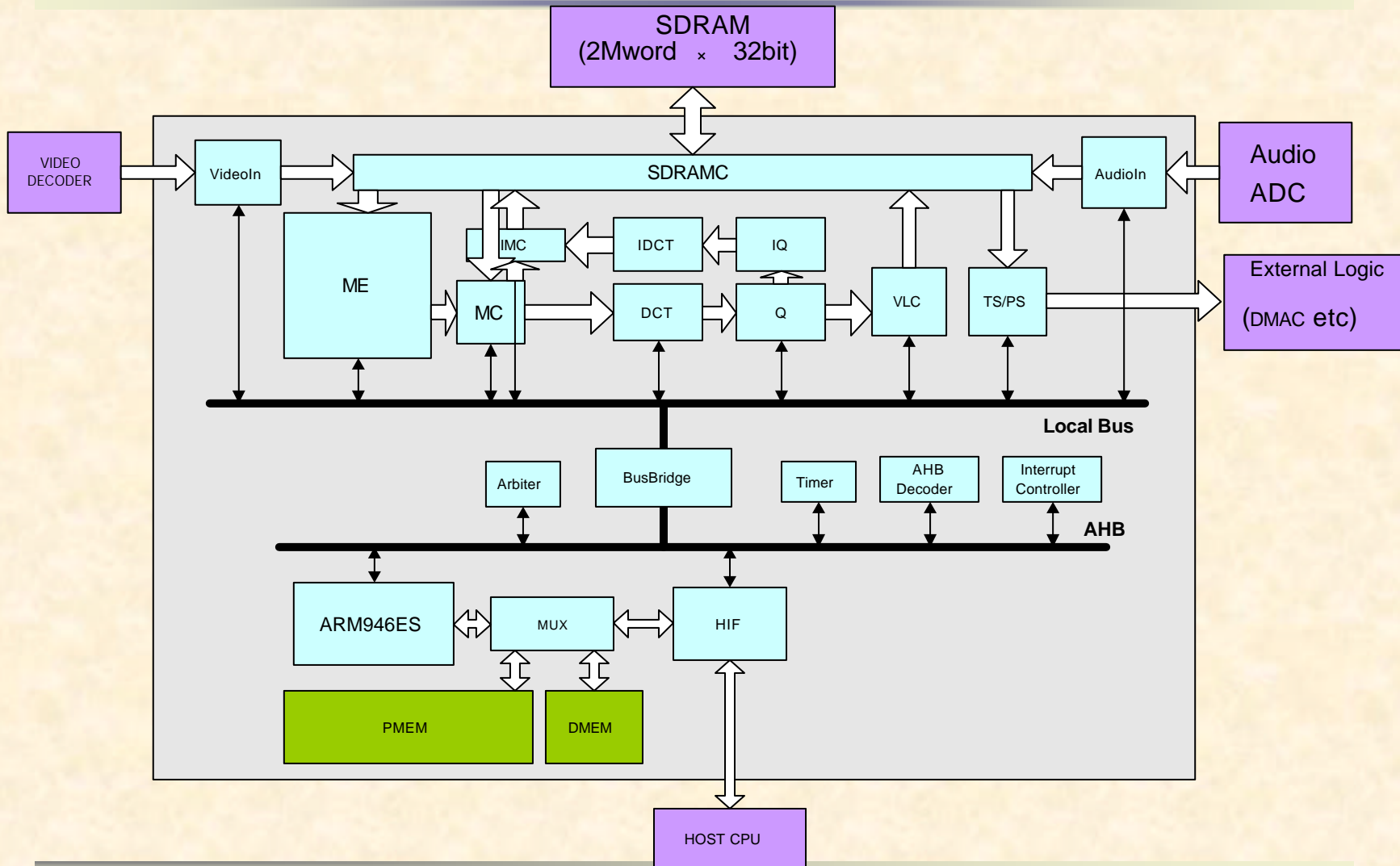
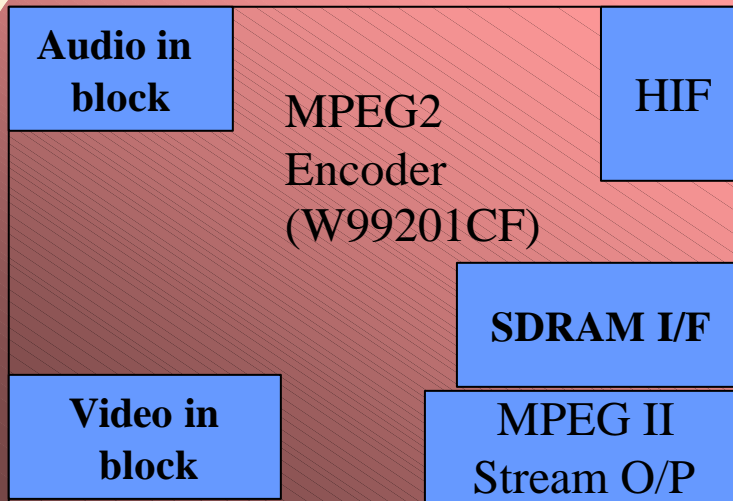


W99201 Architecture overview



W99201 Architecture overview

6 (~24) bit/sample x 2channel
sampling frequency: 48 / 44.1 / 32kHz
Audio Master Clock Generation from 27 MHz
MPEG-1 Audio (IS11172-3) Layer II (32 ~ 384kbit/s) or 2 channel Dolby AC-3
Philips I2S or 32-SCLK serial input format



- Host I/F: 8 bit parallel, direct connection to 8052 (Winbond) CPU

- Memory I/F: 64Mbit (x32bit width) SDRAM

- MPEG-2 Systems (IS13818-1) Transport Stream or Program Stream

- Stream output I/F: 8 bit parallel (simple byte flow or DMA interface)

Stream standard: MP@ML in MPEG-2 Video (IS13818-2)

Picture size/frame rate

Horizontal size: 720, 704 (ITU-R 601 format) and 352 (Half-D1)

Vertical size: 480(NTSC) and 576(PAL)

Bit rate control: VBR (Variable Bit Rate) and CBR (Constant Bit Rate)

VBR: 2~15Mbit/s One pass VBR (Max and Min rate controlled)

CBR: 2~15Mbit/s (601 format), 1~15Mbit/s (Half-D1)

Video input :ITU-R656 and ITU-R601 8 bit Y/Cb/Cr 4:2:2 video format (27MHz)

Flexible GOP structures: ILL..., IPPP..., IBP, IBBP (M= 1~3)

VBI extractions (Closed Caption, CGMS and European Tele-text (when Micronas video decoder is used))

W99201 demo board Function Block Description

